Introduction

It is important to consume as little current as possible when monitoring battery level as not to completely drain the source. This document will detail how to implement a low current 1.0 µA battery voltage monitor with the wake-sleep method.

This solution makes use of three essential blocks: Analog Comparator (ACMP), Wake-Sleep Controller (WSCtrl) and Low Frequency Oscillator (LFOSC). The method which this app note describes can be applied to any Analog Block (ACMP or ADC) and any other devices with wake-sleep controllers. For more examples, see AN-1076 Wake/Sleep Timing Generator.

Analog Comparator

The Analog Comparator will be used to monitor battery level. Select an ACMP from the components window and check the positive input source; this pin will need to be configured as an "Analog I/O". For ACMP0, that pin is PIN6. By default, the pin has a 1 MΩ pull-down resistor. Configure this to "Floating" to avoid the extra pull-down current.

For the negative input, choose the threshold to compare with battery voltage. Use gain for voltages > 1.2V. In Figure 1, the negative input is set to 1000mV and gain set to 0.33x. Assuming a single cell LiION battery, a low voltage indication threshold is 3.0V.

All Analog Blocks require the use of the bandgap reference. The bandgap consumes ~35uA when ON and is powered by a voltage > 2.7V.

This voltage is supplied either by VDD or an internal charge pump. If not forced on, the bandgap can be turned on and off by the analog block power on and off signal. Using the bandgap only when needed reduces the average current consumed.

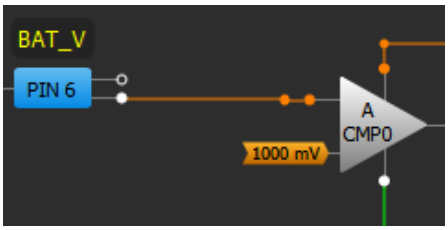


Figure 1. Analog In PIN6 hooked up to ACMP0

Wake-Sleep Controller & LF OSC

The Analog power consumption can be reduced by using the wake-sleep method. This method turns on the analog blocks for a short amount of time (wake), latches in the values and then turns off the block. This is repeated every wake-sleep period.

This method can be implemented in GPAK with CNT/DLY/WSCtrl, which is sourced by the low current Low Frequency Oscillator. Connecting the wake sleep controller to the "PWR ON/OFF" and "WAKE SLEEP" inputs of the ACMP will effectively control when analog blocks ACMP and BG are enabled and disabled. The WSCtrl operates the same as a counter. It loads in the counter data, counts down until zero and generates a 'High' when the counter data equals zero. An ACMP block is powered on if it's "PWR ON" input is 'High'. The ACMP output latch is unlatched when the "WAKE SLEEP" input is 'High'. Therefore the length that WSCtrl out is 'High' is the wake period, equivalent to one LF OSC period.

Wake Period

The minimum wake period depends on bandgap and charge pump turn on time. Refer to tables in Datasheet section 5.8.1 ACMP Power On Delay. There are two tables, one for the BG setting 500 µs and another for the BG setting 100 µs. Choose the correct table based on your voltage supply range and BG setting. At VDDs < 2.7V, BG power on delay is 550 µs to allow for charge pump turn on time; this is the default setting. At VDDs > 2.7V, the charge pump does not need to turn on, therefore the turn on setting can be set to 100 µs.

For this example, we apply the first table for a worst case scenario: BG turn on time of 550 µs across full temperature range. According to the column "maximum", the longest time it would take for the ACMP to turn on is 2092.2 µs. Therefore, the WSCtrl's wake time must be greater than the 2092.2 µs.

To enable the Wake Sleep Controller, select WSCtrl macro-cell and configure the mode to "wake sleep controller". Enable the analog block wake sleep through the WSCtrl settings (See Appendix A). Set the LF OSC power setting to 'Forced Power On'. Adjust the counter data to the desired response period. Here, the counter data was set to 2000. The minimum pre-divider is calculated in the equations below. To achieve a minimum 2092.2µs wake period, use a pre-divider of at least 4 (rounding up from 3.6467).

$$LFOSC = 1.743kHz \text{ or } 574\mu s$$

$$\frac{2092.2\mu s}{574\mu s} = 3.6467$$

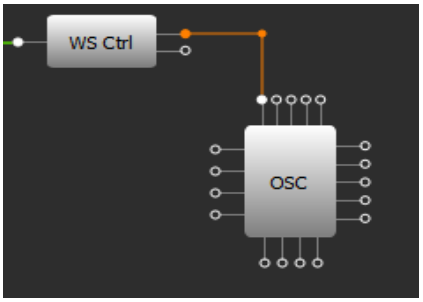


Figure 2. WS Controller to OSC connection

Analog Comparator Current Consumption

The two control signals: "PWR UP" (bottom input) which turns the ACMP on/off and "WAKE SLEEP" (top input) which controls the output latching mechanism, work together to save current.

Table 1 shows a comparison of quiescent current measured for different combinations of "PWR UP" and "WAKE SLEEP" signals. If configured correctly as shown in Figure 3, the quiescent current is limited by the LF OSC rather than the analog bandgap at ~1µA. Otherwise, the bandgap is always on which consumes ~35µA of current. Refer to datasheet section 5.6 Typical Current Consumption for expected component power usage.

PWR	W/S	Quiescent Current
On	Off	44µA
On	W/S	44µA
W/S	*W/S*	*1.0µA (see functionality waveform)*

Table 1. WS and PWR UP Configurations

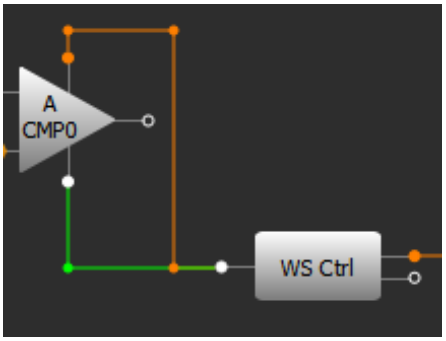


Figure 3. ACMP Wake Sleep and PWR UP inputs connected to WS Controller

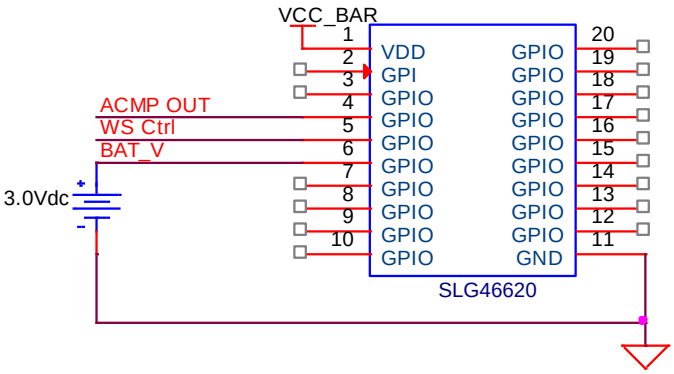


Figure 4. Typical Application Circuit

Typical Application Circuit

The typical application circuit in Figure 4, has been bench tested using the on-board emulator and an external power supply. The battery can be used to power the chip as well, down to the minimum chip supply 1.71V.

Set the signal generator on BAT_V (PIN#6) as a constant voltage signal greater than the 3V ACMP IN- threshold. Start and Stop the signal generator to observe changes at the output.

Waveforms can be found in the section Functionality Waveforms.

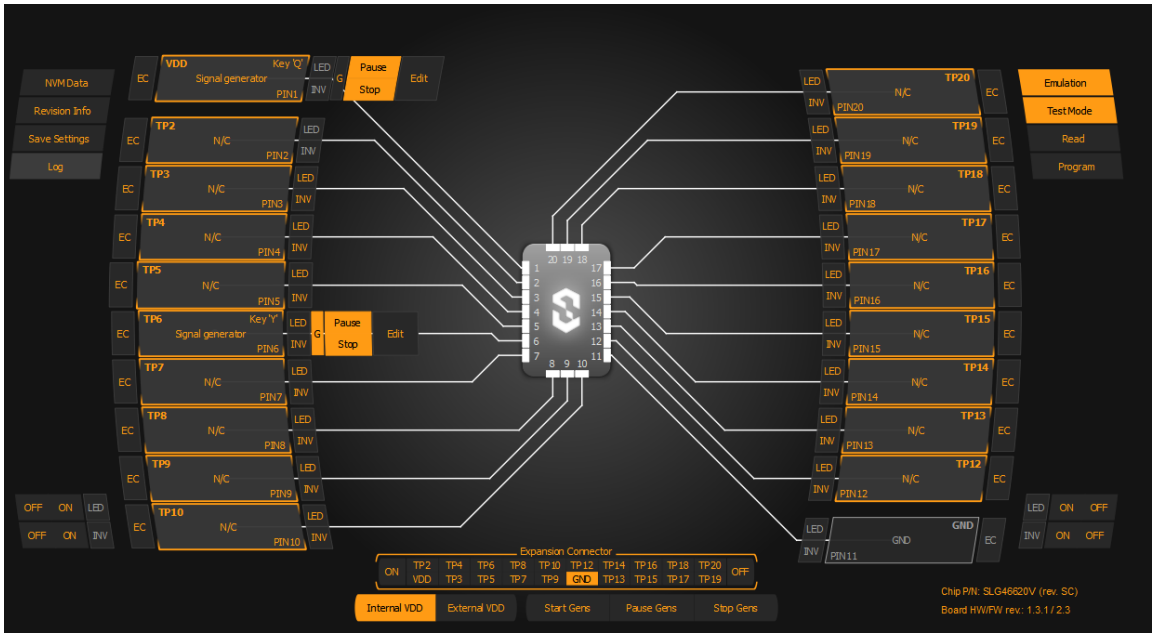


Figure 5. Emulator Configuration

Typical Response Time

The typical response time is determined by the ACMP power-on delay and wake-sleep period.

In this example, the wake-sleep period is 4.63 seconds (counter data 2000) and ACMP Power On Delay is 2092.2 µs.

$$T_{response\_max} = T_{1st} + T_{sleep}$$

$$T_{response\_max} = 2092.2\mu s + 4.63s = 4.63s$$

The power on delay is << sleep time, so the response period is essentially equal to the sleep period.

Conclusion

The wake-sleep method is both an energy and resource efficient solution because it cuts current consumption from 44µA to 1µA and uses only one component, the WSCtrl. Any battery voltage within the GPAK operating range can use an ACMP to self-monitor its voltage; resistor dividers cost no extra current. For correct operation across voltage and temperature, refer to the datasheet section 5.8.1 for minimum ACMP power on delay and adjust the LF OSC accordingly. Use this method for all other GPAK devices where Wake-Sleep Controllers exist.

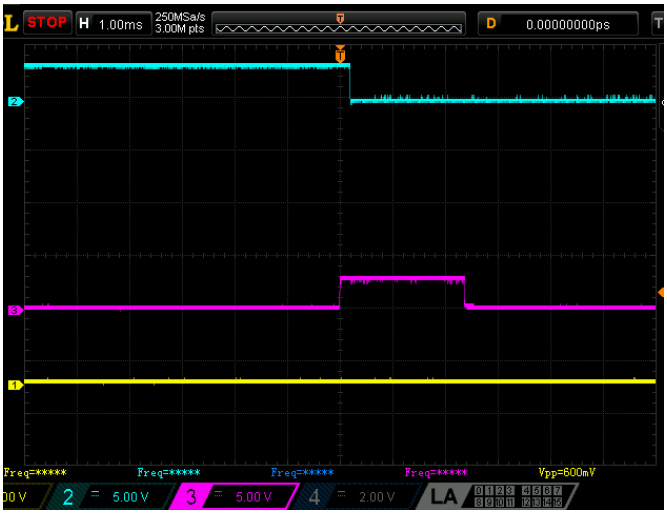
Functionality Waveforms

Channel 2 (light blue) – PIN#4 (ACMP0)

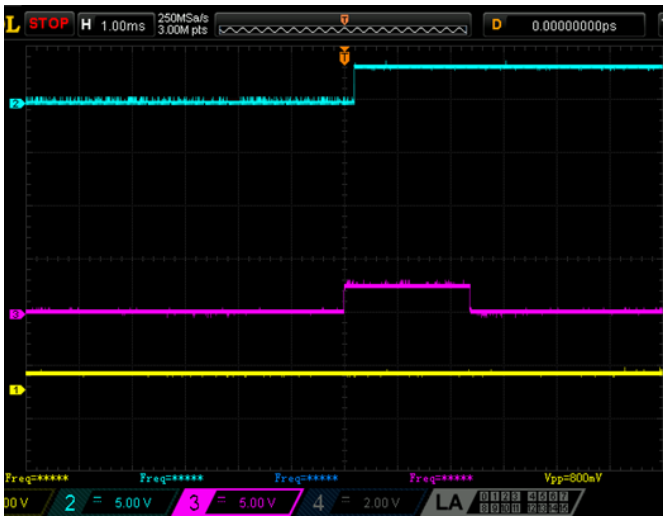
Channel 3 (magenta) – PIN#5 (WSCtrl)

Channel 1 (yellow) – PIN#6 (BAT_V)

Waveform 1 and 2 displays the functionality of the low current battery voltage sense circuit. At every Wake, the ACMP samples the input. At the end of the wake, the output is latched. In the event that the Wake-Sleep input is disconnected, the ACMP sample is not latched as shown in Waveform 3.

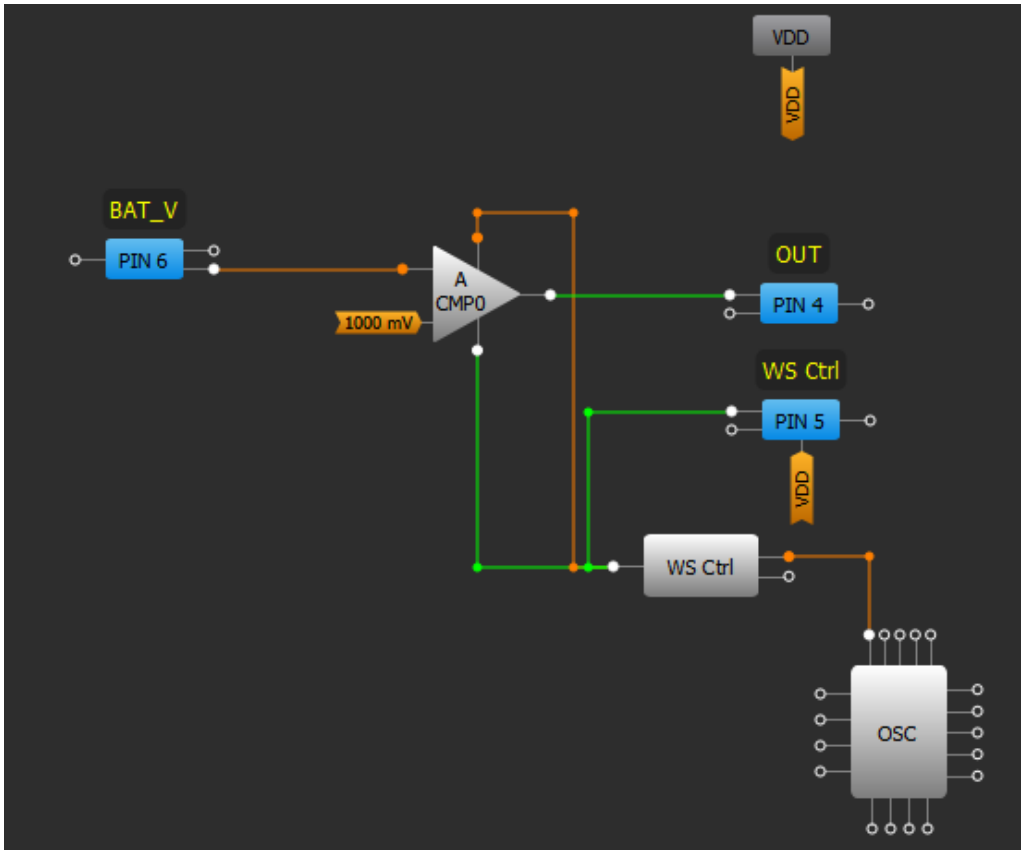


Waveform 1. Wake-Sleep on PWR and W/S ACMP and Battery Voltage < 1000mV



Waveform 2. Wake-Sleep on PWR and W/S ACMP and Battery Voltage >

Appendix A. GP Design



A CMP0

Hysteresis:	Disable
Low bandwidth:	Disable
Buffer bandwidth:	1 kHz
Speed:	None
Input 100uA current source:	Disable
IN+ gain:	Disable

Connections

IN+ source:	PIN 6
IN- source:	1000 mV

PIN 6

I/O selection:	Analog input/outpu
Input mode: OE = 0	Analog input
Output mode: OE = 1	Analog output
Resistor:	Floating
Resistor value:	Floating
Reset:	None
Bypass:	None
Edge detect mode:	None

WS Ctrl/14-bit CNT0/DLY0

Type:	Wake sleep controll
Mode:	Counter
ACMPx wake sleep:	Enable
ADC wake sleep:	Disable
Wake sleep output state:	Force sleep (Low),
Counter data:	2000
	(Range: 1 - 16383)
Output period:	4.63 s Formula
Edge select:	Both
Counter value control:	None
DFF bypass enable:	None

Connections

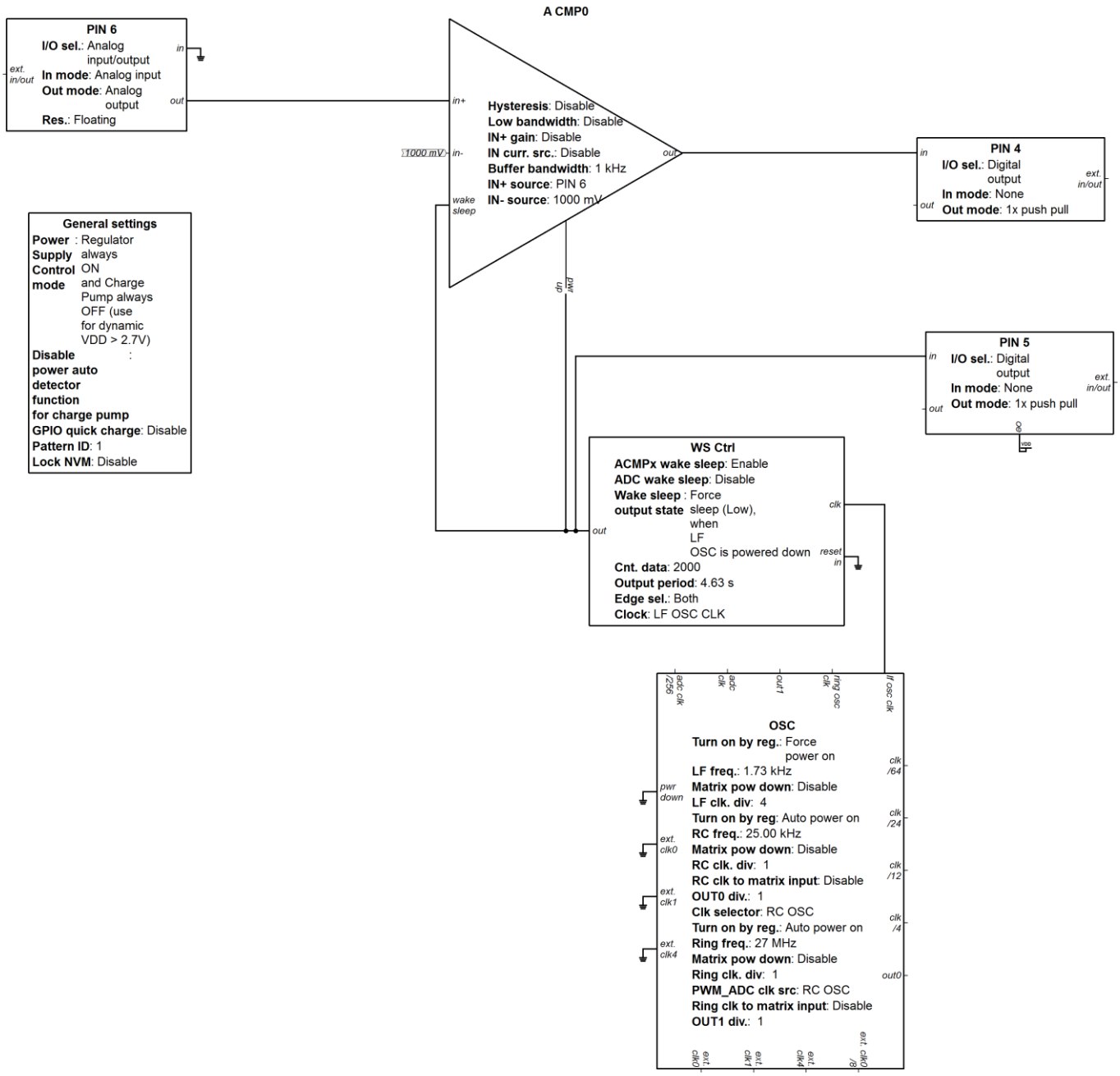
FSM data:	None
Clock:	LF OSC CLK
Clock source:	LF OSC CLK Freq.

OSC

LF OSC | RC OSC | RING OSC

LF OSC power mode:	Force power on
LF OSC frequency:	1.73 kHz
LF matrix power down:	Disable
LF clock predivider by:	4

Appendix B. Block Diagram



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