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H8SX Family

0.18-µm Flash Memory Reprogramming in the User Program Mode

Introduction

This application note describes the reprogramming of flash memory (the user MAT) via a clock-synchronous communications interface in the user boot mode of the H8SX/1582F, and mainly concerns the slave (receive) side. That is, unless otherwise specified, the descriptions are related to the slave side.

Target Device

H8SX/1582F

Contents

1. Specifications

1.1 Specification Outline

The user starts by downloading the erasing or programming module to the RAM and then calls subroutines to erase/program the flash memory.

In this sample task, data for reprogramming are placed in the flash memory on the master side and sent to the slave side by clock synchronous communications. The following procedure is then applied to reprogram the flash memory on the slave side. A sample configuration for on-board reprogramming is shown in figure 1, and the connections for clock synchronous communications between the master and slave are shown in figure 2.

- Power-on resets are applied, and the slave boots up in the user boot mode and the master boots up in the user mode.
- When master side switch 0 (SW0) is turned on, the master side sends the reprogramming command to the slave side, and the slave side reprograms its own flash memory.
- The data in the flash memory reprogrammed by the user program mode.
- The master side sends the data to be reprogrammed from its own flash memory to the slave side.
- The data for reprogramming are transferred in clock synchronous mode via serial communications interface (SCI) 3. The data is transmitted from the master side and received on the slave side.
- On both the master and slave sides, PD7 is low and PD6 is high while the flash memory is being reprogrammed, and PD7 is high and PD6 is low on completion of reprogramming.

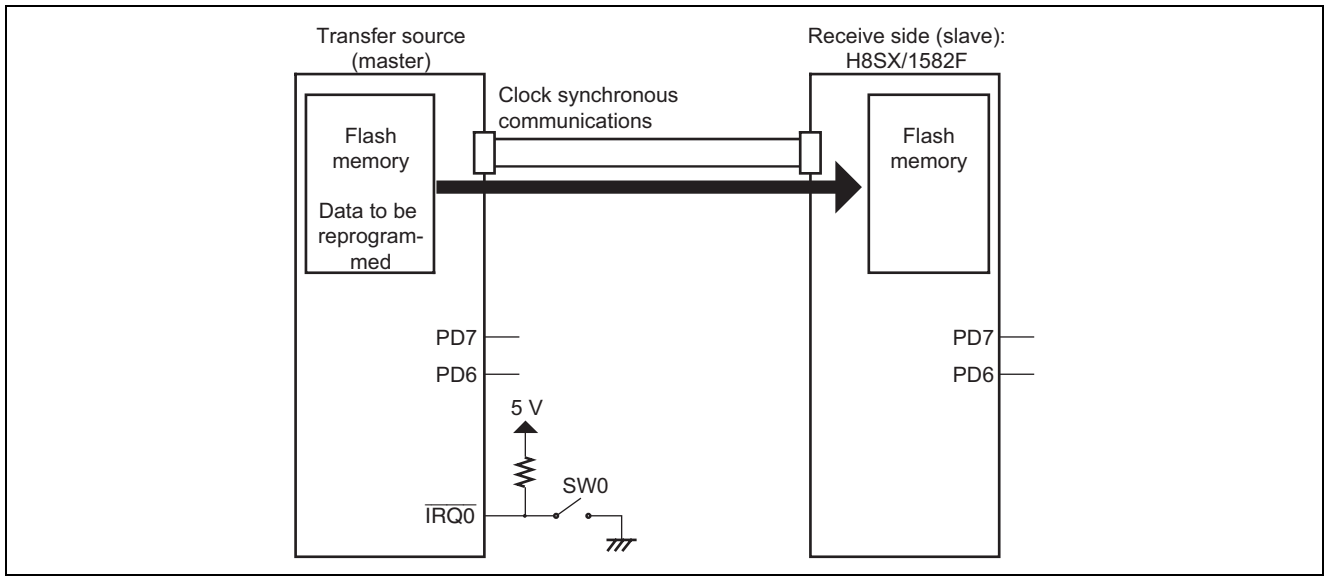


Figure 1 Sample Configuration for On-Board Reprogramming

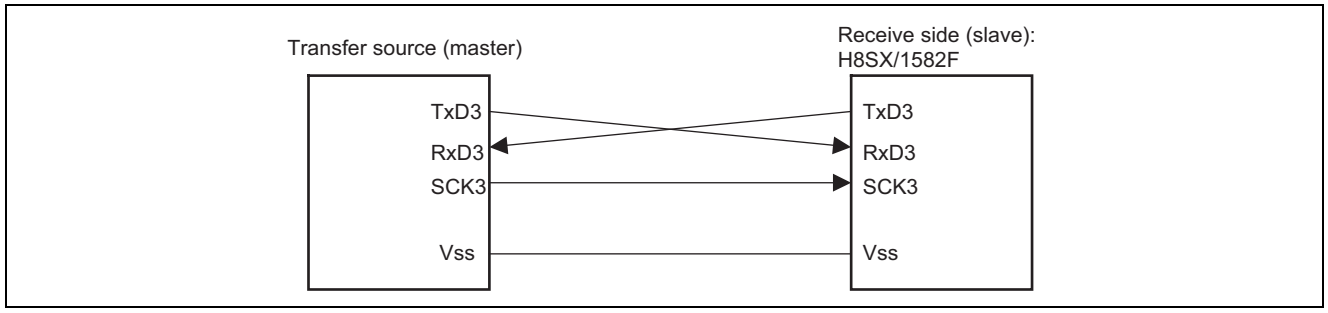


Figure 2 Wiring for Clock Synchronous Communications

1.2 User Program Mode

The RAM transfer program, clock synchronous communications program, and programming/erasing program must be written to the user boot MAT in advance.

1.3 Specifications for Communications

The specifications for communications between the master and slave in this sample task are listed below.

1.3.1 Type of Communications

Table 1 Type of Communications

Item	Setting
Transfer rate	2.5 Mbps
Type	Clock synchronous communications
Data bits	8 bits (1 byte)

1.3.2 Communications Commands

Table 2 Communications Commands

Command Name	Constant Name	Command Data
Start reprogramming	FSTART	H'10
Erase	ERASE	H'11
Write	WRITE	H'12
Read status	STATUSREAD	H'13
128-byte transmission request	TRS128	H'14

1.3.3 State Indicators

Table 3 State Indicators

Status Name	Constant Name	Status Data
Normal	OK	H'00
Erase command error	ER_ECMD	H'C1
Erase download error	ER_EDWNLD	H'C2
Erase initialization error	ER_EINIT	H'C3
Erase error	ER_ERASE	H'C4
Program command error	ER_WCMD	H'A1
Program download error	ER_WDWNLD	H'A2
Program initialization error	ER_WINIT	H'A3
Program error	ER_WRITE	H'A4

1.3.4 Specifying Blocks to be Erased

The erase command "ERASE" is sent from the master to the slave and is immediately followed by an indicator of the block numbers of blocks to be erased. The communications format for block erasure is given in table 4. Block settings are made in a 4-byte (32-bit) unit where bits 11 to 0 correspond to blocks 11 to 0. Since bits 31 to 12 are not used, always set them to 0. Set bits corresponding to blocks to be erased to 1 and bits corresponding to blocks that are not to be erased to 0. An example of the data transmitted to erase block 11 is given in table 5.

Table 4 Correspondence of Blocks to be Erased

Bit	Erased Block	Setting	Description
31 to 12	Not used	0 fixed	Not used. Set 0.
11 to 0	EB11 to EB0	0/1	0: The corresponding block is not erased. 1: The corresponding block is erased.

Table 5 Example of Data for Transmission to Erase Block 11

	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte
Item	Erase command (ERASE)	Erase block			
Byte	H'11	H'00	H'00	H'08	H'00
Bit	00010001	00000000	00000000	00001000	00000000
	MSB LSB	MSB LSB	MSB LSB	MSB LSB	MSB LSB

Note: The data is transmitted in byte units, with the LSB first.

1.4 Memory Map

The memory map for this sample task is given as figure 3.

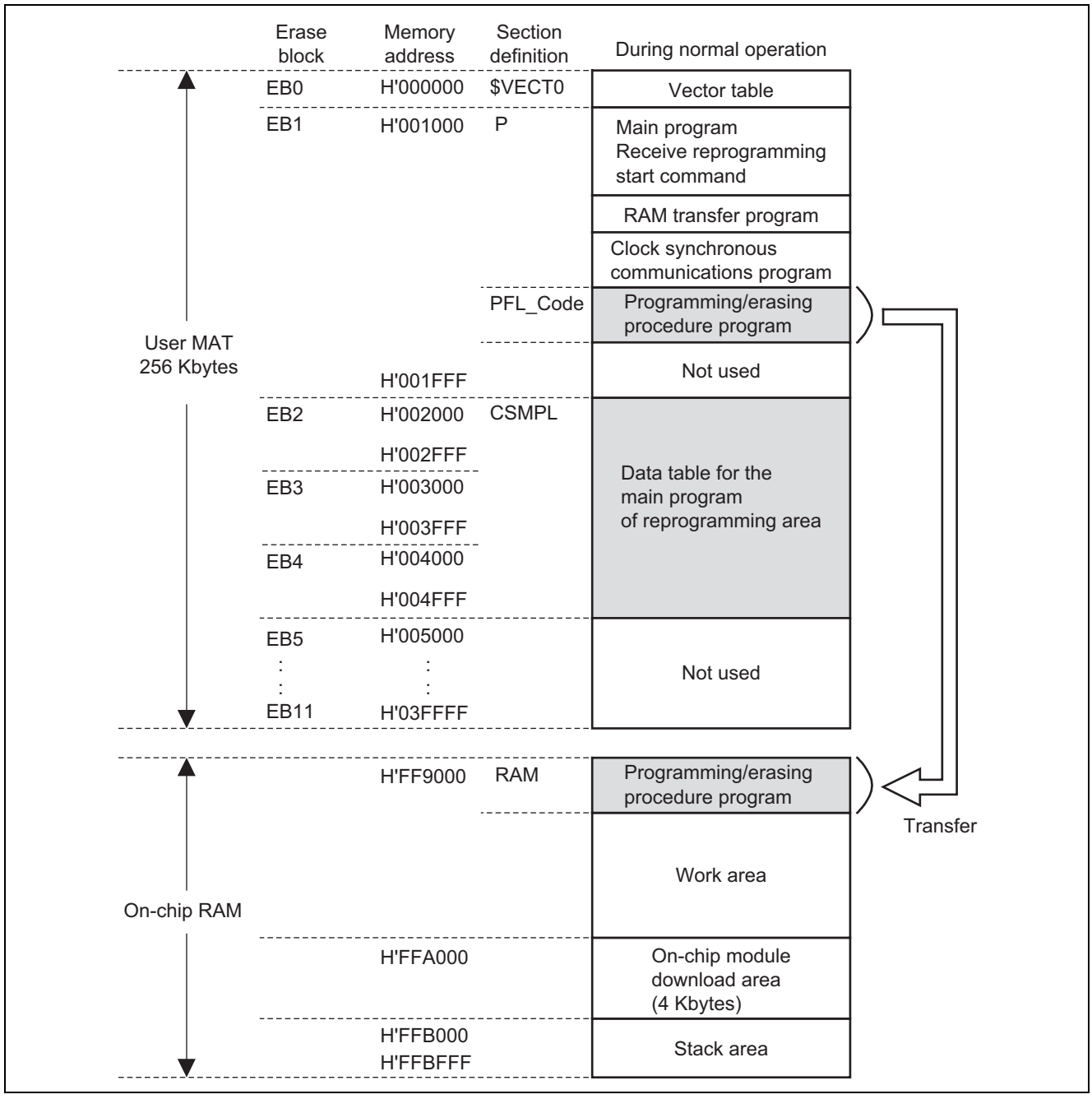


Figure 3 Memory Map

2. Applicable Conditions

Table 6 Applicable Conditions

Item	Description
Operating frequency	Input clock: 5 MHz System clock (Iϕ): 40 MHz Peripheral module clock (Pϕ): 20 MHz External bus clock (Bϕ): 20 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)
On-board programming mode	User program mode
Development tool	High-performance Embedded Workshop Ver. 4.00.02
C/C++ compiler	Renesas Technology Corp. H8S, H8/300 Series C/C++ Compiler Ver. 6.01.00
Compiler option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)
Optimizing linkage editor option	-rom = PFL_Code = RAM

Table 7 Section Setting

Address	Section Name	Description
H'001000	P	Program area
	PFL_Code	Area for storing programming/erasing procedure program
	CSMPL	Area for reprogramming
H'FF9000	RAM	Area for transferring programming/erasing procedure program

3. Description of Modules Used

3.1 User Program Mode

3.1.1 User MAT and User Boot MAT

The on-chip flash memory consists of the two memory units (memory MATs) listed in table 8. Both are allocated to the same address. The user program mode is an arbitrary boot program that suits the user system, and the user MAT can be programmed/erased.

Table 8 Memory MATs

Memory MAT	Activation	Amount of Memory Used
User MAT	Activates when a power-on reset is performed in the user mode	256 Kbytes
User boot MAT	Activates when a power-on reset is performed in the user boot mode	10 Kbytes

3.1.2 Downloading the On-Chip Program

Erasing/programming of the flash memory on this LSI is done by first downloading the on-chip module for either erasing/programming to the on-chip RAM and then running the individual programs.

The destination address for downloading is determined by the setting of the download destination specification register (FTDAR). For the RAM address map after downloading, refer to figure 4. As the figure shows, the on-chip RAM area is the destination for downloading of the erasing and programming programs. The corresponding program must be downloaded to the RAM area indicated by FTDAR prior to the required processing.

During erasing/programming, take care to ensure that the download area does not overlap with an area in use by the user.

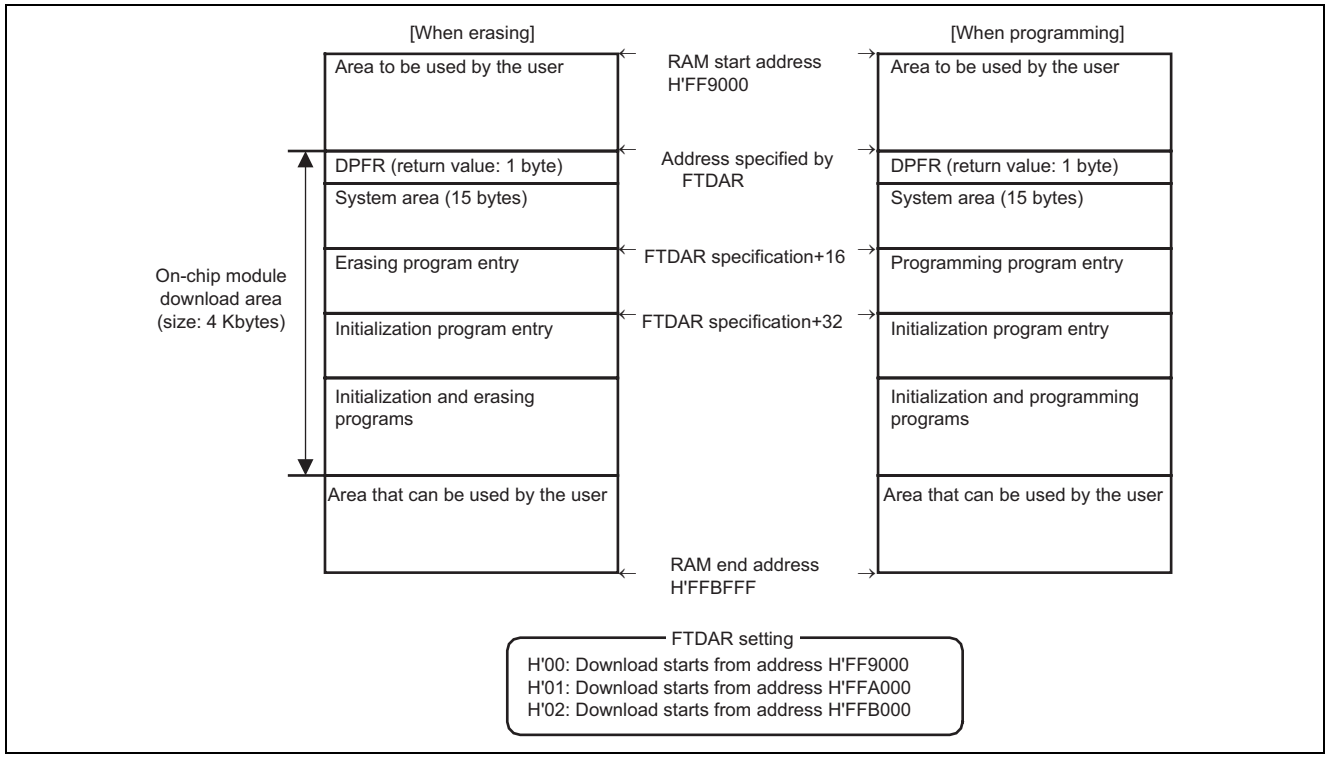


Figure 4 Normal Operation

3.2 Block Configuration

Erase blocks of the user MAT are listed in table 9.

Table 9 User MAT Erase Blocks

Block	Unit of Erasure	Addresses
EB0	4 Kbytes	H'000000 to H'000FFF
EB1	4 Kbytes	H'001000 to H'001FFF
EB2	4 Kbytes	H'002000 to H'002FFF
EB3	4 Kbytes	H'003000 to H'003FFF
EB4	4 Kbytes	H'004000 to H'004FFF
EB5	4 Kbytes	H'005000 to H'005FFF
EB6	4 Kbytes	H'006000 to H'006FFF
EB7	4 Kbytes	H'007000 to H'007FFF
EB8	32 Kbytes	H'008000 to H'00FFFF
EB9	64 Kbytes	H'010000 to H'01FFFF
EB10	64 Kbytes	H'020000 to H'02FFFF
EB11	64 Kbytes	H'030000 to H'03FFFF

3.3 Serial Communications Interface

The SCI operates in the clock synchronous mode. It is used for command-related communications between the master and slave to transfer the data for reprogramming.

4. Description of Operation

4.1 User MAT Reprogramming Procedure

User MAT reprogramming procedure in the user program mode is given in figure 5.

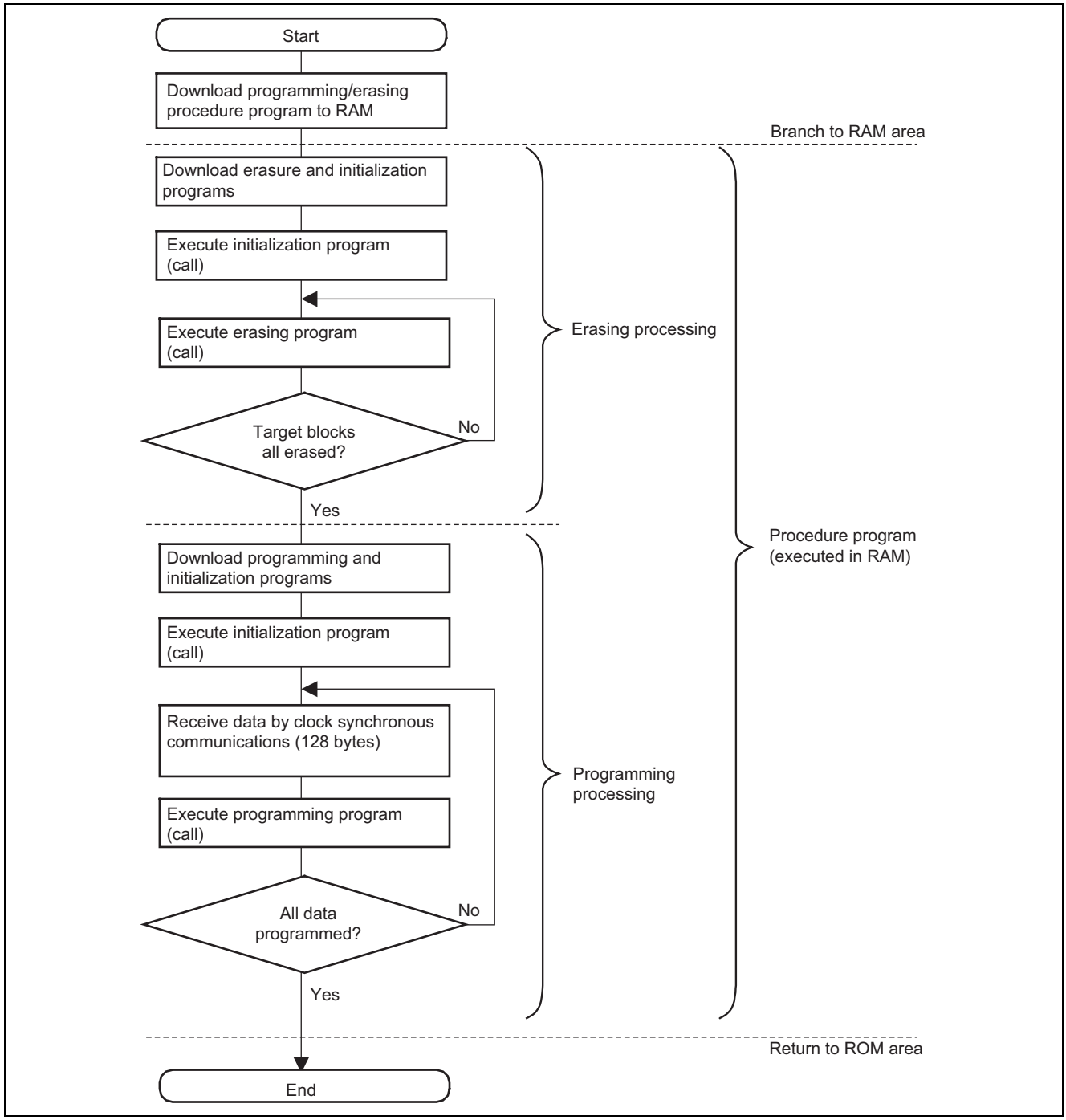


Figure 5 User MAT Reprogramming Procedure

4.2 Operation Overview

4.2.1 Normal Operation

(1) The normal application accesses the data table on the user MAT. The data table is received by the master side and is reprogrammed.

(2) The RAM transfer program, clock synchronous communications program, and the programming/erasing procedure program are already reprogrammed on the slave side user MAT.

(3) Data communications between the master and slave are done in clock synchronous communications.

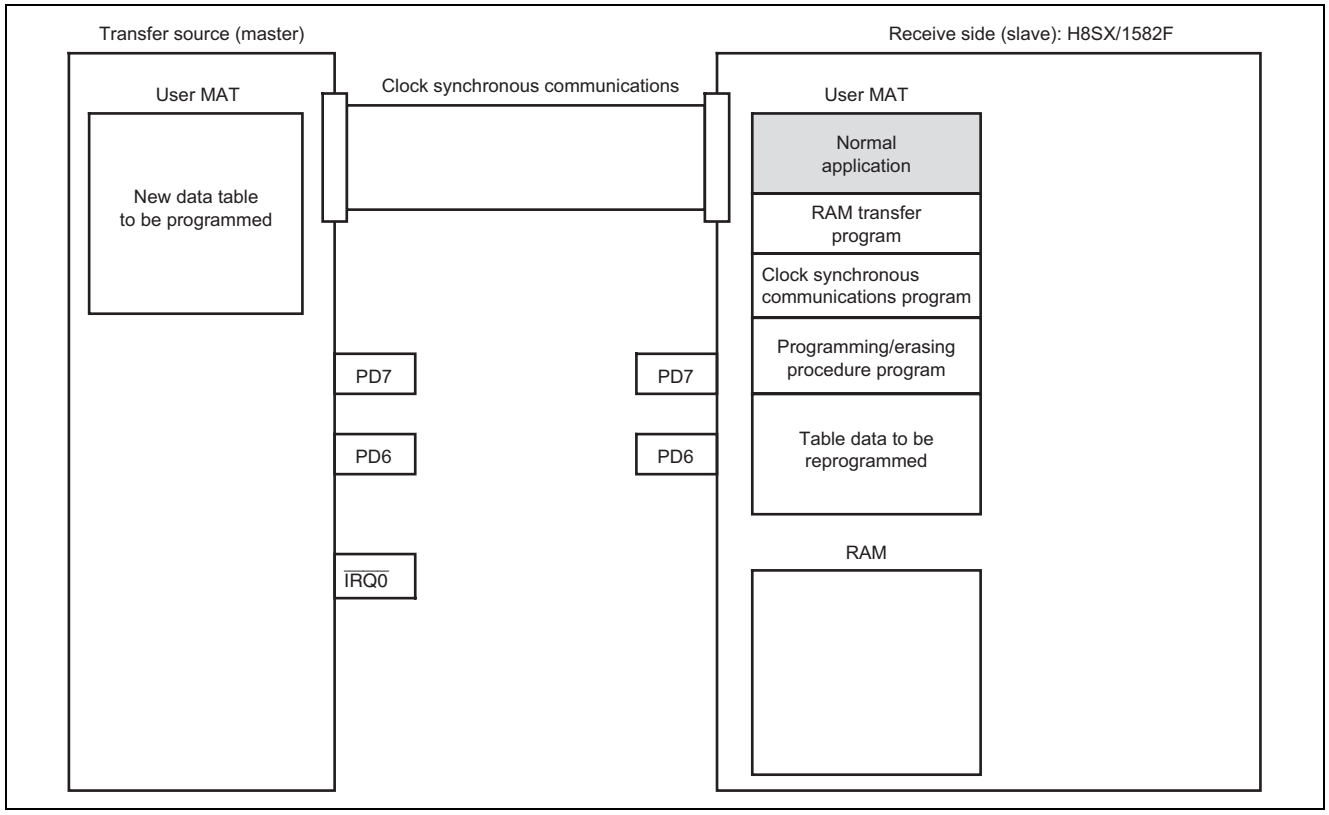


Figure 6 Normal Operation

4.2.2 Preparation of On-Board Reprogramming

(1) When a low level is input to the $\overline{IRQ0}$ pin on the master side as a trigger, the master sends the reprogramming start command "FSTART".

(2) Here, PD7 is low and PD6 is high on the master side.

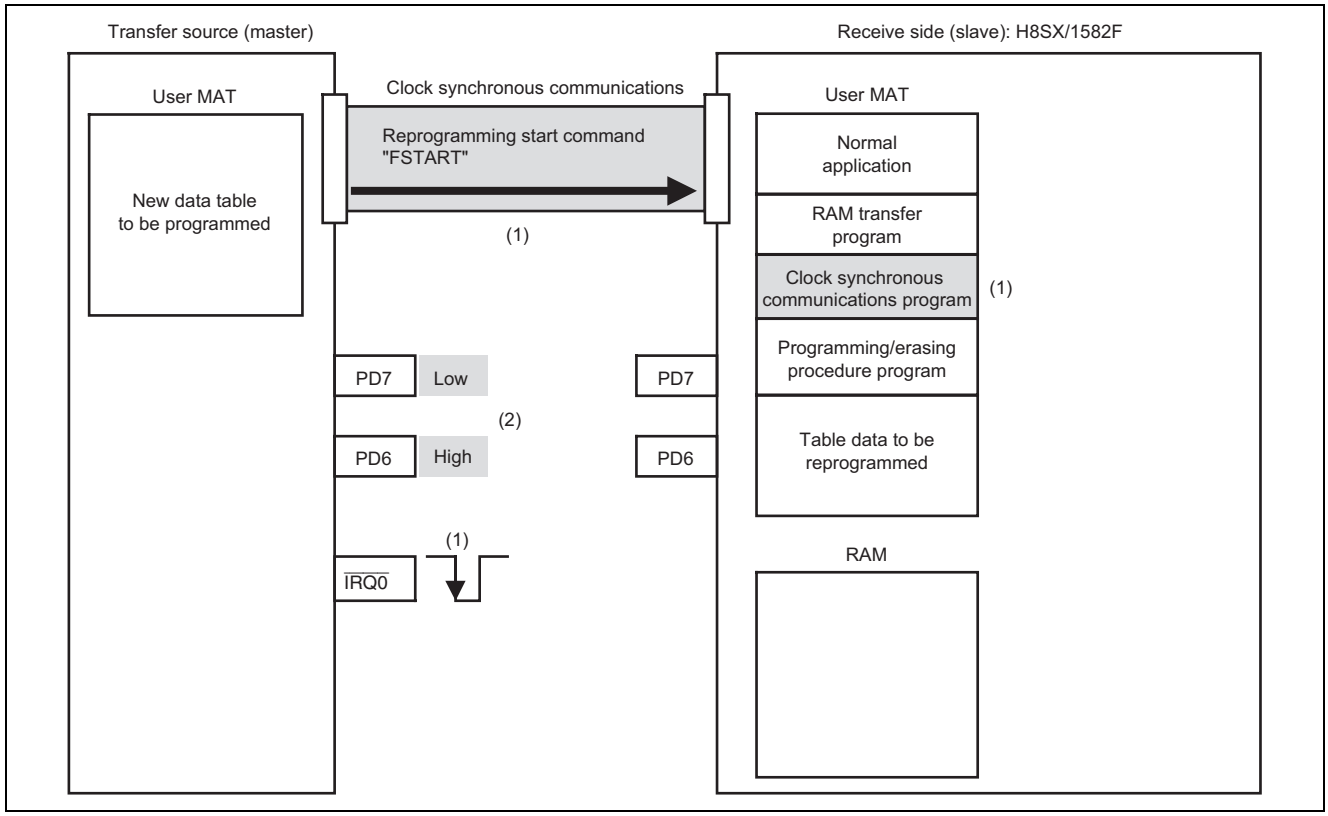


Figure 7 Preparation of On-Board Reprogramming

4.2.3 Start of On-Board Reprogramming

(1) On receiving the reprogramming start command, the slave side initiates the RAM transfer program, and sends the programming/erasing procedure command to the on-chip RAM.

(2) Here, PD7 is low and PD6 is high on the master side.

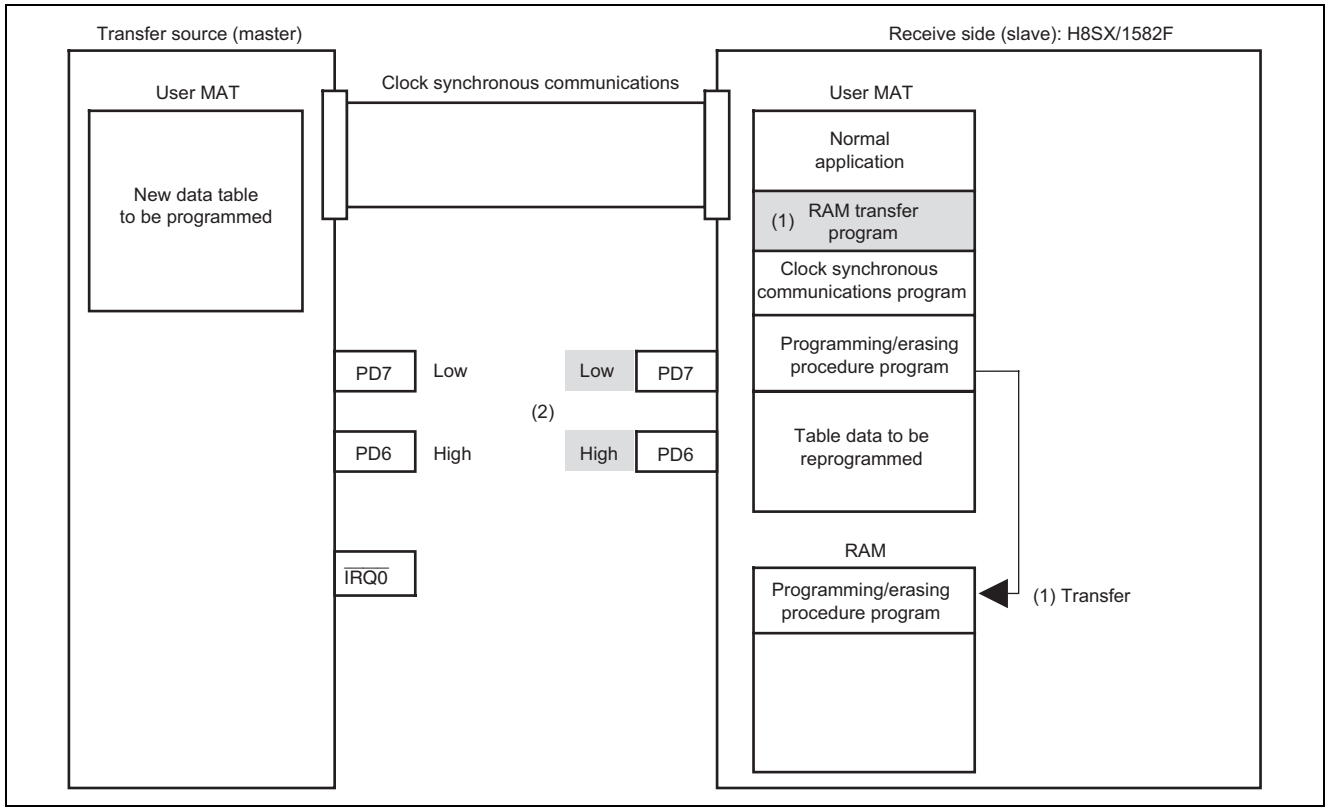


Figure 8 Start of On-Board Reprogramming

4.2.4 Activating the Programming/Erasing Procedure Program

(1) After the transfer programs have been loaded to RAM, the control branches to the programming/erasing procedure program in RAM.

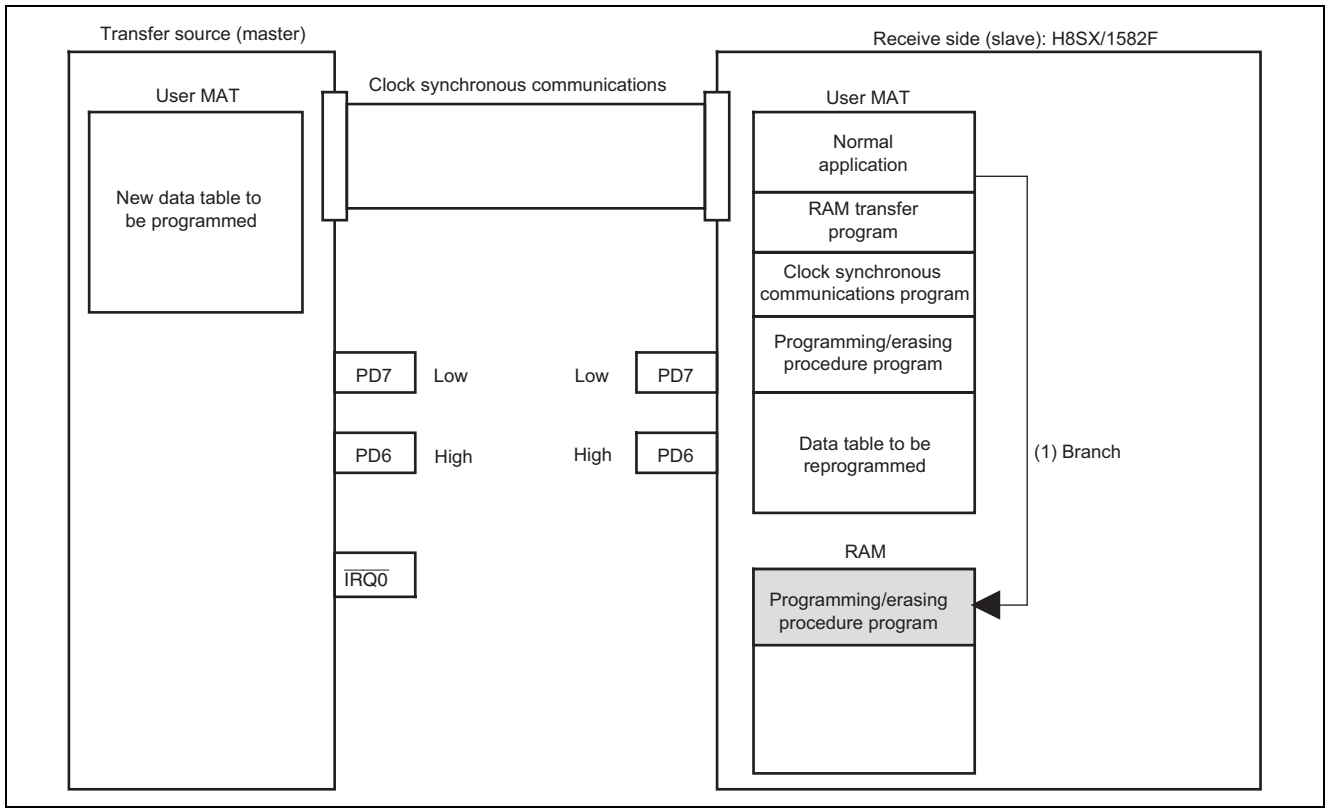


Figure 9 Activation of Programming/Erasing Procedure Program

4.2.5 Erasing User MAT

(1) The master sends the erasing command "ERASE".

(2) Registers for controlling the flash memory are set (Both the EPVB bit of the FECS register and the SCO bit of the FCCS register to 1), and the initialization program and the erasure program are downloaded.

(3) The initialization program is executed.

(4) The erasing program is executed, and the target block for erasure on the user MAT is erased.

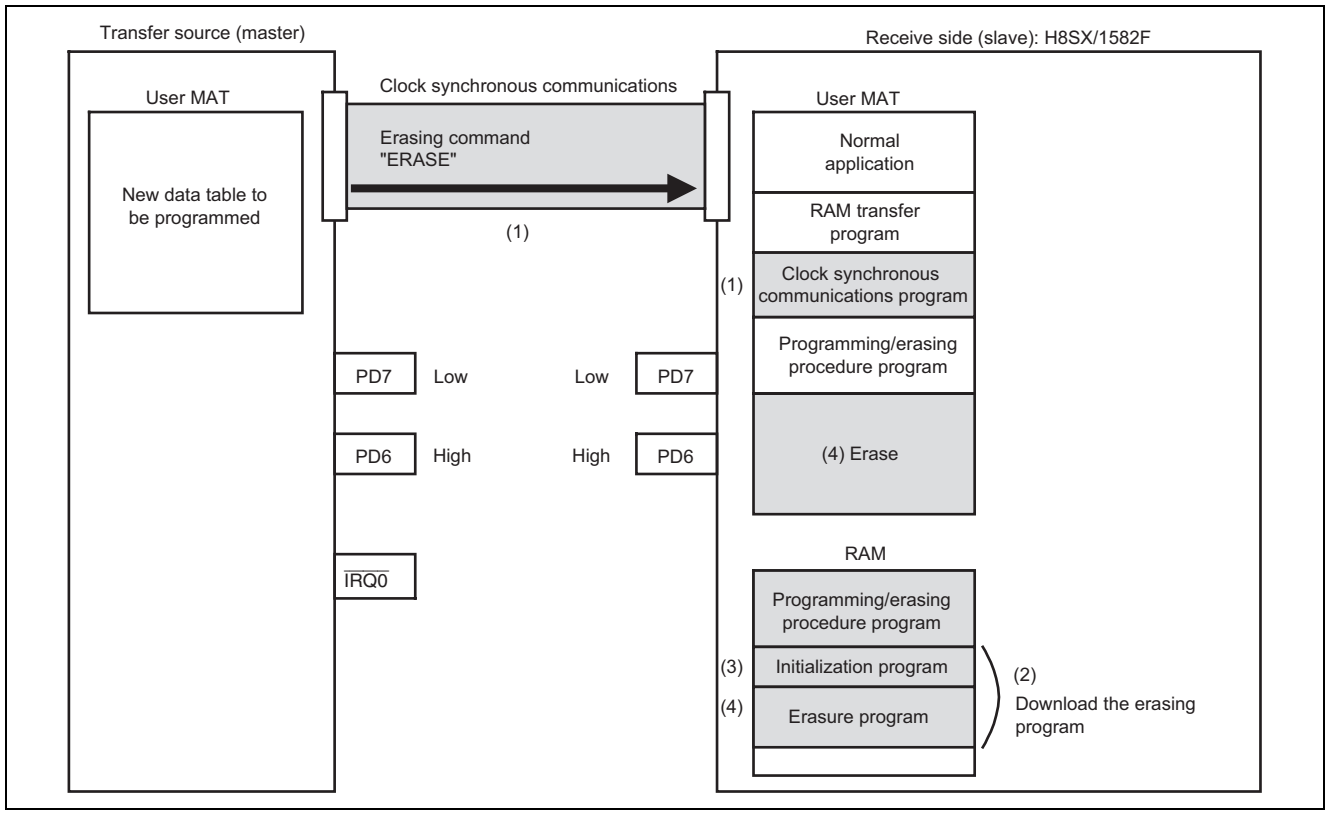


Figure 10 Erasing User MAT

4.2.6 Programming User MAT

(1) The master sends the programming command "WRITE".

(2) Registers for controlling the flash memory are set (Both the PPVS bit of the FPCS register and the SCO bit of the FCCS register to 1), and the initialization program and the programming program are downloaded.

(3) The initialization program is executed.

(4) The following a. to b. are repeated until all new data on the master side is programmed on the slave side.
   a. The receive side (slave) receives 128 bytes of new data from the transfer source (master).
   b. The receive side (slave) executes the programming program, and writes 128 bytes of data to the user MAT.

(5) On completion of programming, PD7 is high and PD6 is low on both the master and slave sides.

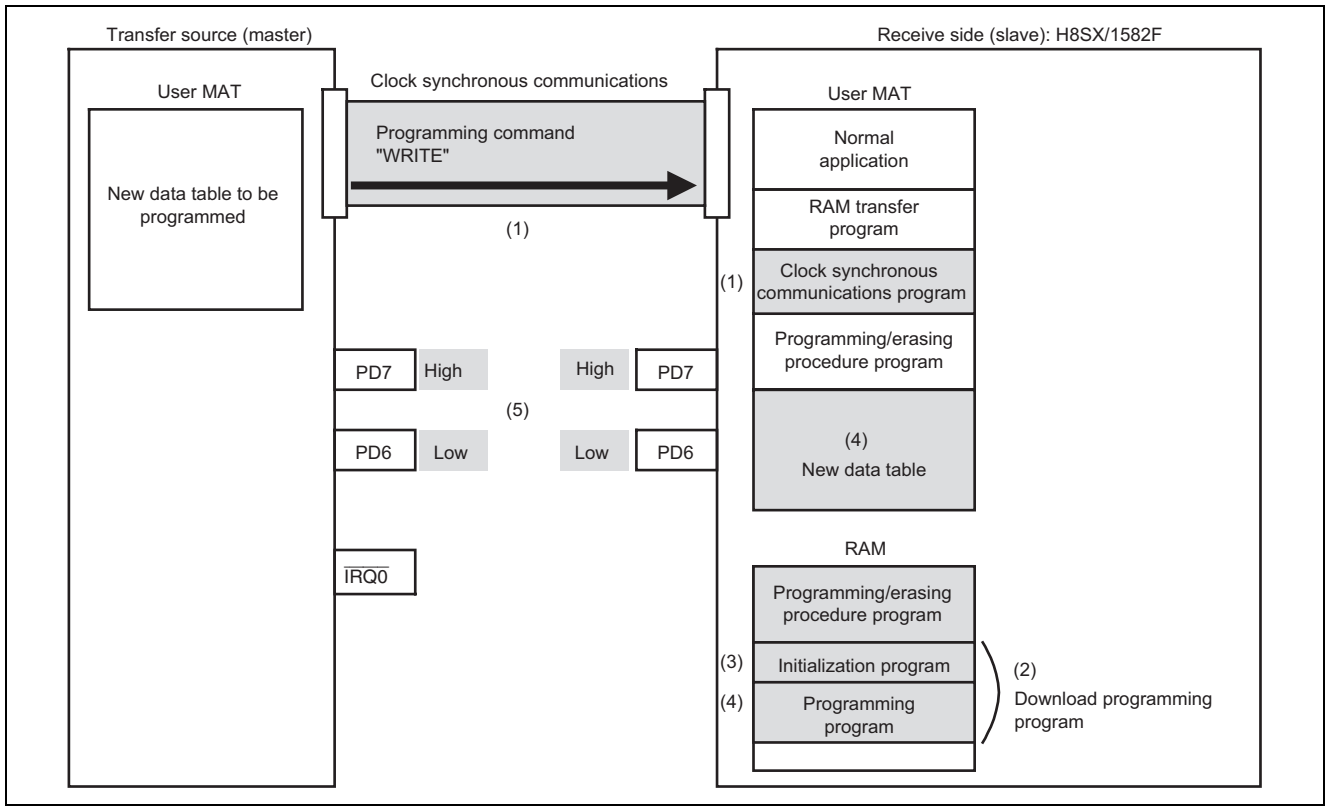


Figure 11 Programming User MAT

4.2.7 Activating the Program

(1) After a reset, the normal application that accesses the new data table is activated.

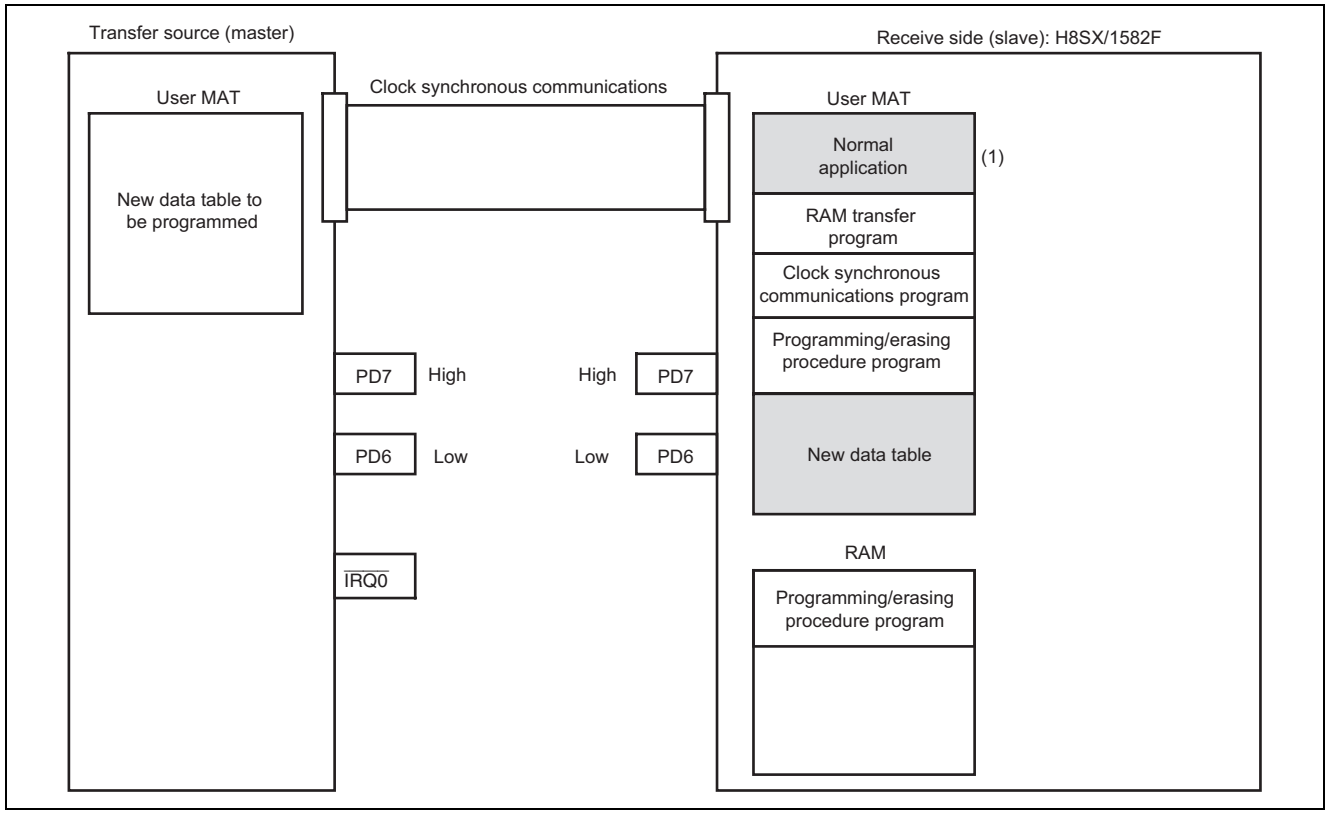


Figure 12 Activating the Program

4.3 Sequence Diagram

4.3.1 Normal Operation

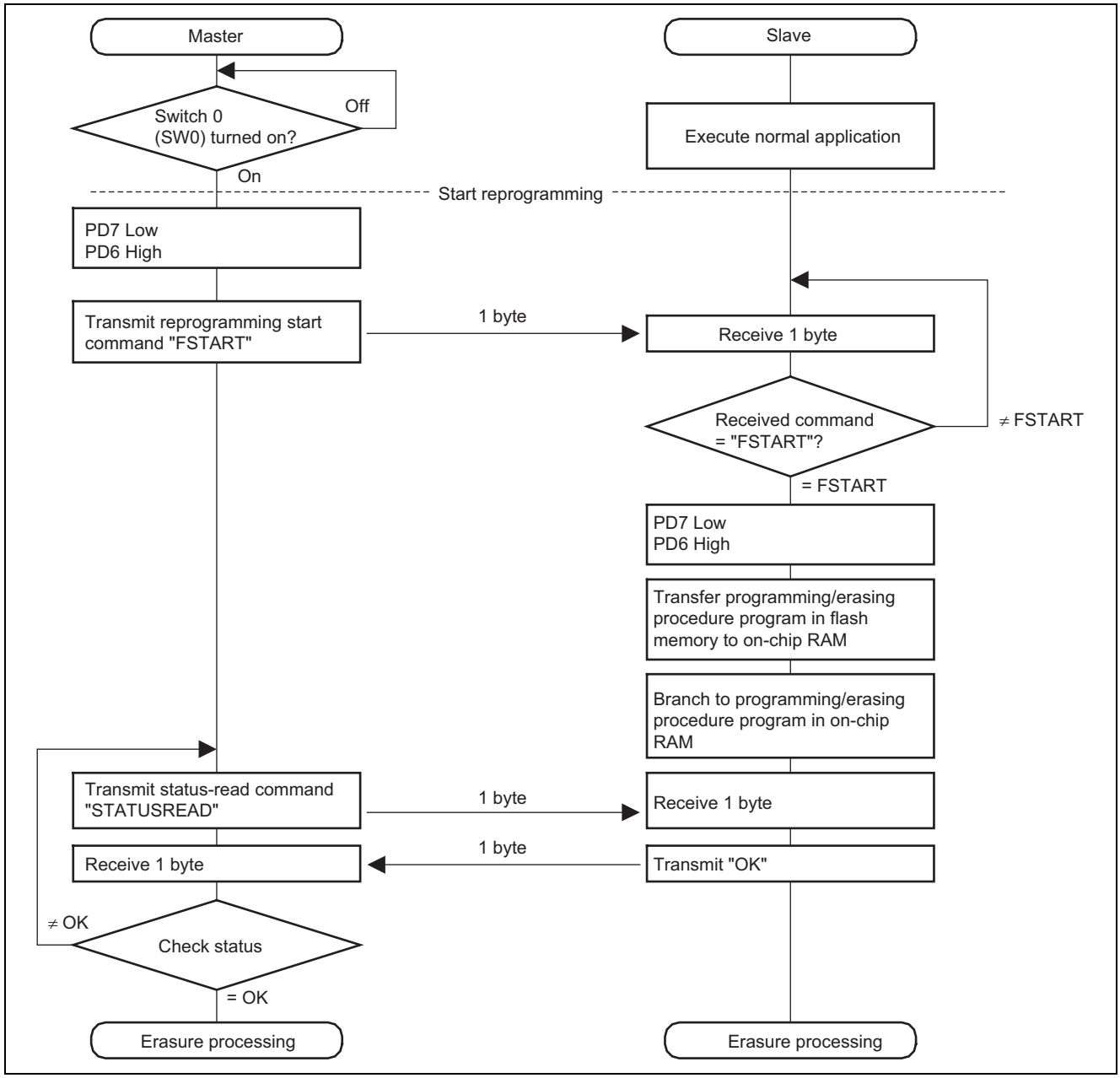


Figure 13 Normal Operation

4.3.2 Erasure Processing

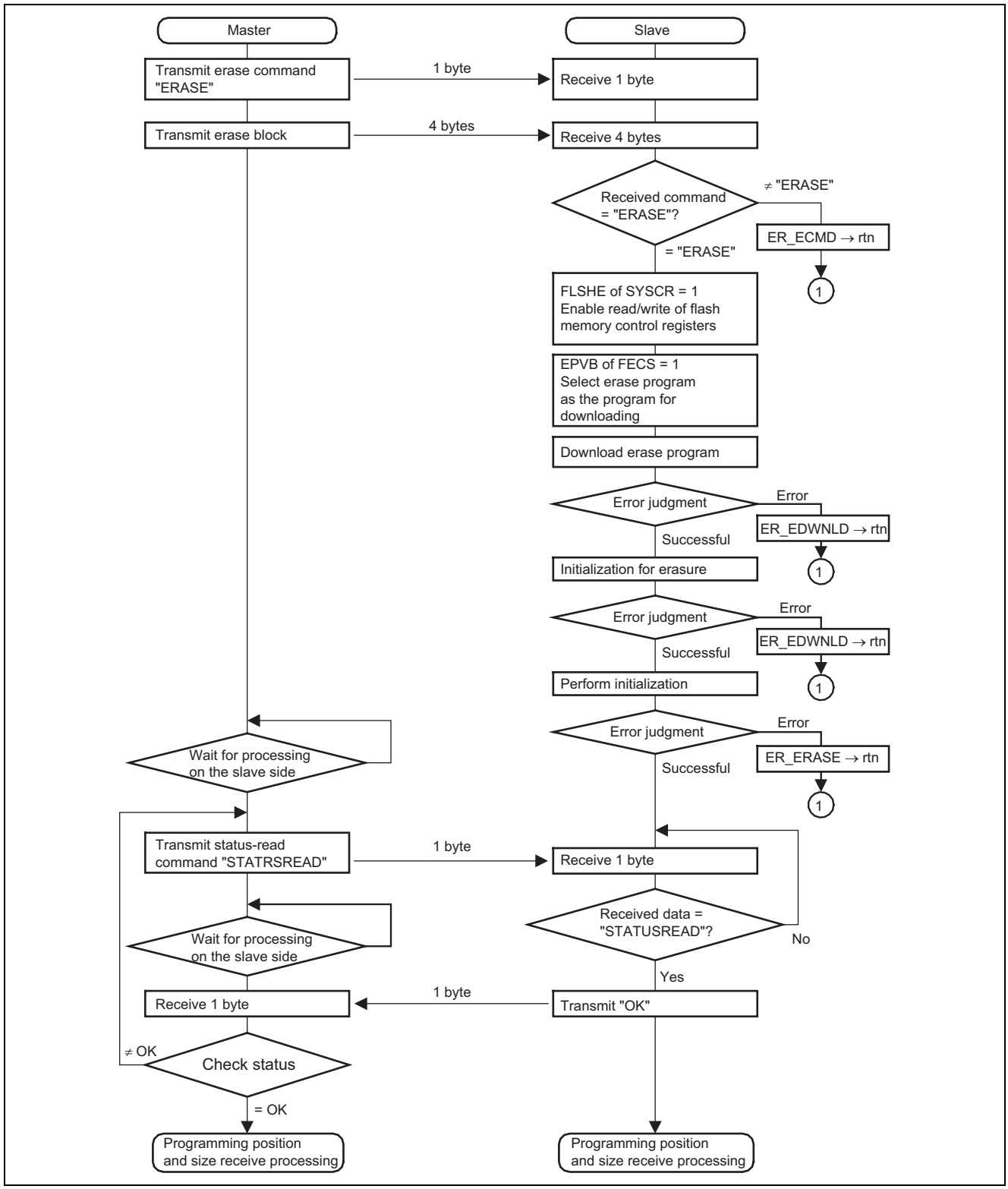


Figure 14 Erasure Processing

4.3.3 Processing to Receive the Position and Range for Programming

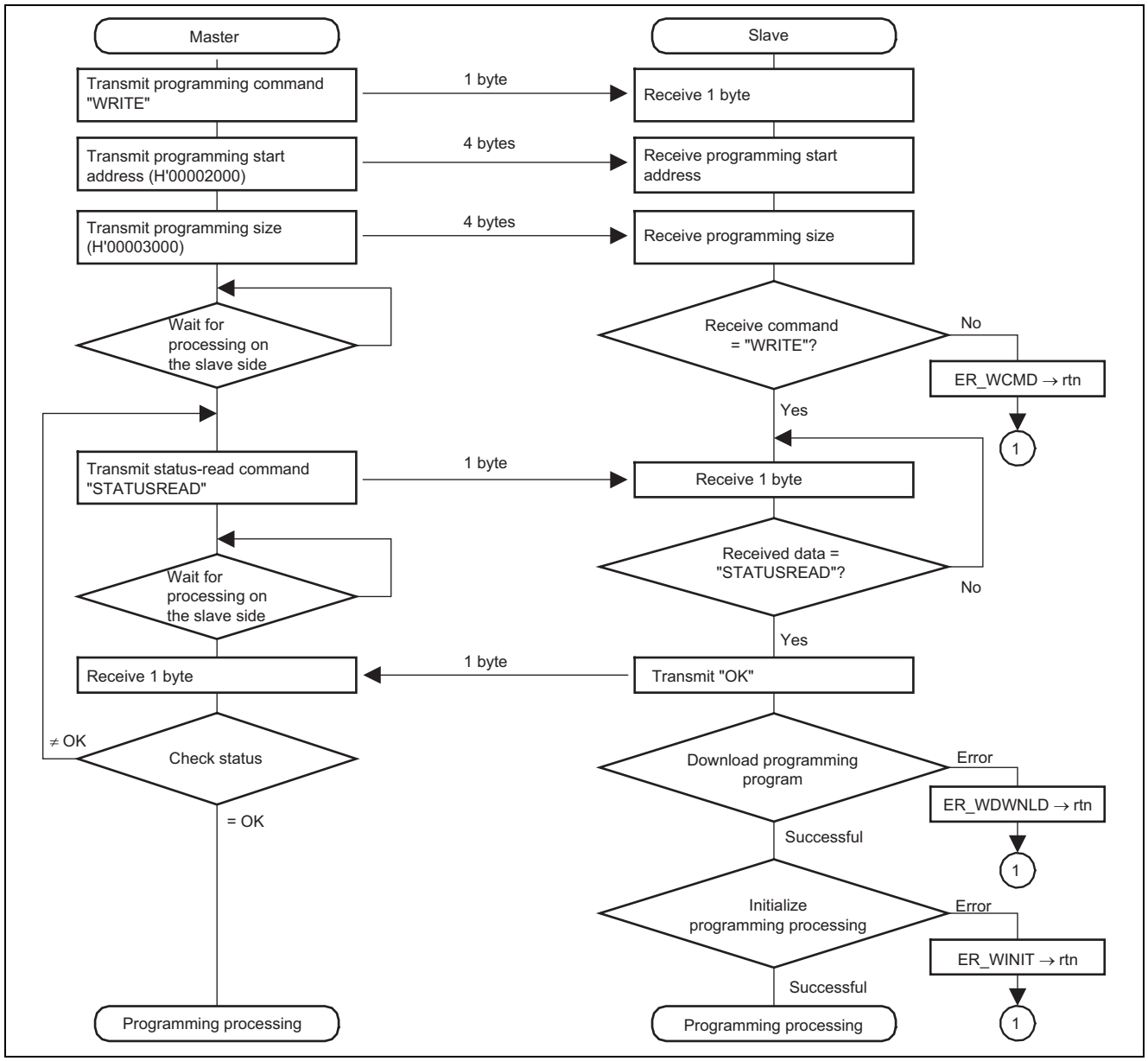


Figure 15 Processing to Receive the Position and Range for Programming

4.3.4 Programming Processing

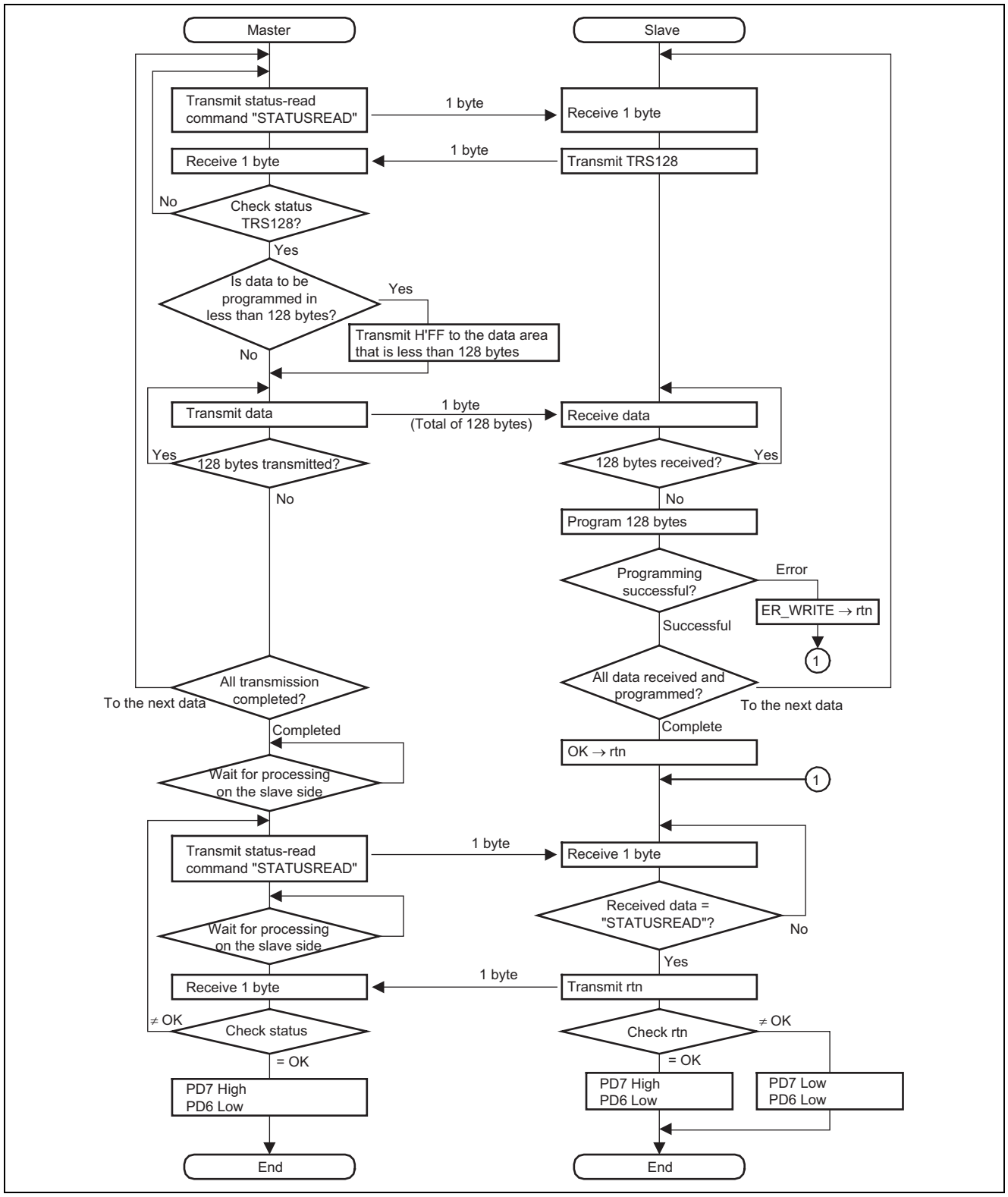


Figure 16 Programming Processing

5. Description of Software for Normal Program on the Receive Side (Slave)

5.1 List of Functions

The normal program (main.c) on the receive side (slave) is used to execute the user application program (normal application), receive the reprogramming start command, and transfer the programming/erasing procedure program to the on-chip RAM. A list of functions used in the normal program on the receive side (slave) is given in table 10, and the hierarchical structure of calls is given in figure 17.

Table 10 Functions in the Normal Program on the Receive Side (Slave)

Function Name	Description
init	Initialization routine. Releases from the module stop mode, makes clock settings, and calls the main function.
main	Main routine. Executes the normal application program, receives the reprogramming start command, and transfers the programming/erasing procedure program to the on-chip RAM.
copyfzram	Transfers the programming/erasing procedure program from the user MAT to the on-chip RAM
flew_main	Programming/erasing procedure program in the user MAT.

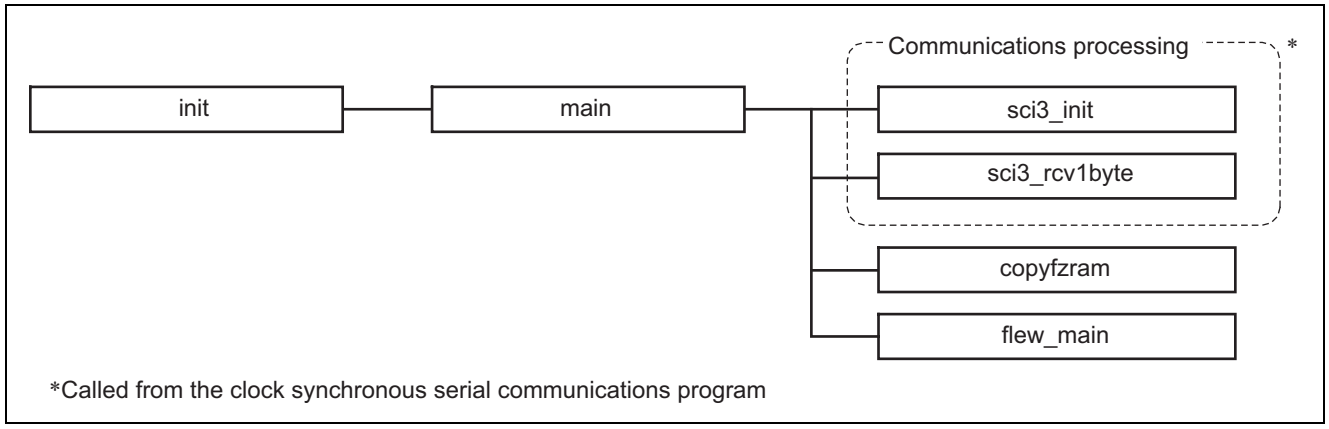


Figure 17 Normal Program on the Slave Side

5.2 Description of Functions

5.2.1 init Function

1. Overview
   Initialization routine, releases the module stop mode, sets the clock, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **System Clock Control Register (SCKCR) Address: H'FFFDC4**

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System clock (Iϕ) select
9	ICK1	0	R/W	Selects the frequency of the CPU, DMAC, DTC module and system clock.
8	ICK0	0	R/W	000: Input clock x 8
6	PCK2	0	R/W	Peripheral module clock (Pϕ) select
5	PCK1	0	R/W	Selects the frequency of peripheral module clock.
4	PCK0	1	R/W	001: Input clock x 4
2	BCK2	0	R/W	External bus clock (Bϕ) select
1	BCK1	0	R/W	Selects the frequency of external bus clock.
0	BCK0	1	R/W	001: Input clock x 4

- The MSTPCRA, MSTPCRB, and MSTPCRC registers control module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode, while clearing the bit to 0 clears the module stop mode.

- **Module Stop Control Register A (MSTPCRA) Address: H'FFFDC8**

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current drawn by stopping the bus controller and I/O port operations when the CPU executes the SLEEP instruction after the module stop mode has been set for all the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
4	MSTPA4	1	R/W	A/D converter unit 1
3	MSTPA3	1	R/W	A/D converter unit 0
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

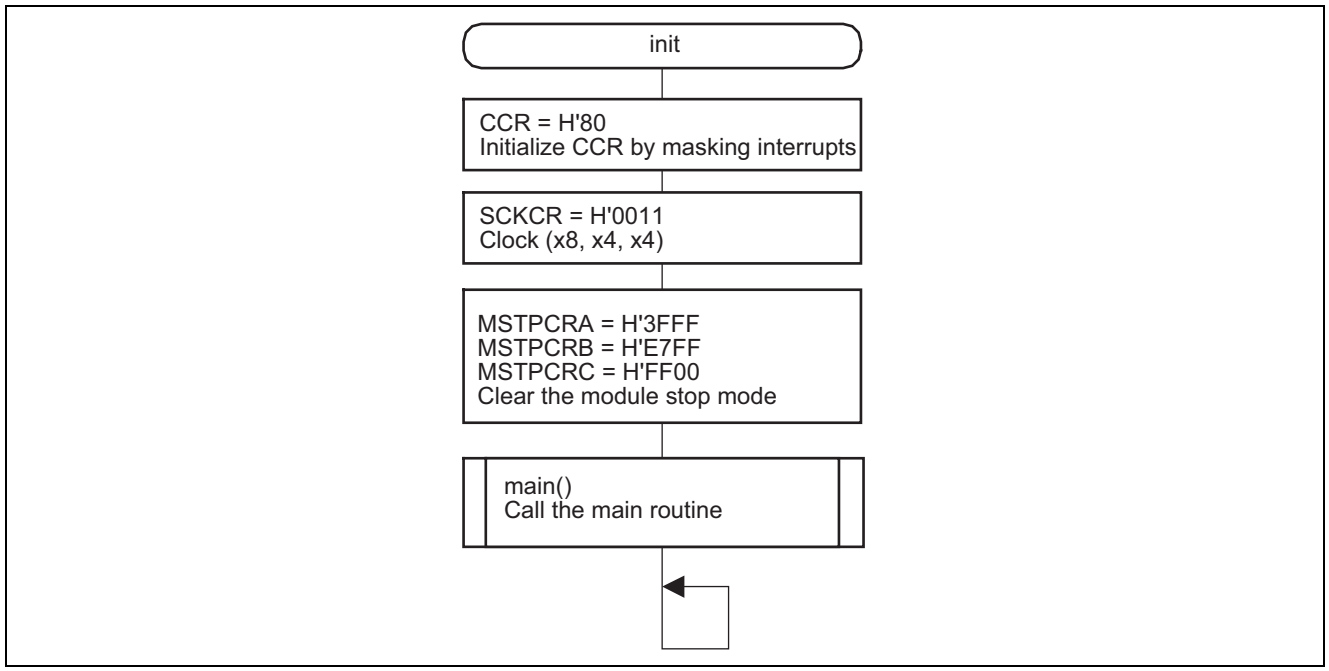
- **Module Stop Control Register B (MSTPCRB) Address: H'FFFDCA**

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable Pulse Generator (PPG)
12	MSTPB12	0	R/W	Serial Communication Interface_4 (SCI_4)
11	MSTPB11	0	R/W	Serial Communication Interface_3 (SCI_3)

- **Module Stop Control Register C (MSTPCRC) Address: H'FFFDCC**

Bit	Bit Name	Setting	R/W	Description
10	MSTPC10	1	R/W	Synchronous serial communications unit 2 (SSU_2)
9	MSTPC9	1	R/W	Synchronous serial communications unit 1 (SSU_1)
8	MSTPC8	1	R/W	Synchronous serial communications unit 0 (SSU_0)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF9000 to H'FFBFFF)
0	MSTPC0	0	R/W	Write a value so that MSTPC1 is always the same value as MSTPC0.

5. Flowchart



5.2.2 main Function

1. Overview
   - Executes the user application program (normal application)
   - Receives the reprogramming start command
   - Branches to programming/erasing procedure program

2. Arguments
   None

3. Return values
   None

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

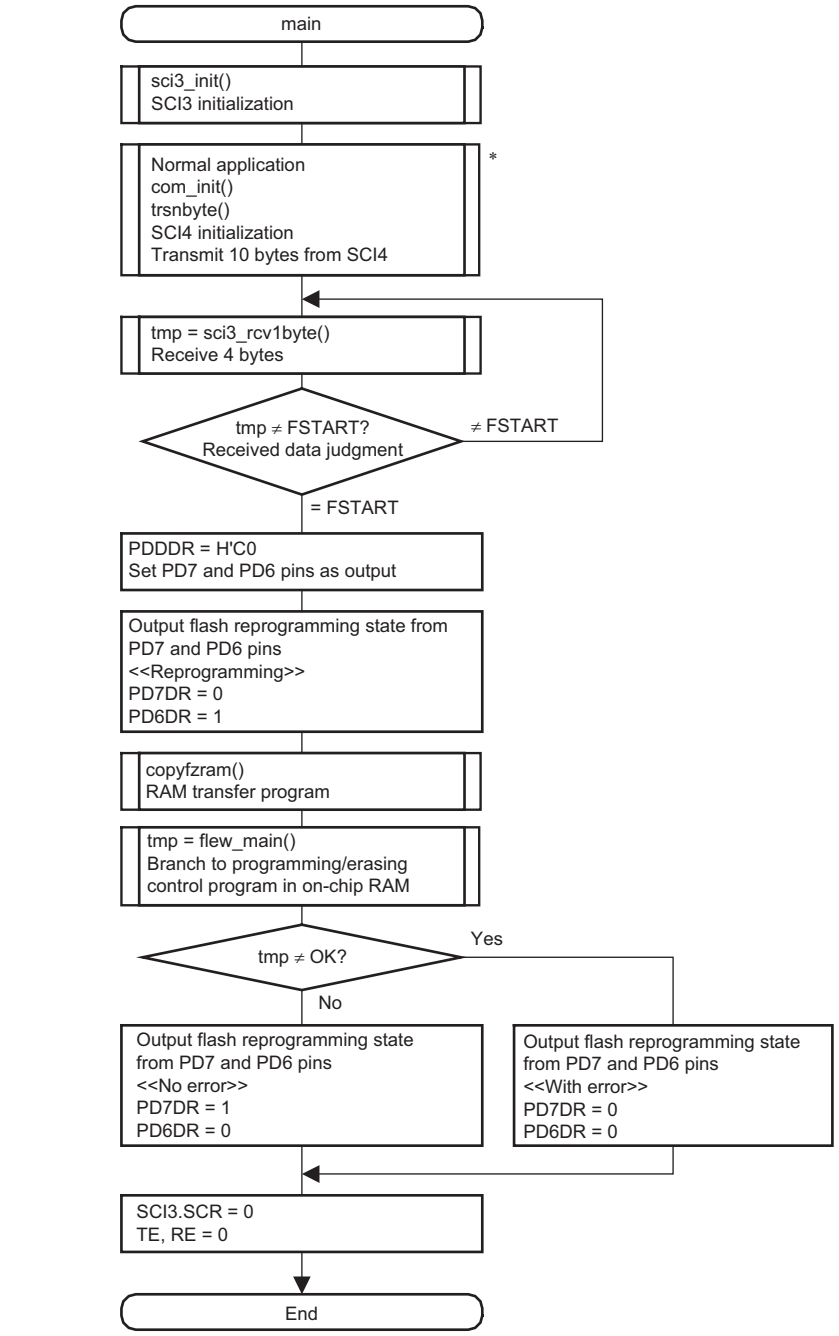
- **Port D Data Direction Register (PDDDR) Address: H'FFFB8C**

Bit	Bit Name	Setting	R/W	Description
7	PD7DDR	1	R/W	0: Set the PD7 pin to input 1: Set the PD7 pin to output
6	PD6DDR	1	R/W	0: Set the PD6 pin to input 1: Set the PD6 pin to output

- **Port D Data Register (PDDR) Address: H'FFFF5C**
  In this sample task, the PD7 and PD6 pins are used for output pins of flash reprogramming.

Bit	Bit Name	Setting	R/W	Description
7	PD7DR	Undefined	R/W	0: PD7 pin is driven low 1: PD7 pin is driven high
6	PD6DR	Undefined	R/W	0: PD6 pin is driven low 1: PD6 pin is driven high

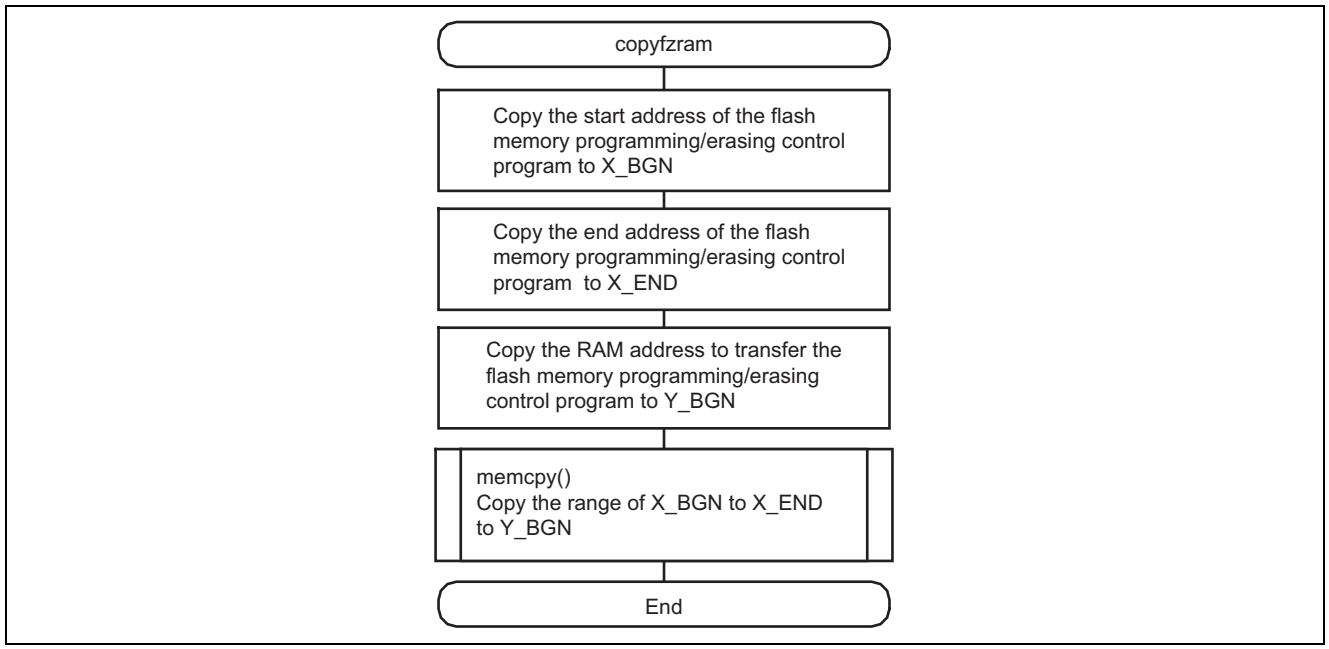
5. Flowchart



*Normal application is a sample program that has nothing to do with the user MAT reprogramming.
In this sample task, it is set to one point above.

5.2.3 copyfzram Function

1. Overview
   Transfers the programming/erasing procedure program to the on-chip RAM.
2. Arguments
   None
3. Return values
   None
4. Internal registers used
   None
5. Flowchart



5.2.4 flew_main Function

1. Overview
   Calls the main routine of the programming/erasing procedure program.

6. Description of Software for Programming/Erasing Procedure Program on the Slave Side

6.1 List of Functions

Programming/erasing procedure program (fwrite.c) performs erasing in erase block units, receives flash memory programming data, and performs programming to flash memory. A list of functions for the routines used in the programming/erasing procedure program is given in table 11. The hierarchical structure is shown in figure 18.

Table 11 List of Functions for Programming/Erasing Procedure Program

Function Name	Description
flew_main	Main processing of flash memory erasing/programming
erase_process	Erases flash memory
write_process	Programs flash memory
download	Downloads on-chip modules
fw_init	Initialization before flash memory erasing and programming

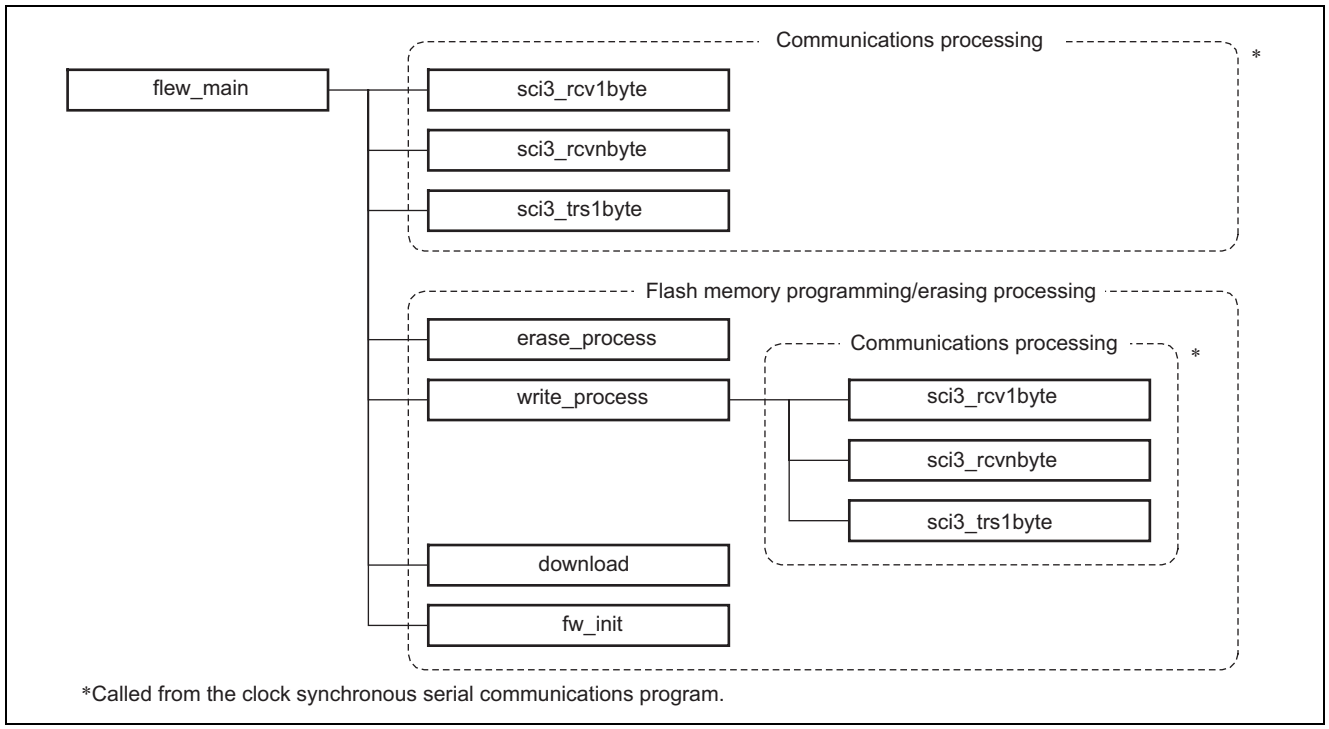


Figure 18 Programming/Erasing Procedure Program

6.2 Description of Modules

6.2.1 flew_main Function

1. Overview
   Main processing of flash memory erasing/programming.

2. Arguments
   None

3. Return value

Type	Description
unsigned char	Error status

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **System Control Register (SYSCR) Address: H'FFFDC2**

Bit	Bit Name	Setting	R/W	Description
7	FLSHE	1	R/W	Flash Memory Control Register Enable Controls accesses by the CPU to the flash memory control registers. Setting this bit to 1 enables read from/write to the flash memory control registers. Clearing this bit to 0 disables the flash memory control registers. At this time, the contents of the flash memory control registers are retained. 0: Disables the flash memory control registers 1: Enables the flash memory control registers

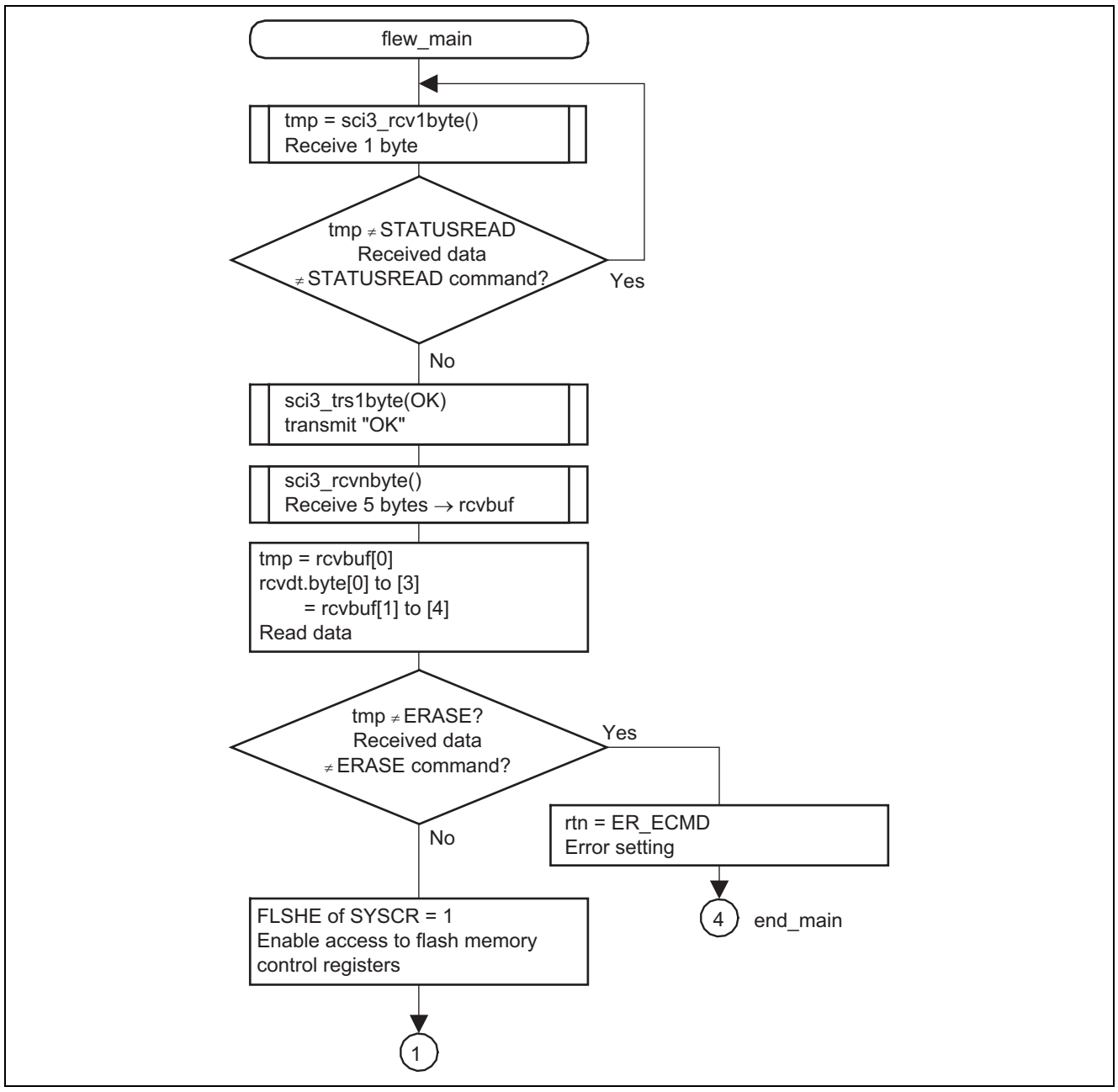
- **Flash Program Code Select Register (FPCS) Address: H'FFFDE9**

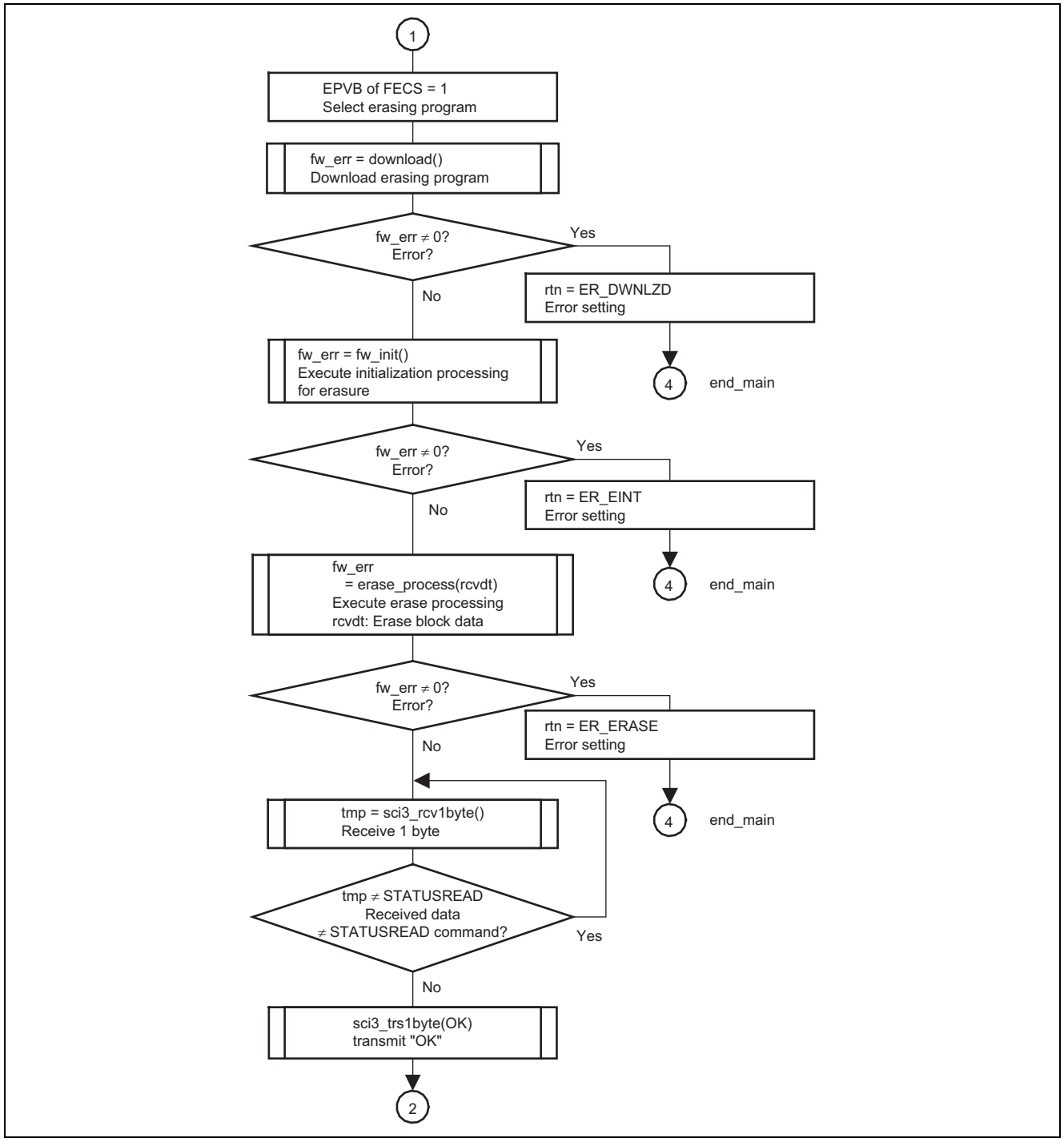
Bit	Bit Name	Setting	R/W	Description
0	PPVS	1	R/W	Program Pulse Verify Selects the programming program to be downloaded. 0: Programming program is not selected [Clearing condition] • When transfer is completed 1: Programming program is selected.

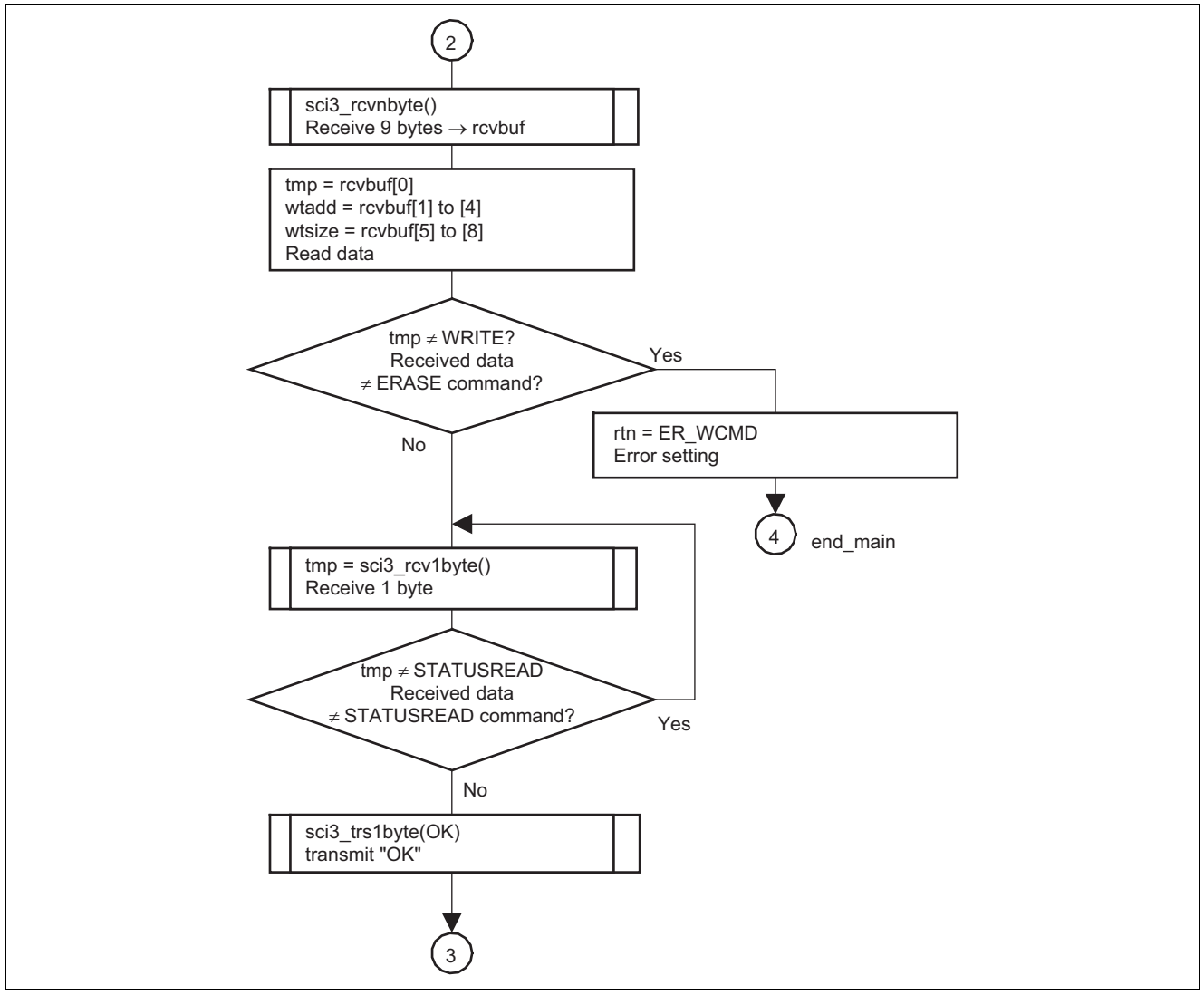
- **Flash Erase Code Select Register (FECS) Address: H'FFFDEA**

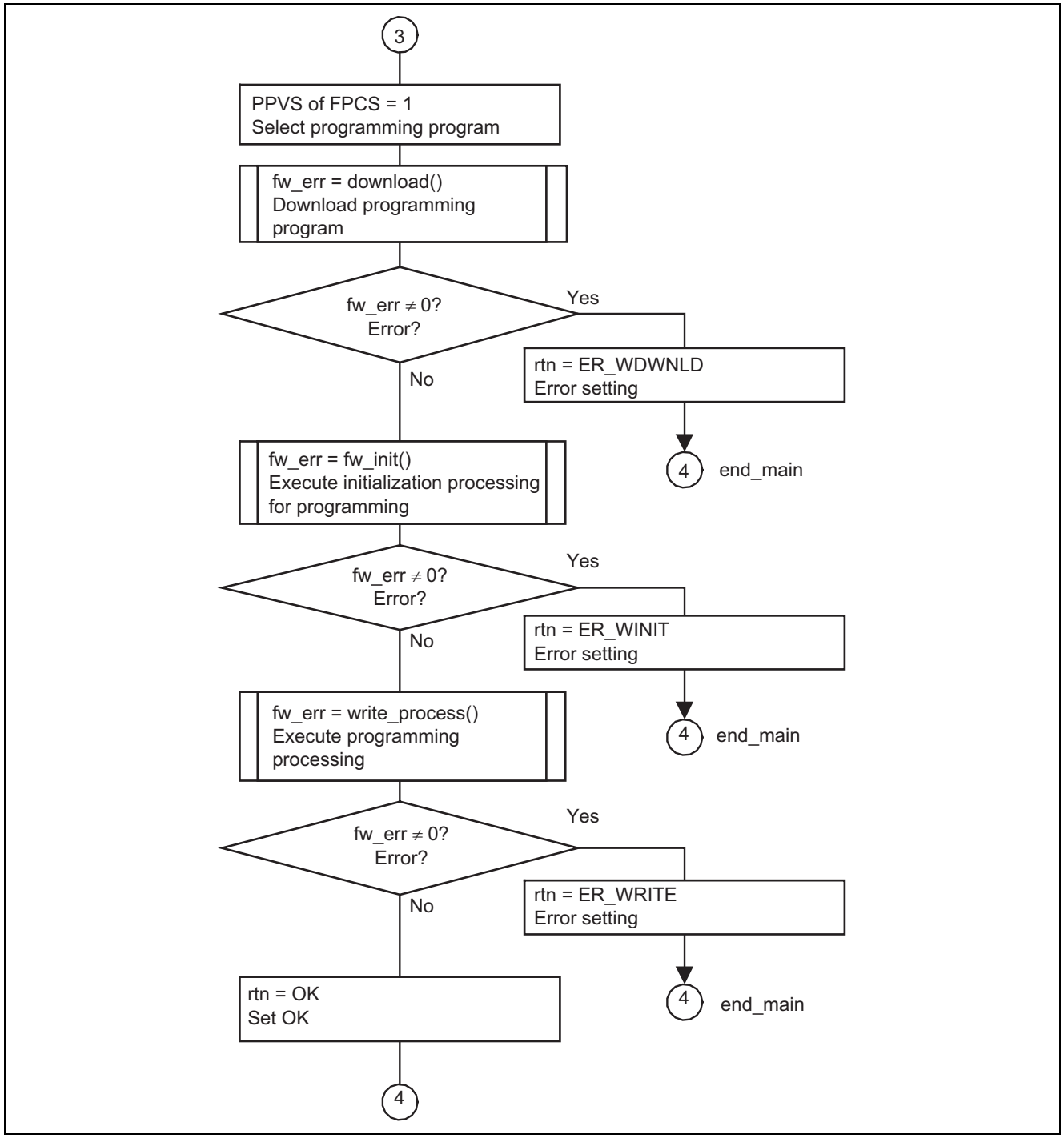
Bit	Bit Name	Setting	R/W	Description
0	EPVB	1	R/W	Erase Pulse Verify Block Selects the erasing program to be downloaded. 0: Erasing program is not selected [Clearing condition] • When transfer is completed 1: Erasing program is selected.

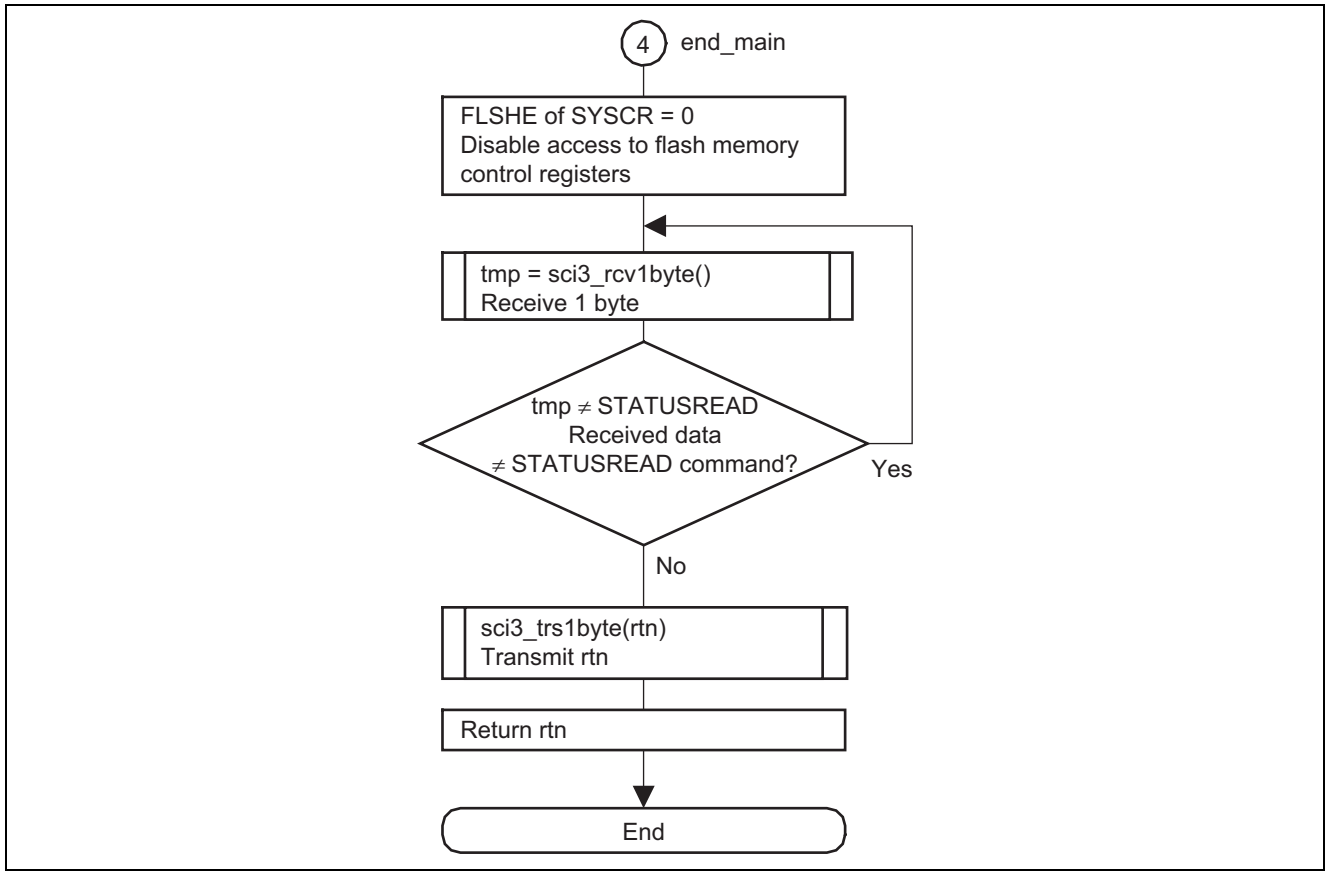
5. Flowchart


flew_main
tmp = sci3_rcv1byte()
Receive 1 byte
tmp ≠ STATUSREAD
Received data
≠ STATUSREAD command?
Yes
No
sci3_trs1byte(OK)
transmit "OK"
sci3_rcvnbyte()
Receive 5 bytes → rcvbuf
tmp = rcvbuf[0]
rcvdt.byte[0] to [3]
= rcvbuf[1] to [4]
Read data
tmp ≠ ERASE?
Received data
≠ ERASE command?
Yes
No
rtn = ER_ECMD
Error setting
4
end_main
FLSHE of SYSCR = 1
Enable access to flash memory
control registers
1


1
EPVB of FECS = 1
Select erasing program
fw_err = download()
Download erasing program
fw_err ≠ 0?
Error?
Yes
No
rtn = ER_DWNLZD
Error setting
4
end_main
fw_err = fw_init()
Execute initialization processing
for erasure
fw_err ≠ 0?
Error?
Yes
No
rtn = ER_EINT
Error setting
4
end_main
fw_err
= erase_process(rcvdt)
Execute erase processing
rcvdt: Erase block data
fw_err ≠ 0?
Error?
Yes
No
rtn = ER_ERASE
Error setting
4
end_main
tmp = sci3_rcv1byte()
Receive 1 byte
tmp ≠ STATUSREAD
Received data
≠ STATUSREAD command?
Yes
No
sci3_trs1byte(OK)
transmit "OK"
2


2
sci3_rcvnbyte()
Receive 9 bytes → rcvbuf
tmp = rcvbuf[0]
wtadd = rcvbuf[1] to [4]
wtsize = rcvbuf[5] to [8]
Read data
tmp ≠ WRITE?
Received data
≠ ERASE command?
Yes
No
rtn = ER_WCMD
Error setting
4
end_main
tmp = sci3_rcv1byte()
Receive 1 byte
tmp ≠ STATUSREAD
Received data
≠ STATUSREAD command?
Yes
No
sci3_trs1byte(OK)
transmit "OK"
3


3
PPVS of FPCS = 1
Select programming program
fw_err = download()
Download programming program
fw_err ≠ 0?
Error?
Yes
No
rtn = ER_WDWNLD
Error setting
4
end_main
fw_err = fw_init()
Execute initialization processing for programming
fw_err ≠ 0?
Error?
Yes
No
rtn = ER_WINIT
Error setting
4
end_main
fw_err = write_process()
Execute programming processing
fw_err ≠ 0?
Error?
Yes
No
rtn = ER_WRITE
Error setting
4
end_main
rtn = OK
Set OK
4


4
end_main
FLSHE of SYSCR = 0
Disable access to flash memory
control registers
tmp = sci3_rcv1byte()
Receive 1 byte
tmp ≠ STATUSREAD
Received data
≠ STATUSREAD command?
Yes
No
sci3_trs1byte(rtn)
Transmit rtn
Return rtn
End

6.2.2 erase_process Function

1. Overview
   Erases flash memory.

2. Arguments

Type	Variable Name	Description
unsigned char	ERASEBLK	Erases block

3. Return value

Type	Description
unsigned char	Flash pass and fail parameter (FPFR). Return value of the erase result.

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **Flash Key Code Register (FKEY) Address: H'FFFDEC**

Bit	Bit Name	Setting	R/W	Description
7	K7	0	R/W	Key Code
6	K6	1	R/W	When H'A5 is written to FKEY, writing to the SCO bit in FCCS is enabled. When a value other than H'A5 is written, the SCO bit cannot be set to 1. Therefore, the on-chip program cannot be downloaded to the on-chip RAM. Only when H'5A is written can programming/erasing of the flash memory be executed. When a value other than H'5A is written, even if the programming/erasing program is executed, programming/erasing cannot be performed. H'A5: Writing to the SCO bit is enabled. (The SCO bit cannot be set to 1 when FKEY is a value other than H'A5.) H'5A: Programming/erasing of the flash memory is enabled. (When FKEY is a value other than H'5A, the software protection state is entered.) H'00: Initial value
5	K5	0	R/W	
4	K4	1	R/W	
3	K3	1	R/W	
2	K2	0	R/W	
1	K1	1	R/W	
0	K0	0	R/W	

- **Flash Pass and Fail Parameter (FPFR) CPU General Register R0L**

  Return value of the erase results

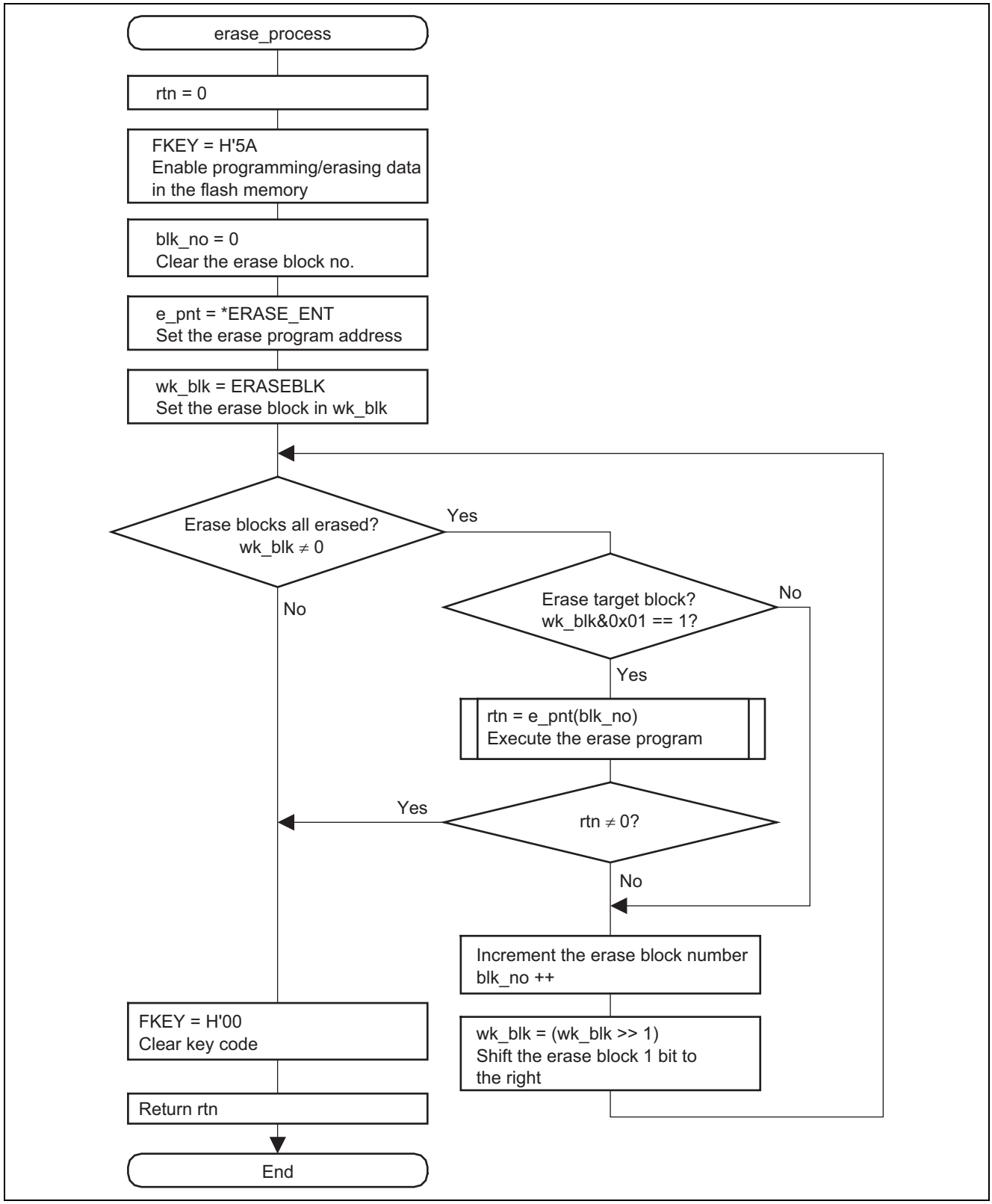
Bit	Bit Name	Setting	R/W	Description
6	MD	Undefined	R/W	Erasing Mode Related Setting Error Detect Detects the error protection state and returns the result. When the error protection state is entered, this bit is set to 1. Whether the error protection state is entered or not can be confirmed with the FLER bit of the FCCS register. 0: Normal operation (FLER = 0) 1: Error protection state, and programming cannot be performed (FLER = 1)
5	EE	Undefined	R/W	Erasing Execution Error Detect Writes 1 to this bit when the specified data could not be written because the user MAT was not erased. If this bit is set to 1, there is a high possibility that the user MAT has been written partially. In this case, after removing the error factor, erase the user MAT. 0: Erasure has ended normally 1: Erasure has ended abnormally
4	FK	Undefined	R/W	Flash Key Register Error Detect Checks the FKEY value (H'A5) before programming starts, and returns the results. 0: FKEY setting is normal (H'5A) 1: FKEY setting is abnormal (a value other than H'5A)
3	EB	Undefined	R/W	Erase Block Selection Error Detect Checks whether the specified erase block number is in the block range of user MAT and returns the result. 0: Setting of erase block number is normal 1: Setting of erase block number is abnormal
0	SF	Undefined	R/W	Success/Fail Indicates the erasure results. 0: Erasure ended normally (no error) 1: Erasure ended abnormally (error occurred)

- **Flash Erase Block Select Parameter (FEBS) CPU General Register ER0**

  Sets the erase block number in the range from 0 to 11 (H'0000 to H'000B). Number 0 corresponds to block EB0 and number 11 corresponds to block EB11. An error occurs when a number other than 0 to 11 is set.

  Setting: blk_no

5. Flowchart


erase_process
rtn = 0
FKEY = H'5A
Enable programming/erasing data in the flash memory
blk_no = 0
Clear the erase block no.
e_pnt = *ERASE_ENT
Set the erase program address
wk_blk = ERASEBLK
Set the erase block in wk_blk
Erase blocks all erased?
wk_blk ≠ 0
Yes
No
Erase target block?
wk_blk&0x01 == 1?
No
Yes
rtn = e_pnt(blk_no)
Execute the erase program
rtn ≠ 0?
Yes
No
Increment the erase block number
blk_no ++
wk_blk = (wk_blk >> 1)
Shift the erase block 1 bit to the right
FKEY = H'00
Clear key code
Return rtn
End

6.2.3 write_process Function

1. Overview
   Programs flash memory.

2. Arguments

Type	Variable Name	Description
unsigned long	fladr	Reprogramming start address
unsigned long	flsize	Reprogramming size

3. Return value

Type	Description
unsigned char	Flash pass and fail parameter (FPFR). Return value of the programming result.

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **Flash Key Code Register (FKEY) Address: H'FFFDEC**

Bit	Bit Name	Setting	R/W	Description
7	K7	0	R/W	Key Code
6	K6	1	R/W	When H'A5 is written to FKEY, writing to the SCO bit in FCCS is enabled. When a value other than H'A5 is written, the SCO bit cannot be set to 1. Therefore, the on-chip program cannot be downloaded to the on-chip RAM. Only when H'5A is written can programming/erasing of the flash memory be executed. When a value other than H'5A is written, even if the programming/erasing program is executed, programming/erasing cannot be performed. H'A5: Writing to the SCO bit is enabled. (The SCO bit cannot be set to 1 when FKEY is a value other than H'A5.) H'5A: Programming/erasing of the flash memory is enabled. (When FKEY is a value other than H'5A, the software protection state is entered.) H'00: Initial value
5	K5	0	R/W	
4	K4	1	R/W	
3	K3	1	R/W	
2	K2	0	R/W	
1	K1	1	R/W	
0	K0	0	R/W	

- **Flash Pass and Fail Parameter (FPFR) CPU General Register R0L**

  Return value of the program results

Bit	Bit Name	Setting	R/W	Description
6	MD	Undefined	R/W	Programming Mode Related Setting Error Detect Detects the error protection state and returns the result. When the error protection state is entered, this bit is set to 1. Whether the error protection state is entered or not can be confirmed with the FLER bit in FCCS. 0: Normal operation (FLER = 0) 1: Error protection state, and programming cannot be performed (FLER = 1)
5	EE	Undefined	R/W	Programming Execution Error Detect Writes 1 to this bit when the specified data could not be written because the user MAT was not erased. If this bit is set to 1, there is a high possibility that the user MAT has been written partially. In this case, after removing the error factor, erase the user MAT. 0: Programming has ended normally 1: Programming has ended abnormally
4	FK	Undefined	R/W	Flash Key Register Error Detect Checks the FKEY value (H'A5) before programming starts, and returns the results. 0: FKEY setting is normal (H'5A) 1: FKEY setting is abnormal (a value other than H'5A)
2	WD	Undefined	R/W	Write Data Address Detect When an address not in the flash memory area is specified as the start address of the storage destination for the program data, an error occurs. 0: Setting of the start address of the storage destination for the program data is normal 1: Setting of the start address of the storage destination for the program data is abnormal
1	WA	Undefined	R/W	Write Address Error Detect When the following items are specified as the start address of the programming destination, an error occurs. • An area other than flash memory • The specified address is not aligned with the 128-byte boundary (lower eight bits of the address are other than H'00 and H'80) 0: Setting of the start address of the programming destination is normal 1: Setting of the start address of the programming destination is abnormal
0	SF	Undefined	R/W	Success/Fail Indicates the program results. 0: Erasure ended normally (no error) 1: Erasure ended abnormally (error occurred)

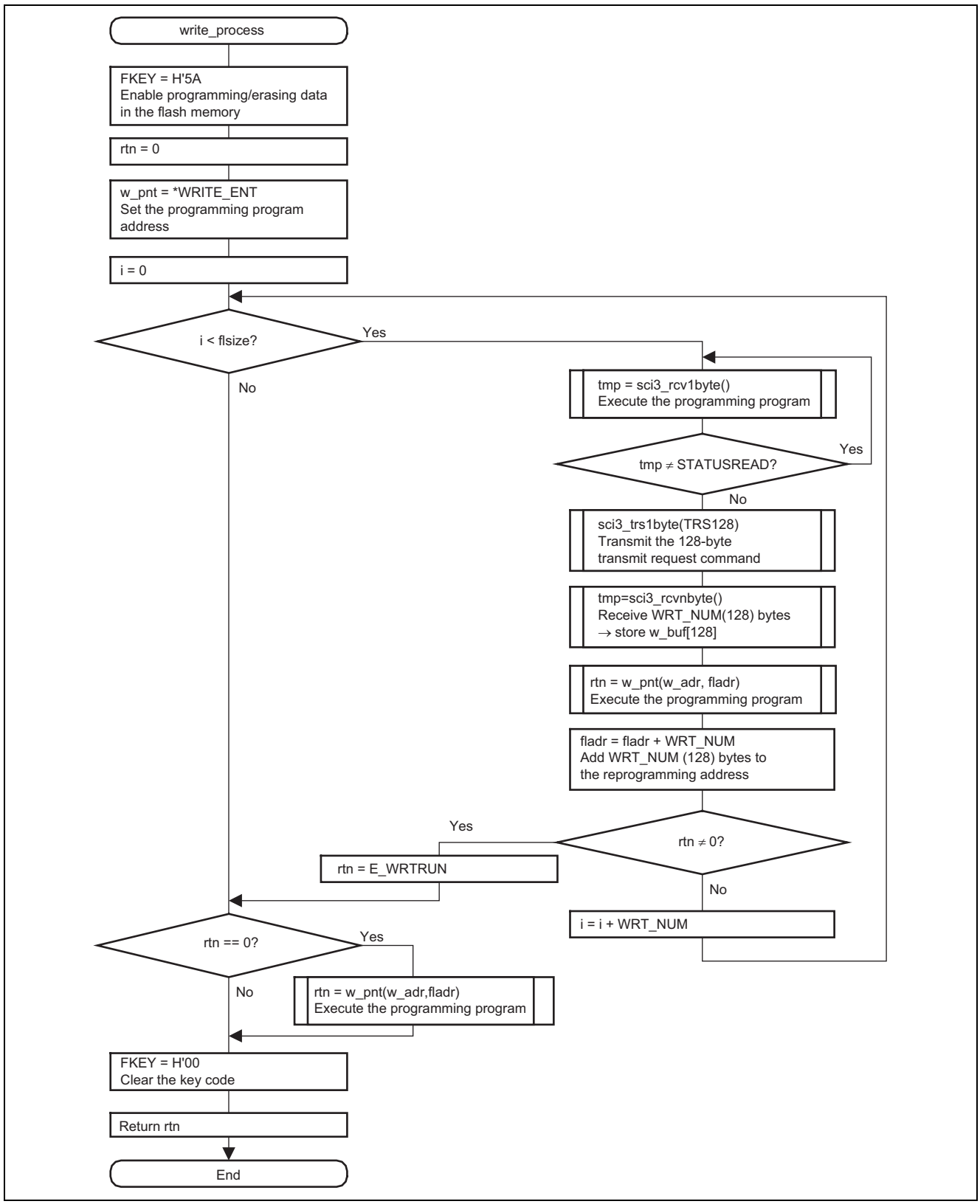
- **Flash Multipurpose Address Area Parameter (FMPAR) CPU General Register ER1**
  FMPAR sets the start address of the programming destination on the user MAT.
  When an address in an area other than the flash memory is set, or the start address of the programming destination is not aligned with the 128-byte boundary, an error occurs. The error occurrence is indicated by the WA bit of the FPFR register.

Bit	Bit Name	Setting	R/W	Description
31 to 0	MOA31 to MOA0	Fladr (local variable)	R/W	Sets the start address of the programming destination on the user MAT. Consecutive 128-byte programming is executed starting from the specified start address of the user MAT. Therefore, the specified start address of the programming destination becomes a 128-byte boundary, and MOA6 to MOA0 are always cleared to 0.

- **Flash Multipurpose Data Destination Parameter (FMPDR) CPU General Register ER0**
  FMPDR sets the start address in the area which stores the data to be programmed in the user MAT.
  When the storage destination for the program data is in flash memory, an error occurs. The error occurrence is indicated by the WD bit in FPFR.

Bit	Bit Name	Setting	R/W	Description
31 to 0	MOD31 to MOD0	Fladr (local variable)	R/W	Sets the start address of the area which stores the program data for the user MAT. Consecutive 128-byte data is programmed to the user MAT starting from the specified start address.

5. Flowchart


write_process
FKEY = H'5A
Enable programming/erasing data in the flash memory
rtn = 0
w_pnt = *WRITE_ENT
Set the programming program address
i = 0
i < flsize?
Yes
No
tmp = sci3_rcv1byte()
Execute the programming program
tmp ≠ STATUSREAD?
Yes
No
sci3_trs1byte(TRS128)
Transmit the 128-byte transmit request command
tmp=sci3_rcvnbyte()
Receive WRT_NUM(128) bytes
→ store w_buf[128]
rtn = w_pnt(w_adr, fladr)
Execute the programming program
fladr = fladr + WRT_NUM
Add WRT_NUM (128) bytes to the reprogramming address
rtn ≠ 0?
Yes
rtn = E_WRTRUN
No
i = i + WRT_NUM
rtn == 0?
Yes
No
rtn = w_pnt(w_adr,fladr)
Execute the programming program
FKEY = H'00
Clear the key code
Return rtn
End

6.2.4 download Function

1. Overview
   Downloads the on-chip modules.

2. Arguments
   None

3. Return value

Type	Description
unsigned char	Download pass and fail result arameter (DPFR). Return value of the download result.

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **Flash Key Code Register (FKEY) Address: H'FFFDEC**

Bit	Bit Name	Setting	R/W	Description
7	K7	1	R/W	Key Code
6	K6	0	R/W	When H'A5 is written to FKEY, writing to the SCO bit in FCCS is enabled. When a value other than H'A5 is written, the SCO bit cannot be set to 1. Therefore, the on-chip program cannot be downloaded to the on-chip RAM. Only when H'5A is written can programming/erasing of the flash memory be executed. When a value other than H'5A is written, even if the programming/erasing program is executed, programming/erasing cannot be performed. H'A5: Writing to the SCO bit is enabled. (The SCO bit cannot be set to 1 when FKEY is a value other than H'A5.) H'5A: Programming/erasing of the flash memory is enabled. (When FKEY is a value other than H'5A, the software protection state is entered.) H'00: Initial value
5	K5	1	R/W	
4	K4	0	R/W	
3	K3	0	R/W	
2	K2	1	R/W	
1	K1	0	R/W	
0	K0	1	R/W	

- **Flash Transfer Destination Address Register (FTDAR) Address: H'FFFDEE**

Bit	Bit Name	Setting	R/W	Description
7	TDER	0	R/W	Transfer Destination Address Setting Error This bit is set to 1 when an error has occurred in setting the start address specified by bits TDA6 to TDA0. A start address error is determined by whether the value set in bits TDA6 to TDA0 is within the range of H'00 to H'02 when download is executed by setting the SCO bit in FCCS to 1. Make sure that this bit is cleared to 0 before setting the SCO bit to 1 and the value specified by bits TDA6 to TDA0 should be within the range of H'00 to H'02. 0: The value specified by bits TDA6 to TDA0 is within the range. 1: The value specified by TDER and bits TDA6 to TDA0 is between H'03 and H'FF and download has stopped.
6	TDA6	0	R/W	Transfer Destination Address Specifies the on-chip RAM start address of the download destination. A value between H'00 and H'02, and up to 4 Kbytes can be specified as the start address of the on-chip RAM. H'00: H'FF9000 is specified as the start address. H'01: H'FFA000 is specified as the start address. H'02: H'FFB000 is specified as the start address. H'03 to H'7F: Setting prohibited. (Specifying a value from H'03 to H'7F sets the TDER bit to 1 and stops download of the on-chip program.)
5	TDA5	0	R/W	
4	TDA4	0	R/W	
3	TDA3	0	R/W	
2	TDA2	0	R/W	
1	TDA1	0	R/W	
0	TDA0	0	R/W	

- **Flash Code Control Status Register (FCCS) Address: H'FFFDE8**

Bit	Bit Name	Setting	R/W	Description
4	FLER	0	R	Flash Memory Error Indicates that an error has occurred during programming/erasing the flash memory. When this bit is set to 1, the flash memory enters the error protection state. When this bit is set to 1, high voltage is applied to the internal flash memory. To reduce the damage to the flash memory, the reset must be released after the reset input period (period of $\overline{RES}$ = 0) of at least 100 µs. 0: Flash memory operates normally (Error protection is invalid) [Clearing condition] • At a power-on reset 1: An error occurs during programming/erasing flash memory (Error protection is valid) [Setting conditions] • When an interrupt, such as NMI, occurs during programming/erasing. • When the flash memory is read during programming/erasing (including a vector read and an instruction fetch). • When the SLEEP instruction is executed during programming/erasing (including software standby mode). • When a bus master other than the CPU, such as the DTC and DMAC, obtains bus mastership during programming/erasing.
0	SCO	0	(R)/W*	Source Program Copy Operation Requests the on-chip programming/erasing program to be downloaded to the on-chip RAM. When this bit is set to 1, the on-chip program which is selected by FPCS or FECS is automatically downloaded in the on-chip RAM area specified by FTDAR. In order to set this bit to 1, the RAM emulation mode must be canceled, H'A5 must be written to FKEY, and the setting of SCO bit must be executed in the on-chip RAM. Dummy read of FCCS must be executed twice immediately after setting this bit to 1. All interrupts must be disabled during download. This bit is cleared to 0 when download is completed. During program download initiated with this bit, particular processing which accompanies bank switching of the program storage area is executed. Before a download request, initialize the VBR contents to H'00000000. After download is completed, the VBR contents can be changed. 0: Download of the programming/erasing program is not requested. [Clearing condition] • When download is completed 1: Download of the programming/erasing program is requested. [Setting conditions] (When all of the following conditions are satisfied) • Not in RAM emulation mode (the RAMS bit of RAMER is cleared to 0) • H'A5 is written to FKEY • Setting of SCO bit in FCCS is executed in the on-chip RAM

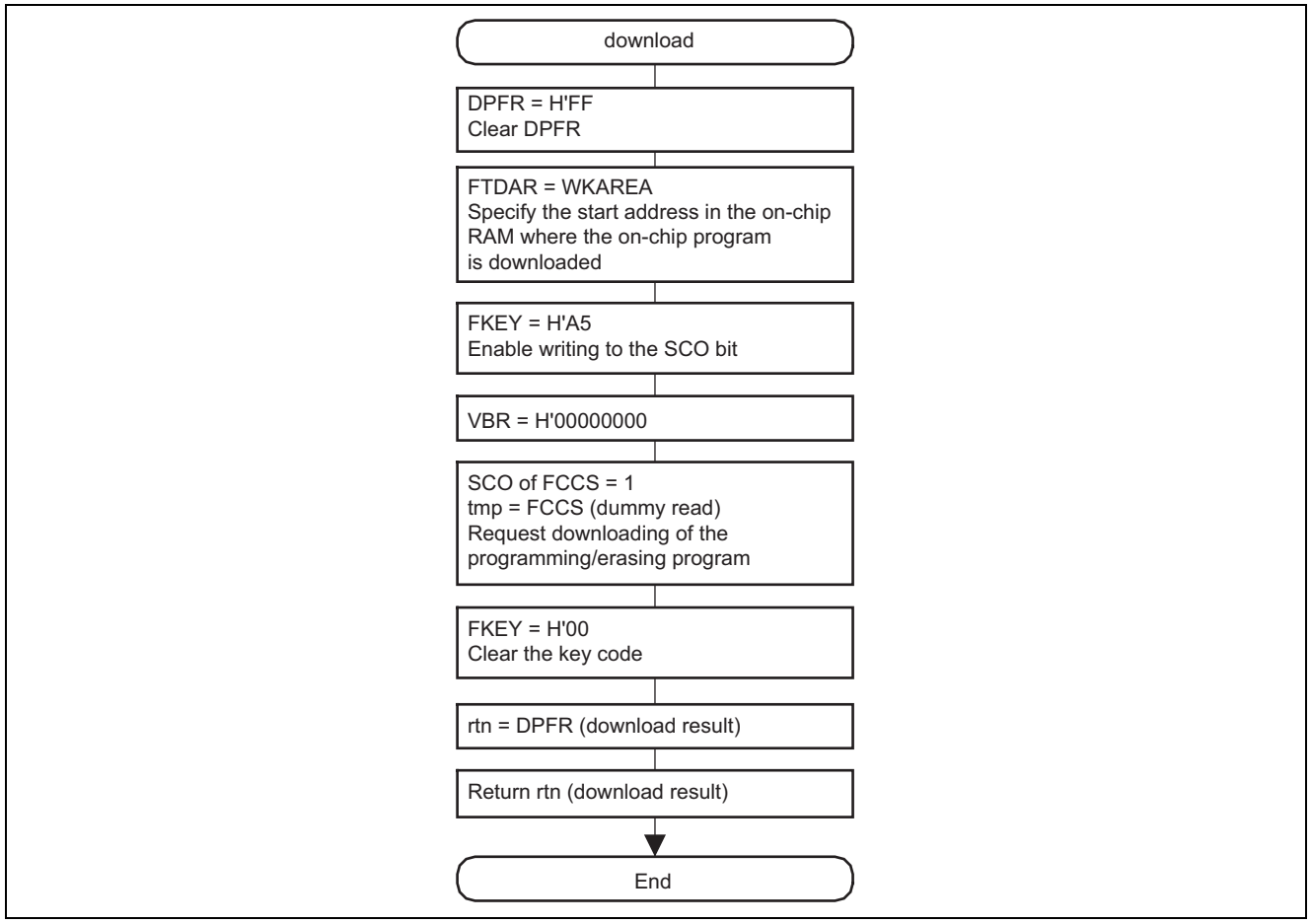
Note: * SCO is a write-only bit. This bit is always read as 0.

- **Download Pass and Fail Result Parameter (DPFR) Single Byte of Start Address in On-Chip RAM Specified by FTDAR**

  DPFR indicates the return value of the download result. The DPFR value is used to determine the download result.

Bit	Bit Name	Setting	R/W	Description
2	SS	1	R/W	Source Select Error Detect Only one type can be specified for the on-chip program which can be downloaded. When the program to be downloaded is not selected, more than two types of programs are selected, or a program which is not mapped is selected, an error occurs. 0: Download program selection is normal 1: Download program selection is abnormal
1	FK	1	R/W	Flash Key Register Error Detect Checks the FKEY value (H'A5) and returns the result. 0: FKEY setting is normal (H'A5) 1: FKEY setting is abnormal (value other than H'A5)
0	SF	1	R/W	Success/Fail Returns the download result. Reads back the program downloaded to the on-chip RAM and determines whether it has been transferred to the on-chip RAM. 0: Download of the program has ended normally 1: Download of the program has ended abnormally (error occurred)

5. Flowchart


download
DPFR = H'FF
Clear DPFR
FTDAR = WKAREA
Specify the start address in the on-chip RAM where the on-chip program is downloaded
FKEY = H'A5
Enable writing to the SCO bit
VBR = H'00000000
SCO of FCCS = 1
tmp = FCCS (dummy read)
Request downloading of the programming/erasing program
FKEY = H'00
Clear the key code
rtn = DPFR (download result)
Return rtn (download result)
End

6.2.5 fw_init Function

1. Overview
   Initializes flash memory before programming.

2. Arguments
   None

3. Return value

Type	Description
unsigned char	Flash pass and fail parameter (FPFR). Return value of the initialization result.

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

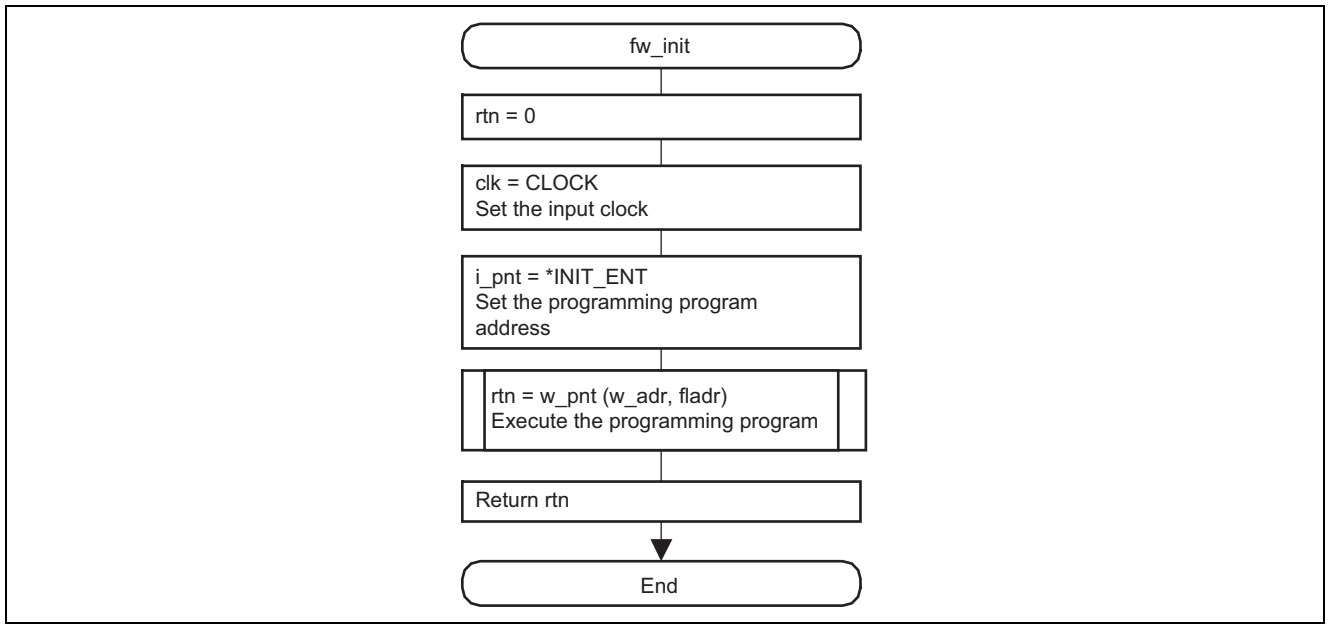
- **Flash Program/Erase Frequency Parameter (FPEFEQ) CPU General Register ER0**
  FPEFEQ sets the operating frequency of the CPU. The CPU operating frequency available in this LSI ranges from 8 MHz to 48 MHz.

Bit	Bit Name	Setting	R/W	Description
15 to 0	F15 to F0	CLOCK	R/W	Frequency Set Sets the operating frequency of the CPU. When the PLL multiplication function is used, set the multiplied frequency. The setting value must be calculated as follows: • The operating frequency shown in MHz units must be rounded in a number of three decimal places and be shown in a number of two decimal places. • The value multiplied by 100 is converted to the binary digit and is written to FPEFEQ (general register ER0). For example, when the operating frequency of the CPU is 35.000 MHz, the value is as follows: 1. The number of three decimal places of 35.000 is rounded. 2. The formula of 35.00 × 100 = 3500 is converted to the binary digit and B'0000 1101 1010 1100 (H'0CE4) is set to ER0.

- **Flash Pass and Fail Parameter (FPFR) CPU General Register R0L**
  Return value of the initialization results

Bit	Bit Name	Setting	R/W	Description
1	FQ	Undefined	R/W	Frequency Error Detect Compares the specified CPU operating frequency with the operating frequencies supported by this LSI, and returns the result. 0: Setting of operating frequency is normal 1: Setting of operating frequency is abnormal
0	SF	Undefined	R/W	Success/Fail Returns the initialization result. 0: Initialization has ended normally (no error) 1: Initialization has ended abnormally (error occurred)

5. Flowchart


fw_init
rtn = 0
clk = CLOCK
Set the input clock
i_pnt = *INIT_ENT
Set the programming program address
rtn = w_pnt (w_adr, fladr)
Execute the programming program
Return rtn
End

7. Description of Software for the Clock Synchronous Serial Communications Program on the Slave Side

7.1 List of Functions

The clock synchronous serial communications program (sci3.c) performs communications processing to the master side. Table 12 is a list of functions in the clock synchronous serial communications program, and figure 19 shows the hierarchy structure.

Table 12 Functions in the Clock Synchronous Serial Communication Program

Function Name	Description
sci3_init	Initializes clock synchronous serial communications
sci3_rcv1byte	Receives one byte of data
sci3_rcvnbyte	Receives n bytes of data
sci3_trs1byte	Transmits one byte of data
sci3_trsnbyte	Transmits n bytes of data

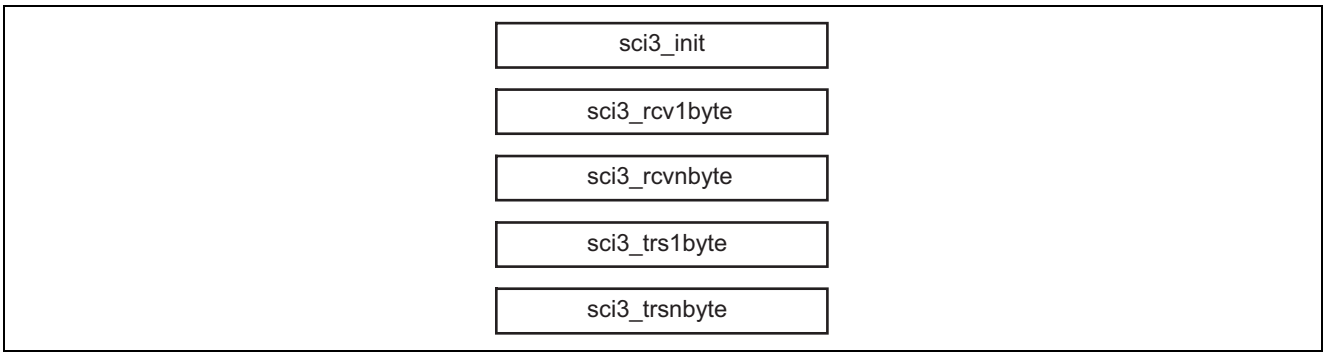


Figure 19 Clock Synchronous Serial Communications Program

7.2 Description of Modules

7.2.1 sci3_init Function

1. Overview
   Initializes clock synchronous serial communications.
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **Serial Mode Register_3 (SMR_3) Address: H'FFFE88**

Bit	Bit Name	Setting	R/W	Description
7	C/$\overline{A}$	0	R/W	Communications Mode 0: Asynchronous mode 1: Clocked synchronous mode
6	CHR	0	R/W	Character Length 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length.
1	CKS1	0	R/W	Clock Selection 1, 0
0	CKS0	0	R/W	B'00: Clock source of the on-chip baud rate generator is set to Pϕ clock.

- **Serial Control Register_3 (SCR_3) Address: H'FFFE8A**

Bit	Bit Name	Setting	R/W	Description
5	TE	0	R/W	Transmit Enable 0: Disables transmission 1: Enables transmission
4	RE	0	R/W	Receive Enable 0: Disables reception 1: Enables reception
1	CKE1	0	R/W	Clock Selection 1, 0
0	CKE0	0	R/W	In the clock synchronous mode: B'00: Internal clock is used for clock source, and SCK3 pin is set to clock output pin B'1X: External clock is used for clock source, and SCK3 pin is set to clock input pin

Legend
X: Don't care

- **Serial Status Register_3 (SSR_3) Address: H'FFFE8C**

Bit	Bit Name	Setting	R/W	Description
7	TDRE	1	R/(W)*	Transmit Data Register Empty 0: Transmit data written to TDR is not transferred to TSR 1: Transmit data is not written to TDR, or transmit data written to TDR is not transferred to TSR
6	RDRF	0	R/(W)*	Receive Data Register Full 0: No receive data is stored in RDR. 1: The receive data is stored in RDR.
5	ORER	0	R/(W)*	Overrun Error 0: No overrun error 1: Overrun error occurred during receive operation
2	TEND	Undefined	R	Transmit End 0: In transmission 1: Transmission completed

Note: * Only 0 can be written here, to clear the flags for TDRE, RDRF, and ORER.

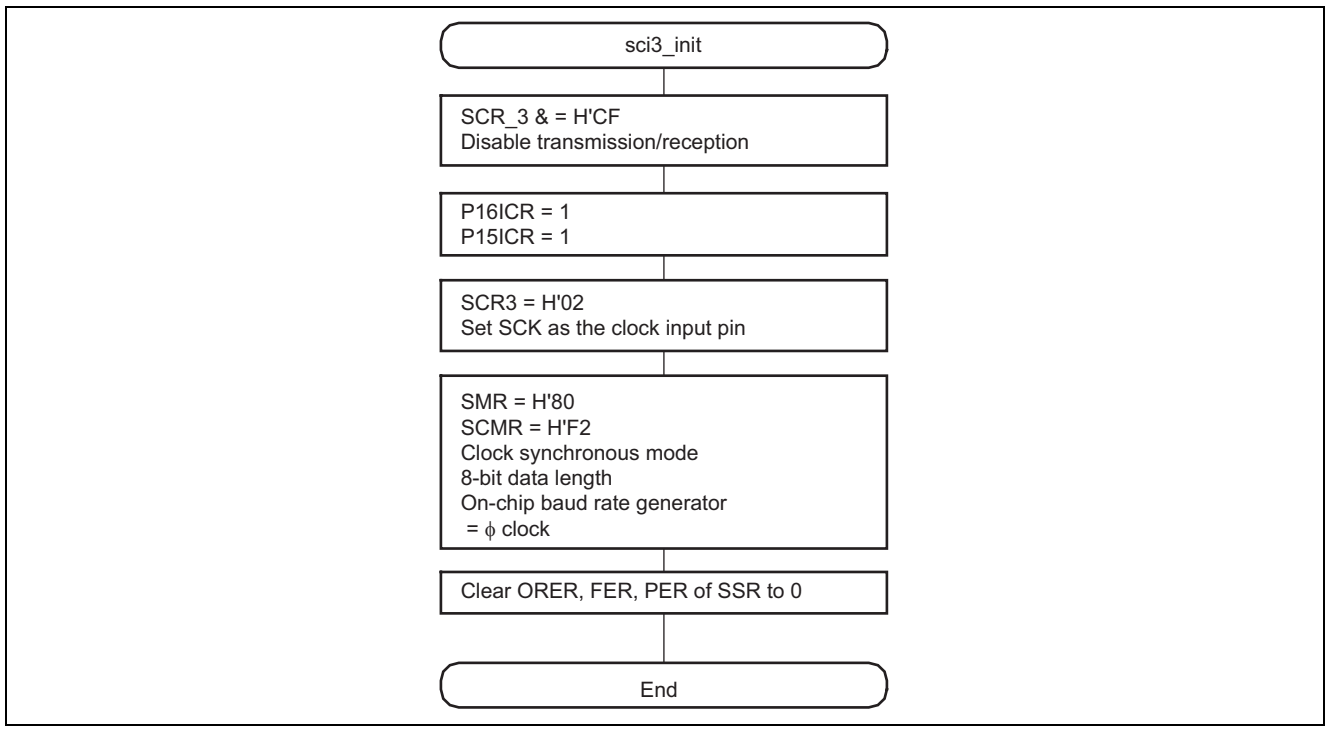
- **Port 1 Input Buffer Control Register (P1ICR) Address: H'FFFB90**

Bit	Bit Name	Setting	R/W	Description
6	P16ICR	1	R/W	0: Input buffer for P16 (SCK3) pin is disabled 1: Input buffer for P16 (SCK3) pin is enabled
5	P15ICR	1	R/W	0: Input buffer for P15 (RxD3) pin is disabled 1: Input buffer for P15 (RxD3) pin is enabled

- **Smart Card Mode Register_3 (SCMR_3) Address: H'FFFE8E**

Bit	Bit Name	Setting	R/W	Description
0	SMIF	0	R/W	Smart Card Interface Mode Select 0: Operates in normal asynchronous or clock synchronous mode 1: Operates in smart card interface mode

5. Flowchart


sci3_init
SCR_3 & = H'CF
Disable transmission/reception
P16ICR = 1
P15ICR = 1
SCR3 = H'02
Set SCK as the clock input pin
SMR = H'80
SCMR = H'F2
Clock synchronous mode
8-bit data length
On-chip baud rate generator
= ϕ clock
Clear ORER, FER, PER of SSR to 0
End

7.2.2 sci3_rcv1byte Function

1. Overview
   Receives one byte of clock synchronous serial data.
2. Arguments
   None
3. Return value

Type	Variable Name	Description
unsigned char	tmp	Receives one byte of data

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **Serial Control Register_3 (SCR_3) Address: H'FFFE8A**

Bit	Bit Name	Setting	R/W	Description
4	RE	0	R/W	Receive Enable 0: Disables reception 1: Enables reception

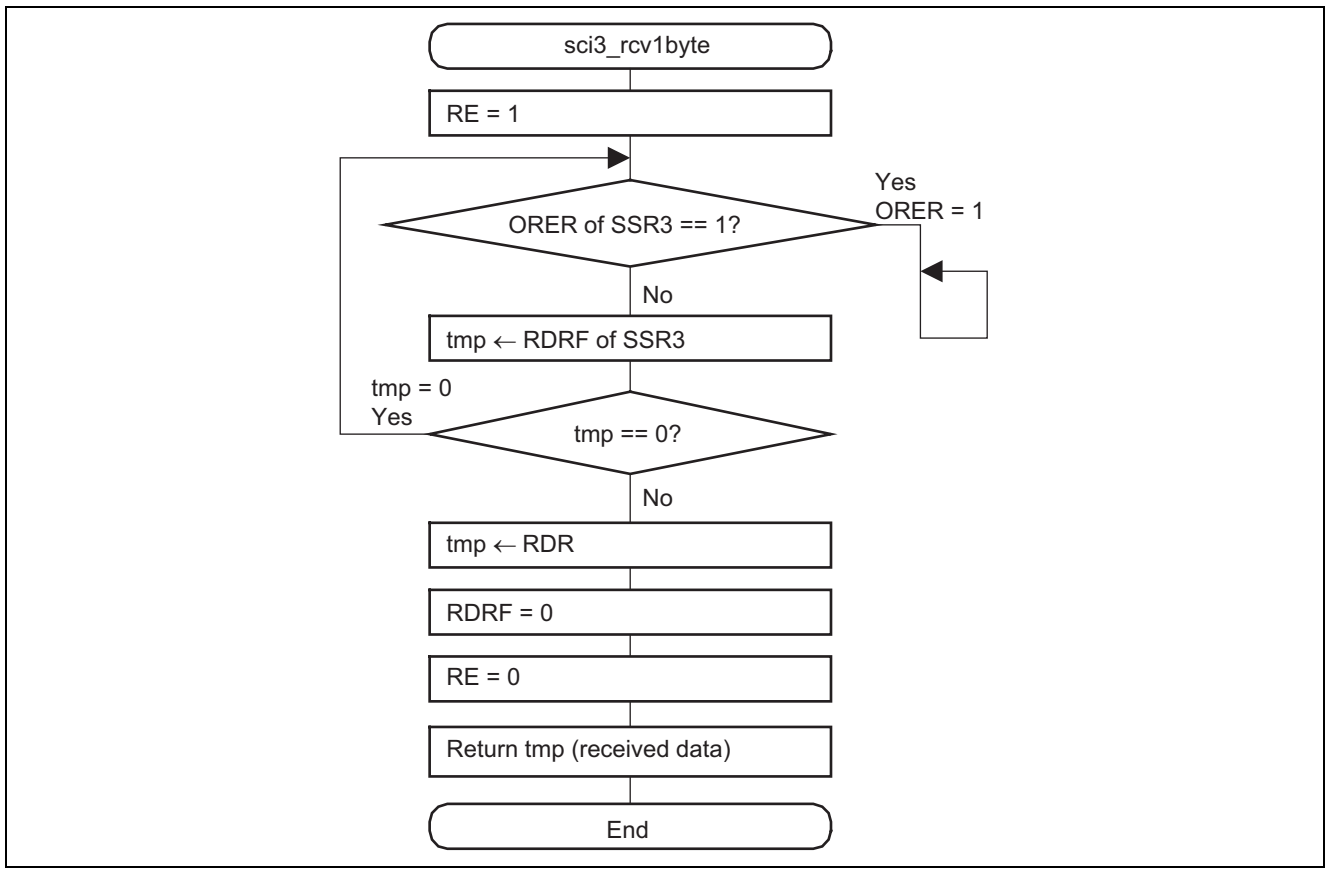
- **Serial Status Register_3 (SSR_3) Address: H'FFFE8C**

Bit	Bit Name	Setting	R/W	Description
6	RDRF	Undefined	R/W	Receive Data Register Full Indicates whether receive data is stored in RDR. [Setting condition] • When serial reception ends normally and receive data is transferred from RSR to RDR [Clearing conditions] • Writing of 0 to RDRF after having read RDRF = 1 • Generation of an RXI interrupt request allowing DMAC or DTC to read data from RDR. The RDRF flag is not affected and retains its previous value even though the RE bit in SCR is cleared to 0. Note that when the next reception is completed while the RDRF flag is being set to 1, an overrun error occurs and the received data are lost.
5	ORER	Undefined	R/W	Overrun Error [Setting condition] • Occurrence of an overrun error during reception [Clearing condition] • Writing of 0 to ORER after having read ORER = 1

Note: Only 0 can be written here, to clear the flags for RDRF and ORER.

- **Receive Data Register_3 (RDR_3) Address: H'FFFE8D**
  Function: An 8-bit register for storing receive data.
  Setting: Undefined

5. Flowchart


sci3_rcv1byte
RE = 1
ORER of SSR3 == 1?
Yes
ORER = 1
No
tmp ← RDRF of SSR3
tmp = 0
Yes
tmp == 0?
No
tmp ← RDR
RDRF = 0
RE = 0
Return tmp (received data)
End

7.2.3 sci3_rcvnbyte Function

1. Overview
   Receives n byte of clock synchronous serial data.

2. Arguments

Type	Variable Name	Description
unsigned char	dtno	No. of receive bytes
unsigned char	*ram	The start address of RAM in which the receive data is stored

3. Return value
   None

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **Serial Control Register_3 (SCR_3) Address: H'FFFE8A**

Bit	Bit Name	Setting	R/W	Description
4	RE	0	R/W	Receive Enable 0: Disables reception 1: Enables reception

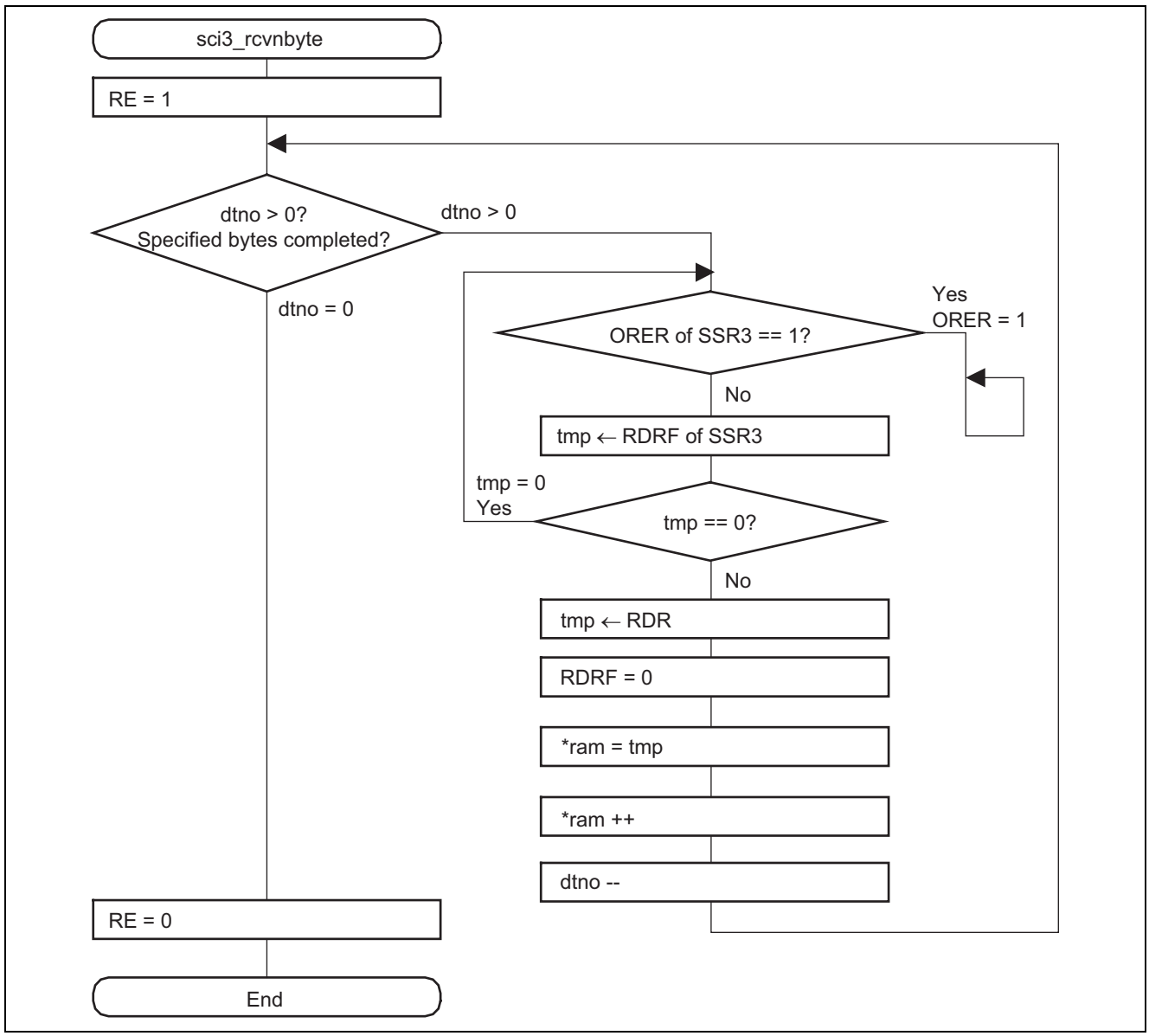
- **Serial Status Register_3 (SSR_3) Address: H'FFFE8C**

Bit	Bit Name	Setting	R/W	Description
6	RDRF	Undefined	R/(W)	Receive Data Register Full Indicates whether receive data is stored in RDR. [Setting condition] • When serial reception ends normally and receive data is transferred from RSR to RDR [Clearing conditions] • Writing of 0 to RDRF after having read RDRF = 1 • Generation of an RXI interrupt request allowing DMAC or DTC to read data from RDR. The RDRF flag is not affected and retains its previous value even though the RE bit in SCR is cleared to 0. Note that when the next reception is completed while the RDRF flag is being set to 1, an overrun error occurs and the received data are lost.
5	ORER	Undefined	R/(W)	Overrun Error [Setting condition] • Occurrence of an overrun error during reception [Clearing condition] • Writing of 0 to ORER after having read ORER = 1

Note: Only 0 can be written here, to clear the flags for RDRF and ORER.

- **Receive Data Register_3 (RDR_3) Address: H'FFFE8D**
  Function: An 8-bit register for storing receive data.
  Setting: Undefined

5. Flowchart


sci3_rcvnbyte
RE = 1
dtno > 0?
Specified bytes completed?
dtno > 0
dtno = 0
ORER of SSR3 == 1?
Yes
ORER = 1
No
tmp ← RDRF of SSR3
tmp = 0
Yes
tmp == 0?
No
tmp ← RDR
RDRF = 0
*ram = tmp
*ram ++
dtno --
RE = 0
End

7.2.4 sci3_trs1byte Function

1. Overview
   Receives one byte of clock synchronous serial data.

2. Arguments

Type	Variable Name	Description
unsigned char	tdt	Transmits one byte of data

3. Return value
   None

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **Serial Control Register_3 (SCR_3) Address: H'FFFE8A**

Bit	Bit Name	Setting	R/W	Description
5	TE	0	R/W	Transmit Enable 0: Disables transmission 1: Enables transmission

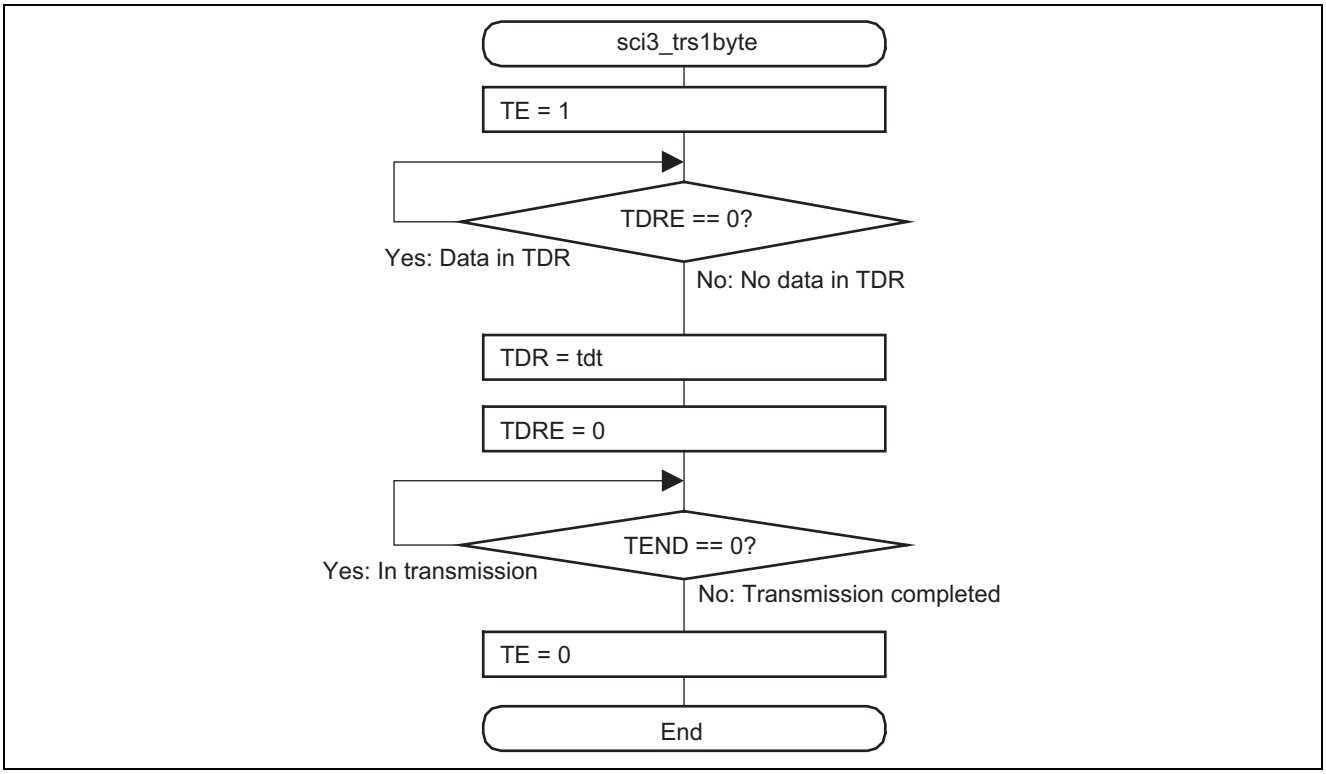
- **Transmit data Register_3 (TDR_3) Address: H'FFFE8B**
  Function: An 8-bit register for storing transmit data.
  Setting: Undefined

- **Serial Status Register_3 (SSR_3) Address: H'FFFE8C**

Bit	Bit Name	Setting	R/W	Description
7	TDRE	Undefined	R/(W)*	Transmit Data Register Empty Indicates whether TDR contains transmit data. [Setting conditions] • Clearing of TE bit in SCR to 0 • Transferring of data from TDR to TSR [Clearing conditions] • Writing of 0 to TDRE after having read TDRE = 1 • Generation of a TXI interrupt request allowing DMAC to transfer transmitted data to TDR.
2	TEND	Undefined	R	Transmit End [Setting conditions] • Clearing of TE bit in SCR to 0 • When TDRE = 1 after a specified time passed after completion of 1-byte data transfer. [Clearing conditions] • Writing of 0 to TDRE after having read TDRE = 1 • Generation of a TXI interrupt request allowing DMAC to transfer transmitted data to TDR.

Note: * Only 0 can be written here, to clear the flag for TDRE.

5. Flowchart


sci3_trs1byte
TE = 1
TDRE == 0?
Yes: Data in TDR
No: No data in TDR
TDR = tdt
TDRE = 0
TEND == 0?
Yes: In transmission
No: Transmission completed
TE = 0
End

7.2.5 sci3_trsnbyte Function

1. Overview
   Transmits n bytes of clock synchronous serial data.

2. Arguments

Type	Variable Name	Contents
unsigned short	dtno	Transmit size
unsigned char	*tdt	Start address of the transmit data

3. Return value
   None

4. Internal registers used
   The internal registers used in this sample task are shown below. The setting values are the values used in this sample task, and not the initial values.

- **Serial Control Register_3 (SCR_3) Address: H'FFFE8A**

Bit	Bit Name	Setting	R/W	Description
5	TE	0	R/W	Transmit Enable 0: Disables transmission 1: Enables transmission

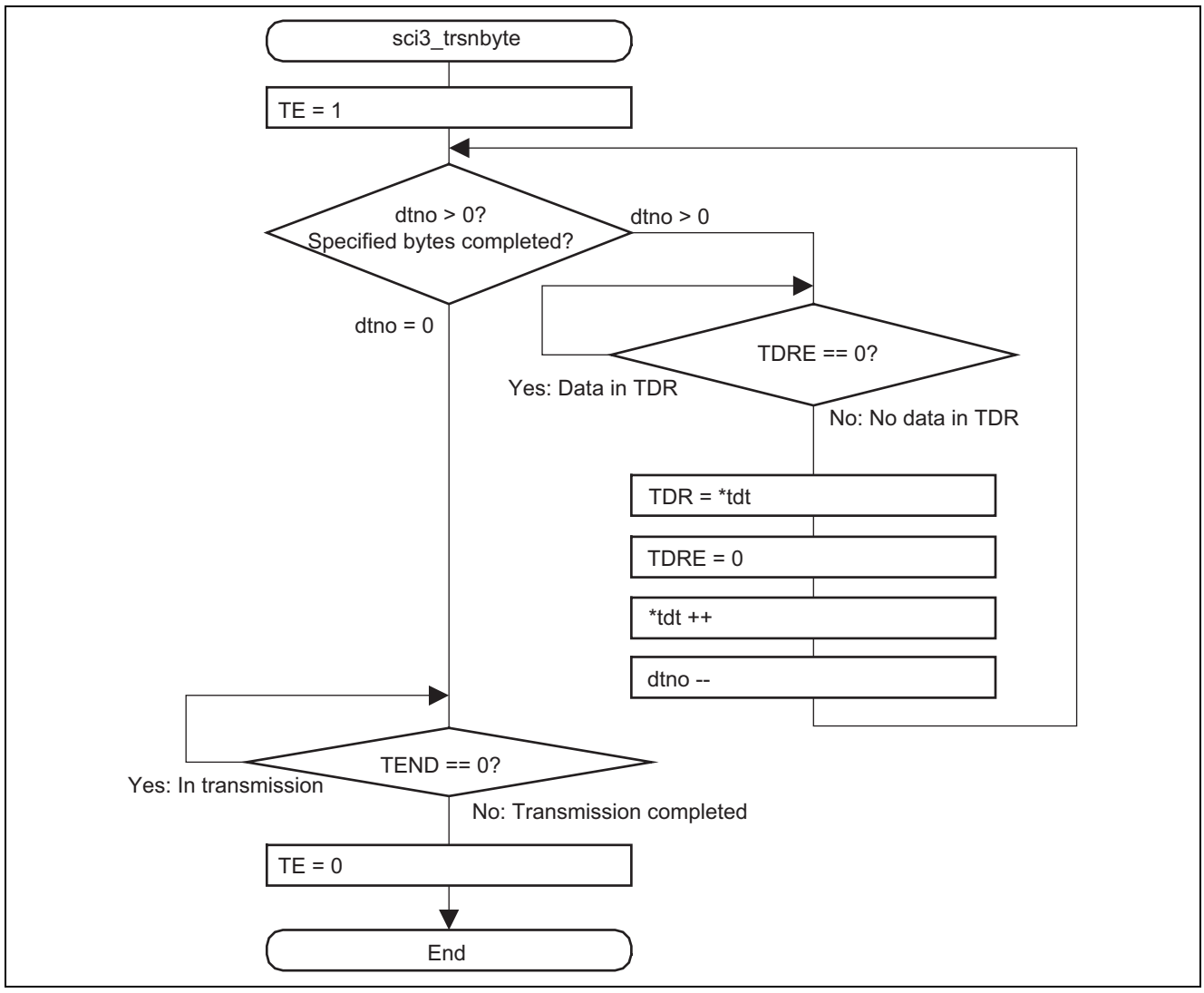
- **Transmit data Register_3 (TDR_3) Address: H'FFFE8B**
  Function: An 8-bit register for storing transmit data.
  Setting: Undefined

- **Serial Status Register_3 (SSR_3) Address: H'FFFE8C**

Bit	Bit Name	Setting	R/W	Description
7	TDRE	Undefined	R/(W)*	Transmit Data Register Empty Indicates whether TDR contains transmit data. [Setting conditions] • Clearing of TE bit in SCR to 0 • Transferring of data from TDR to TSR [Clearing conditions] • Writing of 0 to TDRE after having read TDRE = 1 • Generation of a TXI interrupt request allowing DMAC to transfer transmitted data to TDR.
2	TEND	Undefined	R	Transmit End [Setting conditions] • Clearing of TE bit in SCR to 0 • When TDRE = 1 after a specified time passed after completion of 1-byte data transfer. [Clearing conditions] • Writing of 0 to TDRE after having read TDRE = 1 • Generation of a TXI interrupt request allowing DMAC to transfer transmitted data to TDR.

Note: * Only 0 can be written here, to clear the flag for TDRE.

5. Flowchart


sci3_trsnbyte
TE = 1
dtno > 0?
Specified bytes completed?
dtno > 0
dtno = 0
TDRE == 0?
Yes: Data in TDR
No: No data in TDR
TDR = *tdt
TDRE = 0
*tdt ++
dtno --
TEND == 0?
Yes: In transmission
No: Transmission completed
TE = 0
End

8. Documents for Reference (Note)

- Hardware Manual
  H8SX/1582 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Technical News/Technical Update
  The most up-to-date information is available on the Renesas Technology Website.

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