

#### ISL91108IIA-EVZ/ISL91108IIN-EVZ

**Evaluation Board** 

AN1903 Rev 1.00 March 11, 2014

#### **Evaluation Board Features**

- · ISL91108 high efficiency buck-boost regulator
- Input voltage rating from 1.8V to 5.5V
- Resistor programmable output voltage on the ISL91108IIA-EVZ evaluation board
- Fixed 3.3V output voltage on the ISL91108IIN-EVZ evaluation board
- Up to 1.5A output current (PVIN = 3.0V, V<sub>OUT</sub> = 3.3V)
- 2.5MHz switching frequency
- Jumper selectable EN (enabled/disabled)
- Jumper selectable MODE (auto-PFM/forced-PWM)
- · Connectors, testpoints, and jumpers for easy evaluation

### Required Equipment

- · Power supply capable of delivering up to 5.5V and 4A
- · Electronic load
- · Multimeter to measure voltages and currents
- Oscilloscope

# Testpoints, Connectors, and Jumpers

**TABLE 1. DESCRIPTION OF TEST POINTS** 

TEST POINT(S)	DESCRIPTION				
TP1	LX1 (Input side of power inductor)				
TP2	LX2 (Output side of power inductor)				
TP3	V <sub>OUT</sub>				

**TABLE 2. DESCRIPTION OF CONNECTORS** 

CONNECTOR	DESCRIPTION
J1	Header for connecting input power. Includes S+ and S-sense lines.
J2	Header for connecting external load. Includes S+ and S- sense lines.

#### **TABLE 3. DESCRIPTION OF JUMPERS**

JUMPER	DESCRIPTION					
J3	Jumper to select EN input logic state. Set EN = $V_{\text{IN}}$ to enable device, or set EN = GND to disable device.					
J4	Jumper to select MODE input logic state. Set MODE = V <sub>IN</sub> to enable auto-PFM mode, or set MODE = GND to select forced PWM mode.					
	To use external sync feature, remove this jumper and apply an external clock between 2.75MHz and 3.25MHz on the center pin on the J4 header.					

### **Quick Setup Guide**

- 1. Install jumper on J3, shorting EN to VIN.
- 2. Install jumper on J4, shorting MODE to VIN.
- Connect power supply to J1, with voltage setting between 1.8V and 5.5V.
- 4. Connect electronic load to J2.
- Place scope probes on VOUT testpoint, and other testpoints of interest.
- 6. Turn on the power supply.
- Monitor the output voltage startup sequence on the scope. The waveforms will look similar to that shown in Figures 1 and 2.
- 8. Turn on the electronic load.
- Measure the output voltage with the voltmeter. The voltage should regulate within data sheet spec limits.
- 10. To determine efficiency, measure input and output voltages at the Kelvin sense testpoints (S+ and S-) which are part of J1 and J2 headers. The bench power supply can be connected to the PVIN and GND headers on J1. The electronic load can be connected to the VOUT and GND headers on J2. Measure the input and output currents. Calculate efficiency based on these measurements.
- 11. To test external sync, remove the jumper at J4, then apply an external clock between 2.75MHz and 3.25MHz on the MODE input (the center pin of header J4).

### **Typical Start-up Waveforms**

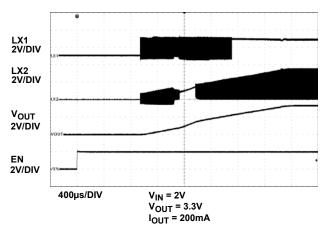


FIGURE 1. ISL91108 START-UP WITH  $V_{IN}$  = 2V and  $V_{OUT}$  = 3.3V

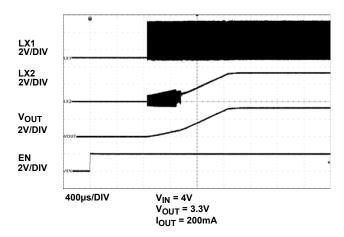


FIGURE 2. ISL91108 START-UP WITH  $\ensuremath{V_{IN}}=4\ensuremath{V}$  and  $\ensuremath{V_{OUT}}=3.3\ensuremath{V}$ 

## **Output Voltage Programming**

The ISL91108IIA-EVZ evaluation board uses resistors to program the output voltage. To change the output voltage, resistor R1 should be removed and replaced with a resistor value corresponding to the desired output voltage, as shown in Table 4. A precision resistor with 1% tolerance should be used.

**TABLE 4. OUTPUT VOLTAGE PROGRAMMING** 

DESIRED OUTPUT VOLTAGE (V)	R1 RESISTOR VALUE ( $\mathbf{k}\Omega$ )
2.0	90.9
2.5	127
3.0	165
3.3	187
3.6	210
4.0	243
4.5	280
5.0	316

### **ISL91108IIA-EVZ Evaluation Board Schematic**

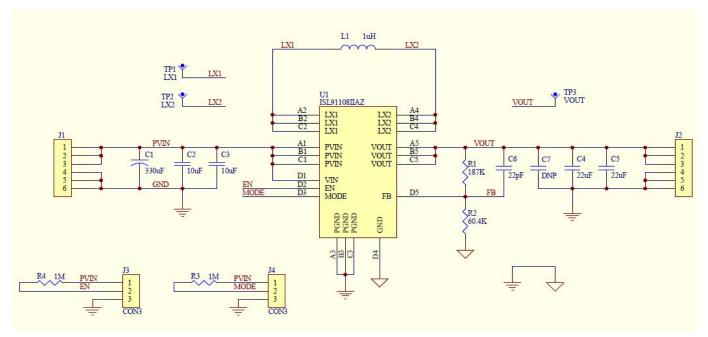


FIGURE 3. ISL91108IIA-EVZ EVALUATION BOARD SCHEMATIC

#### TABLE 5. ISL91108IIA-EVZ EVALUATION BOARD BILL OF MATERIALS

ITEM#	QTY	DESIGNATORS	PART TYPE	FOOTPRINT	DESCRIPTION	VENDORS
1	1	U1	ISL91108IIAZ	W4x5.20 WLCSP	Intersil ISL91108 Buck-Boost Regulator with Adjustable Output Voltage	INTERSIL
2	1	L1	1μΗ	3.2mmx2.5mm	Power Inductor DFE322512C, 4.6A, $34m\Omega$	токо
3	1	C1	330µF	7343	Capacitor, Tantalum	ANY
4	2	C2, C3	10µF/16V/X5R	0603	Capacitor, Ceramic, GRM188R61C106MA73D	Murata
5	2	C4, C5	22μF/10V/X5R	0603	Capacitor, Ceramic, GRM188R61A226M	Murata
6	1	C6	22pF/50V/NP0	0402	Capacitor, Generic	ANY
7	1	<b>C</b> 7	0.1μF	0402	Capacitor, Generic	ANY
8	1	R1	187k $\Omega$ , 1%	0402	Resistor, Generic	ANY
9	1	R2	60.4kΩ, <b>1</b> %	0402	Resistor, Generic	ANY
10	2	R3, R4	<b>1</b> ΜΩ, 5%	0603	Resistor, Generic	ANY
11	2	J1, J2	HDR-6	HDR-6	Vert. Pin Header, 6-Pin, 0.1" Spacing, Generic	ANY
12	2	J3, J4	HDR-3	HDR-3	Vert. Pin Header, 3-Pin, 0.1" Spacing, Generic	ANY
13	3	TP1, TP2, TP3	SCOPEPROBE	SCOPEPROBE	Test Point, Scope Probe 131-5031-00	TEKTRONIX

# **ISL91108IIN-EVZ Evaluation Board Schematic**

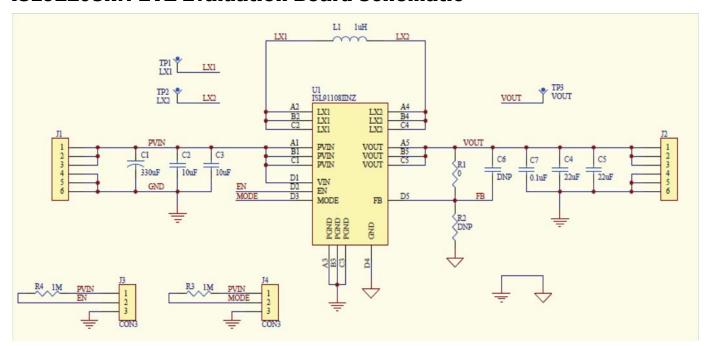


FIGURE 4. ISL91108IIN-EVZ EVALUATION BOARD SCHEMATIC

#### TABLE 6. ISL91108IIN-EVZ EVALUATION BOARD BILL OF MATERIALS

ITEM#	QTY	DESIGNATORS	PART TYPE	FOOTPRINT	DESCRIPTION	VENDORS
1	1	U1	ISL91108IINZ	W4x5.20 WLCSP	Intersil ISL91108 Buck-Boost Regulator with Fixed 3.3V Output Voltage	INTERSIL
2	1	L1	1μΗ	3.2mmx2.5mm	Power Inductor DFE322512C, 4.6A, $34m\Omega$	токо
3	1	C1	330µF	7343	Capacitor, Tantalum	ANY
4	2	C2, C3	10µF/16V/X5R	0603	Capacitor, Ceramic, GRM188R61C106MA73D	Murata
5	2	C4, C5	22μF/10V/X5R	0603	Capacitor, Ceramic, GRM188R61A226M	Murata
6	1	C6	DNP	0402		ANY
7	1	<b>C</b> 7	0.1μF	0402	Capacitor, Generic	ANY
8	1	R1	<b>0</b> Ω	0402	Resistor, Generic	ANY
9	1	R2	DNP	0402		ANY
10	2	R3, R4	<b>1M</b> Ω, 5%	0603	Resistor, Generic	ANY
11	2	J1, J2	HDR-6	HDR-6	Vert. Pin Header, 6-Pin, 0.1" Spacing, Generic	ANY
12	2	J3, J4	HDR-3	HDR-3	Vert. Pin Header, 3-Pin, 0.1" Spacing, Generic	ANY
13	3	TP1, TP2, TP3	SCOPEPROBE	SCOPEPROBE	Test Point, Scope Probe 131-5031-00	TEKTRONIX

# **ISL91108 Evaluation Board Layout**

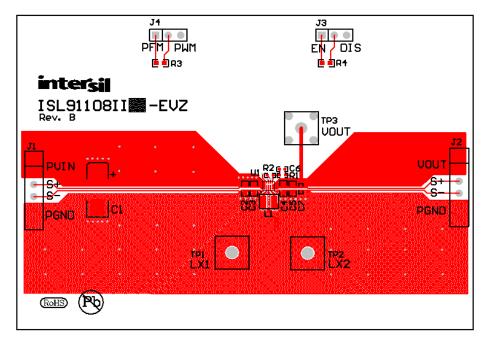


FIGURE 5. ISL91108 EVALUATION BOARD LAYOUT

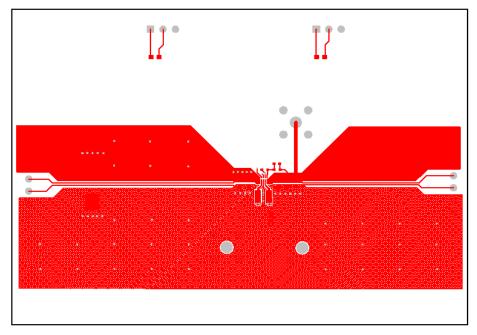


FIGURE 6. TOP LAYER

# ISL91108 Evaluation Board Layout (Continued)

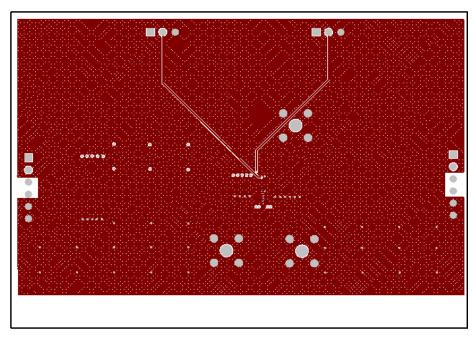


FIGURE 7. MID LAYER

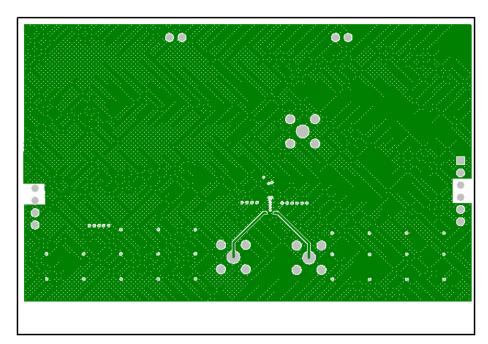


FIGURE 8. MID LAYER 2

# ISL91108 Evaluation Board Layout (Continued)

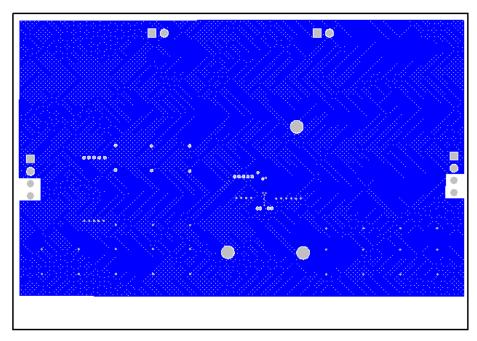


FIGURE 9. BOTTOM LAYER

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