

ISL55110 11EVAL1Z, ISL55110 11EVAL2Z

Evaluation Board User's Manual

AN1283 Rev 0.00 February 13, 2007

Before Getting Started

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Scope Probe Test Points (TP) are provisioned across all inputs, outputs and VDD/VH to ground.

SCOPE PROBE CONNECTIONS

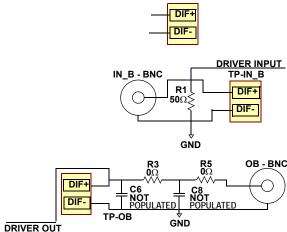


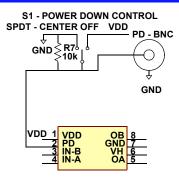
FIGURE 1. DUAL.1" SPACED PINS ARE PLACED ON THE EVALUATIONS BOARDS FOR LEADLESS ACTIVE PROBE CONNECTIONS

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ISL55110, ISL55111_TSSOP

FIGURE 2. TSSOP AND QFN EVALUATION BOARDS HAVE THE SAME POWER DOWN CIRCUITRY

Finally the center off position provides a means of connecting a repetitive signal source to the PD input. This is so that the user can observe Power Down Enable/Disable timing. An important note to remember when using the PD - BNC: 1) Place the switch in Center-Off position. 2) The PD input is referenced to VDD and ground.

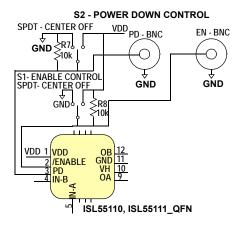


FIGURE 3. QFN PACKAGES HAVE BOTH POWER DOWN AND OUTPUT ENABLE DIGITAL INPUTS

Initial Power Up

Please refer to the device specification for power up sequencing and current requirements. Also note that the frequency of operation of each driver will determine the current needed. There are graphs in the specification regarding current characteristics.

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Schematics are drawn with physical location in mind. Any changes in electrical circuitry will be updated in this document as needed.

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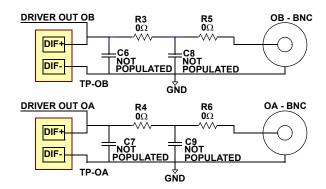


FIGURE 4. CUSTOM LOAD COMPONENTS

Component locations C6 to C7 and R3 to R6 are surface mount locations provided so the user can experiment with various load configurations.

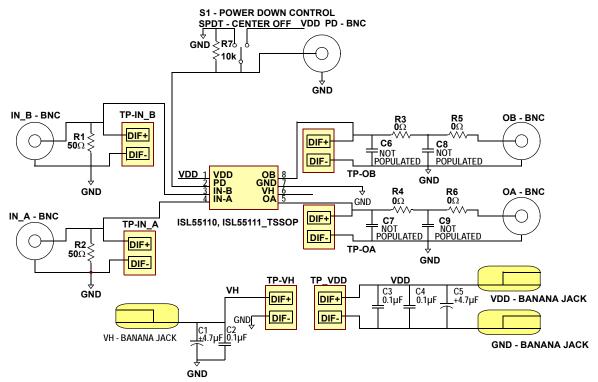


FIGURE 5. TSSOP EVALUATION BOARD SCHEMATIC

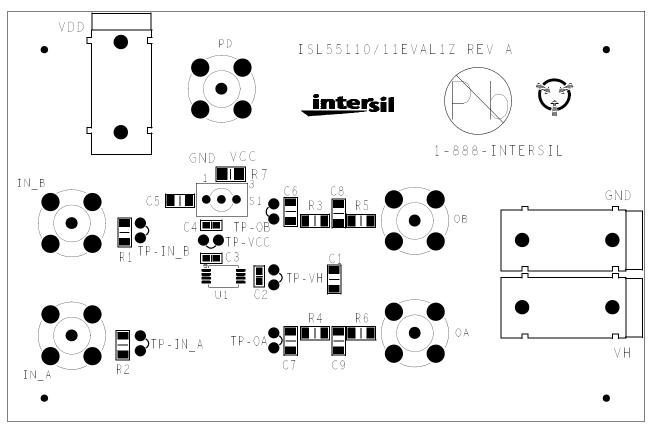


FIGURE 6. TSSOP LAYOUT

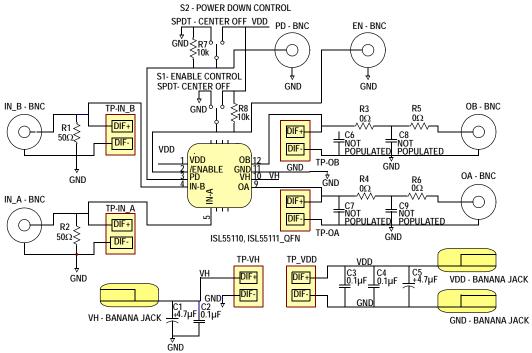
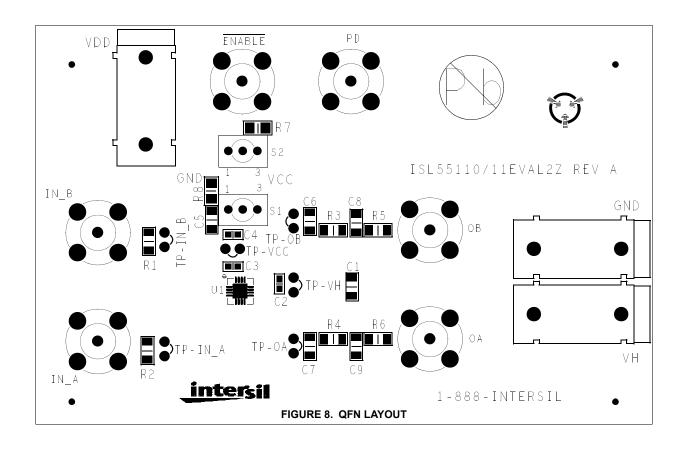


FIGURE 7. QFN EVALUATION BOARD SCHEMATIC



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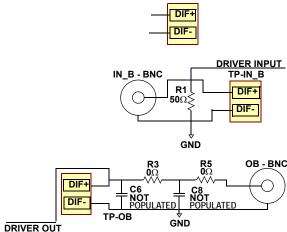


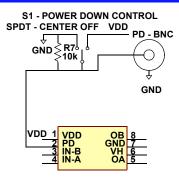
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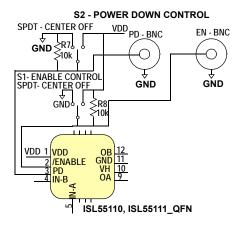


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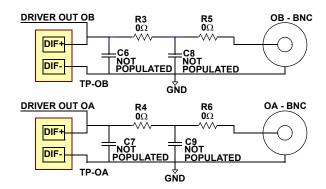


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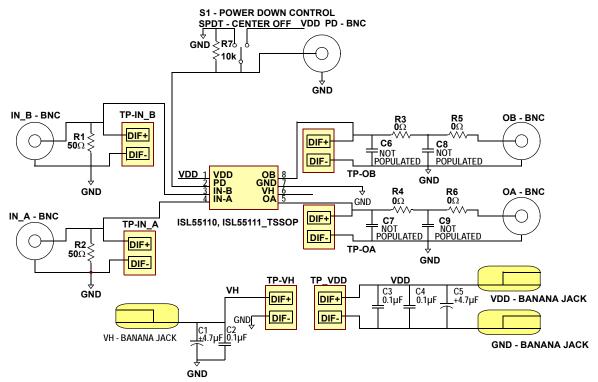


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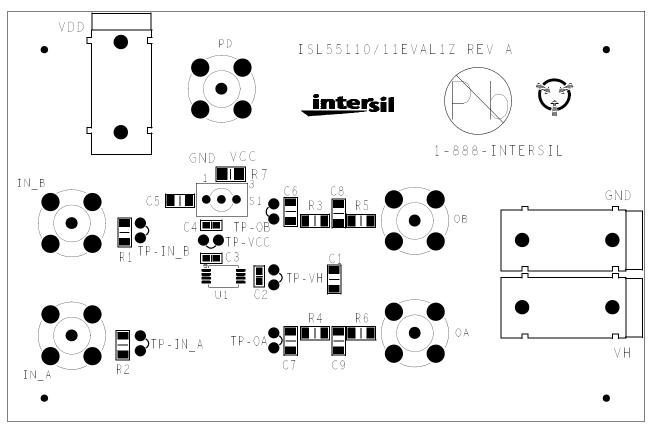


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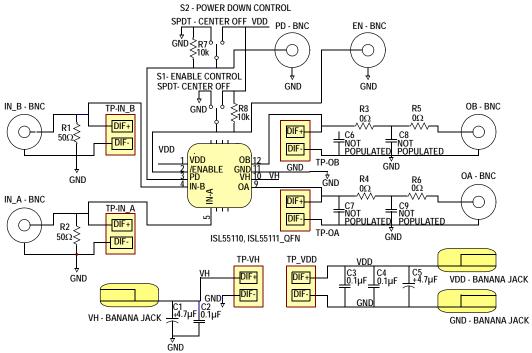
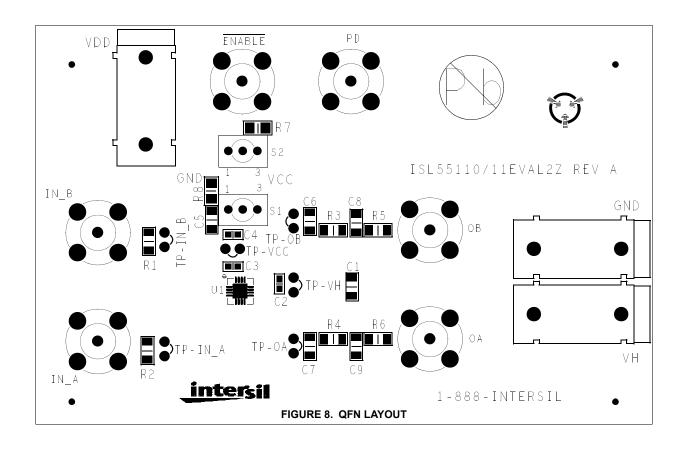


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