intersil

DATASHEET

HS-139RH, HS-139EH

Radiation Hardened Quad Voltage Comparator

The Radiation Hardened HS-139RH, HS-139EH consists of four independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground, even when operated from a single supply and the low supply current makes these comparators suitable for low power applications. These types were designed to directly interface with TTL and CMOS.

The HS-139RH, HS-139EH are fabricated on our dielectrically isolated Rad Hard Silicon Gate (RSG) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-139RH, HS-139EH are contained in <u>SMD 5962-98613</u>. A "hot-link" is provided on our homepage with instructions for downloading. www.intersil.com/spacedefense/newsafclasst.asp

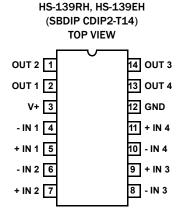
Features

- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
 - Latch-up free under any conditions
- SEU LET threshold 20MeV/cm²/mg
- Low dose rate effects immunity
- 100V output voltage withstand capability
- ESD protection to >3000V
- Differential input voltage range equal to the supply voltage
- Input offset voltage (VIO)..... 2mV (Max)
- Quiescent supply current 2mA (Max)
- Pb-Free (RoHS Compliant)

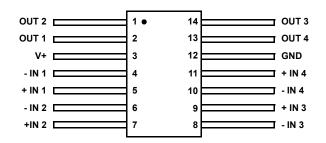
Applications

- Pulse generators
- Timing circuitry
- Level shifting
- · Analog-to-digital conversion

Pin Configurations



HS-139RH, HS-139EH (FLATPACK CDFP3-F14) TOP VIEW



FN3573 Rev 6.00 August 8, 2013

Ordering Information

ORDERING SMD NUMBER (Note 1)	PART NUMBER (Note 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F9861303VCC	HS1-139EH-Q	Q 5962F98 61303VCC	-55 to +125	14 Ld SBDIP	D14.3
5962F9861301VCC	HS1-139RH-Q	Q 5962F98 61301VCC	-55 to +125	14 Ld SBDIP	D14.3
5962F9861301QCC	HS1-139RH-8	Q 5962F98 61301QCC	-55 to +125	14 Ld SBDIP	D14.3
HS1-139RH/PROTO	HS1-139RH/PROTO	HS1-139RH/PROTO	-55 to +125	14 Ld SBDIP	D14.3
5962F9861301VXC	HS9-139RH-Q	Q 5962F98 61301VXC	-55 to +125	14 Ld FLATPACK	K14.A
5962F9861301QXC	HS9-139RH-8	Q 5962F98 61301QXC	-55 to +125	14 Ld FLATPACK	K14.A
5962F9861303VXC	HS9-139EH-Q	Q 5962F98 61303VXC	-55 to +125	14 Ld FLATPACK	K14.A
HS9-139RH/PROTO	HS9-139RH/PROTO	HS9-139RH /PROTO	-55 to +125	14 Ld FLATPACK	K14.A
5962F9861303V9A	HSO-139EH-Q		-55 to +125	Die	
5962F9861301V9A	HSO-139RH-Q		-55 to +125	Die	
HS0-139RH/SAMPLE	HS0-139RH/SAMPLE		-55 to +125	Die	

NOTES:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table on page 2 must be used when ordering.

2. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Die Characteristics

DIE DIMENSIONS:

3750µm x 2820µm (148 mils x 111 mils) 483µm ±25.4µm (19 mils ±1 mil)

INTERFACE MATERIALS:

Glassivation:

Type: Silox (SiO₂) Thickness: 8.0kÅ ±1.0kÅ

Top Metallization:

Type: AlSiCu Thickness: 16.0kÅ ±2kÅ

Substrate:

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

Worst Case Current Density:

 $<2.0 \text{ x} 10^5 \text{ A/cm}^2$

Transistor Count:

49

Metallization Mask Layout

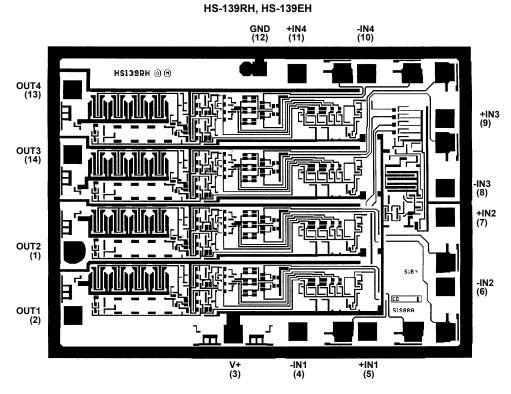


TABLE 1. HS-139RH, HS-139EH PAD COORDINATES

		RELATIVE TO PIN 1		
PIN NUMBER	PAD NAME	X COORDINATES	Y COORDINATES	
1	OUT 2	0	0	
2	OUT 1	0	-535	
3	V+	1323	-688	
4	-IN 1	1862	-670	
5	+IN 1	2439	-670	
6	-IN 2	3084	-299	
7	+IN 2	3084	278	
8	-IN 3	3084	518	
9	+IN 3	3084	1095	
10	-IN 4	2439	1466	
11	+IN 4	1862	1466	
12	GND	1550	1503	
13	OUT 4	0	1331	
14	OUT 3	0	796	

NOTE: Dimensions in microns

© Copyright Intersil Americas LLC 1999-2013. All Rights Reserved. All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

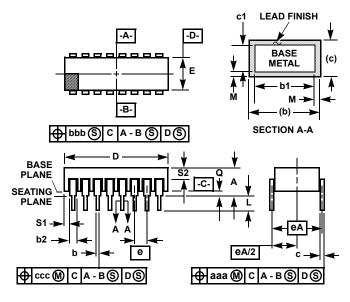
Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

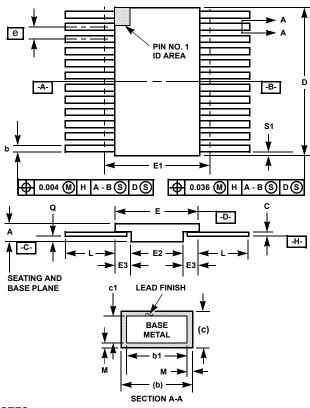
- Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- 4. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- 5. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
- Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
- 7. Dimension Q shall be measured from the seating plane to the base plane.
- 8. Measure dimension S1 at all four corners.
- 9. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
- 10. N is the maximum number of terminal positions.
- 11. Braze fillets shall be concave.
- 12. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 13. Controlling dimension: INCH.

D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C) 14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
с	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
е	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90 ⁰	105 ⁰	90 ⁰	105 ⁰	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
М	-	0.0015	-	0.038	2
Ν	1	4	1	4	8

Rev. 0 4/94

Ceramic Metal Seal Flatpack Packages (Flatpack)



K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B) 14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
С	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
е	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
М	-	0.0015	-	0.04	-
N	1	4	1	4	-

NOTES:

- Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
- 2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
- 3. This dimension allows for off-center lid, meniscus, and glass overrun.
- 4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- 5. N is the maximum number of terminal positions.
- 6. Measure dimension S1 at all four corners.
- For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
- 8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
- 9. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 10. Controlling dimension: INCH.

Rev. 0 5/18/94