

NP35N04YUG

MOS FIELD EFFECT TRANSISTOR

R07DS0016EJ0100 Rev.1.00 Jul 01, 2010

Description

The NP35N04YUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
 - $R_{DS(on)} = 10 \text{ m}\Omega \text{ MAX}$. ($V_{GS} = 10 \text{ V}$, $I_D = 17.5 \text{ A}$)
- Low Ciss: Ciss = 1900 pF TYP. $(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP35N04YUG -E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	8-pin HSON, Taping (E1 type)
NP35N04YUG -E2-AY *1			8-pin HSON, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25^{\circ}C$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V _{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±35	А
Drain Current (pulse) *1	I _{D(pulse)}	±105	А
Total Power Dissipation (T _C = 25°C)	P _{T1}	77	W
Total Power Dissipation (T _A = 25°C) *2	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	−55 to +175	°C
Repetitive Avalanche Current *3	I _{AR}	22	А
Repetitive Avalanche Energy *3	E _{AR}	48	mJ

Thermal Resistance

Notes: *1. $T_C = 25^{\circ}C$, PW $\leq 10 \mu s$, Duty Cycle $\leq 1\%$

*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mmt

*3. $T_{ch(peak)} \le 150^{\circ}C$, $R_G = 25 \Omega$

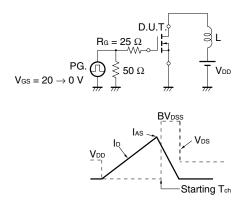
Electrical Characteristics ($T_A = 25^{\circ}C$)

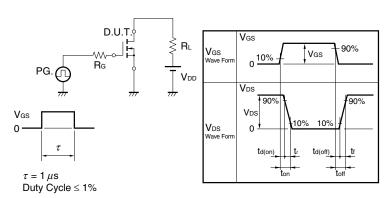
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
Forward Transfer Admittance *1	y _{fs}	8.0	16		S	$V_{DS} = 5 \text{ V}, I_{D} = 17.5 \text{ A}$
Drain to Source On-state Resistance *1	R _{DS(on)}		7.9	10	mΩ	V _{GS} = 10 V, I _D = 17.5 A
Input Capacitance	C _{iss}		1900	2850	pF	$V_{DS} = 25 V$,
Output Capacitance	Coss		190	290	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		120	220	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		18	36	ns	$V_{DD} = 20 \text{ V}, I_D = 17.5 \text{ A},$
Rise Time	t _r		10	25	ns	$V_{GS} = 10 \text{ V},$
Turn-off Delay Time	$t_{d(off)}$		38	76	ns	$R_G = 0 \Omega$
Fall Time	t _f		5	13	ns	
Total Gate Charge	Q_G		36	54	nC	$V_{DD} = 32 V$,
Gate to Source Charge	Q_{GS}		10		nC	V _{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		12		nC	I _D = 35 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I _F = 35 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		31		ns	$I_F = 35 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Q _{rr}		30		nC	di/dt = 100 A/μs

Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME

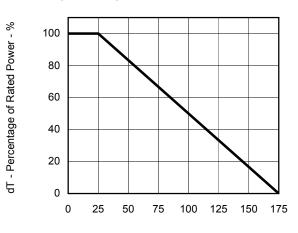




TEST CIRCUIT 3 GATE CHARGE

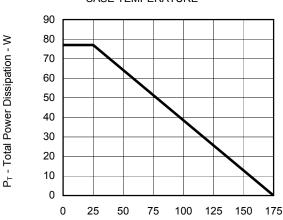
Typical Characteristics ($T_A = 25^{\circ}C$)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



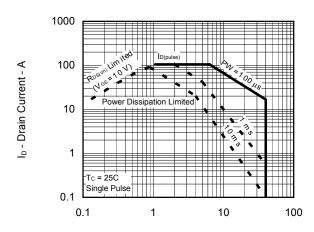
 T_{C} - Case Temperature - $^{\circ}\text{C}$

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



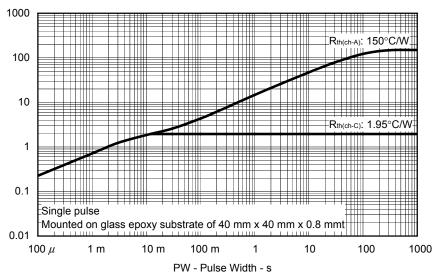
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



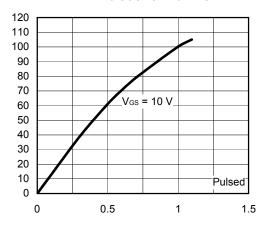


I_D - Drain Current - A

V_{GS(th)} - Gate to Source Threshold Voltage - V

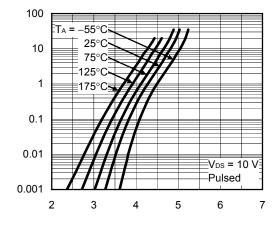
 $R_{\text{DS}(\text{on})}$ - Drain to Source On-state Resistance - $m\Omega$





 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS

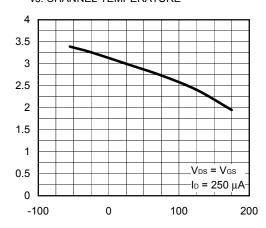


Ip - Drain Current - A

y_{fs} | - Forward Transfer Admittance - S

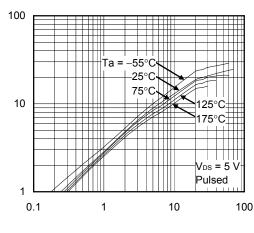
V_{GS} - Gate to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



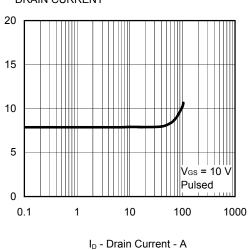
T_{ch} - Channel Temperature - °C

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

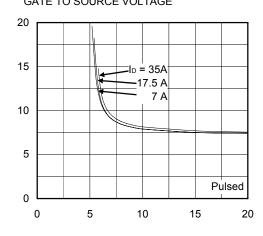


ID - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



 V_{GS} - Gate to Source Voltage - V

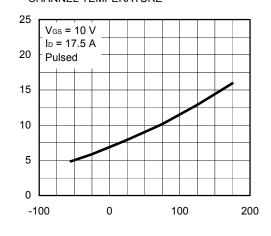
 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

t_{d(on)}, t_r, t_{d(off)}, t_f - Switching Time - ns

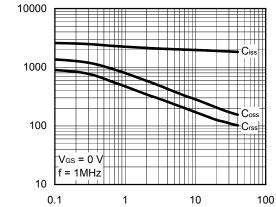
I_F - Diode Forward Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



T_{ch} - Channel Temperature - $^{\circ}C$

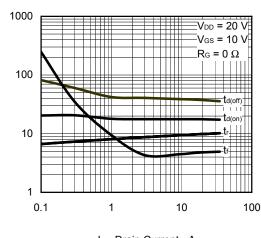
Ciss, Coss, Crss - Capacitance - pF



CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

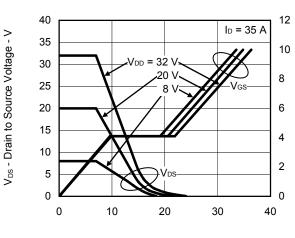
V_{DS} - Drain to Source Voltage - V

SWITCHING CHARACTERISTICS



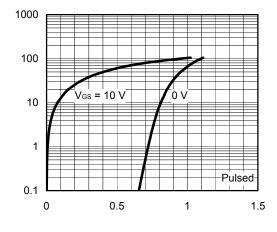
I_D - Drain Current - A

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



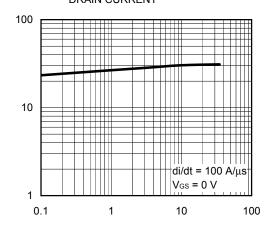
Q_G - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



 $V_{\text{F(S-D)}}$ - Source to Drain Voltage - V

REVERSE RECOVERY TIME vs. DRAIN CURRENT

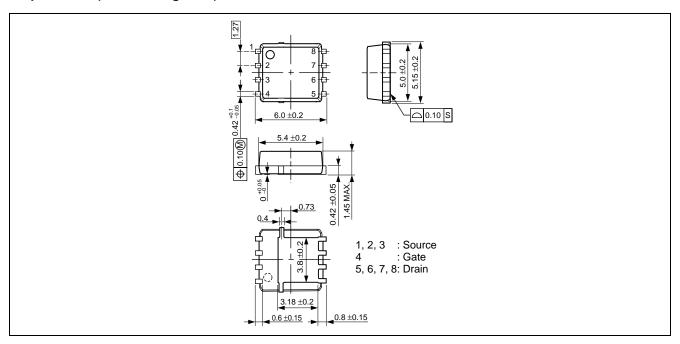


I_F - Drain Current - A

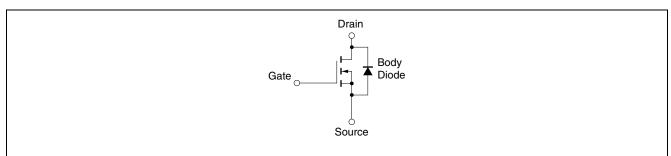
t_{rr} - Reverse Recovery Time - ns

Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History NP35N04YUG

		Description		
Rev.	Date	Page	Summary	
1.00	Jul 01, 2010	-	First Eddition Issued	

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