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Renesas Electronics website: http://www.renesas.com

April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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# MOS FIELD EFFECT TRANSISTOR NP90N06VLG

# **SWITCHING N-CHANNEL POWER MOS FET**

## **DESCRIPTION**

The NP90N06VLG is N-channel MOS Field Effect Transistor designed for high current switching applications.

# ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE		
NP90N06VLG-E1-AY Note	Dura Cn /Tin)	Tono 2500 n/rool	TO 252 (MD 27D) him 0.27 c		
NP90N06VLG-E2-AY Note	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZP) typ. 0.27 g		

Note Pb-free (This product does not contain Pb in external electrode.)

## **FEATURES**

- Logic level
- Built-in gate protection diode
- Super low on-state resistance

 $R_{DS(on)1} = 7.8 \text{ m}\Omega$  MAX. (Vgs = 10 V, ID = 45 A)

 $R_{DS(on)2} = 12.5 \text{ m}\Omega$  MAX. (Vgs = 4.5 V, ID = 35 A)

High current rating

 $I_{D(DC)} = \pm 90 \text{ A}$ 

Low input capacitance

Ciss = 4600 pF TYP.

• Designed for automotive application and AEC-Q101 qualified

# ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	60	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±90	Α
Drain Current (pulse) Note1	D(pulse)	±180	Α
Total Power Dissipation (Tc = 25°C)	P <sub>T1</sub>	105	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.2	W
Channel Temperature	Tch	175	$^{\circ}\text{C}$
Storage Temperature	Tstg	-55 to +175	°C
Repetitive Avalanche Current Note2	Iar	32	Α
Repetitive Avalanche Energy Note2	Ear	102	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

**2.** Tch  $\leq 150^{\circ}$ C, Rg = 25  $\Omega$ 

## THERMAL RESISTANCE

Channel to Case Thermal Resistance 1.43 °C/W Rth(ch-C) Channel to Ambient Thermal Resistance  $R_{th(ch-A)}$ 125 °C/W

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(TO-252)

# **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

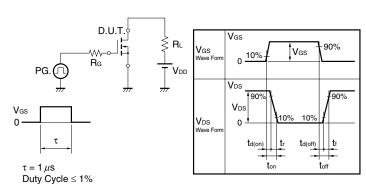
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	μΑ
Gate Leakage Current	Igss	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μΑ
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.4		2.5	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 45 A	30	66		S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 45 A		6.2	7.8	mΩ
	RDS(on)2	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 35 A		7.5	12.5	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 25 V,		4600	6900	pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		370	560	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		220	400	pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 45 A,		17	34	ns
Rise Time	tr	V <sub>GS</sub> = 10 V,		13	33	ns
Turn-off Delay Time	t <sub>d(off)</sub>	$R_G = 0 \Omega$		76	152	ns
Fall Time	tf			7	18	ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 48 V,		90	135	nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = 10 V,		13		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 90 A		26		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = 90 A, V <sub>GS</sub> = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	I <sub>F</sub> = 90 A, V <sub>GS</sub> = 0 V,		38		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>μ</i> s		56		nC

Note Pulsed test

# TEST CIRCUIT 1 AVALANCHE CAPABILITY

# $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$

# **TEST CIRCUIT 2 SWITCHING TIME**



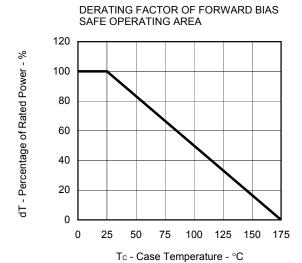
# **TEST CIRCUIT 3 GATE CHARGE**

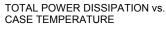
$$\begin{array}{c|c} D.U.T. \\ I_G = 2 \text{ mA} \\ \hline \end{array}$$

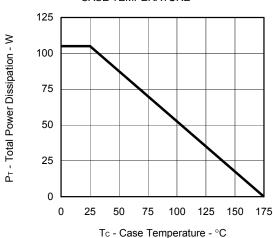
$$\begin{array}{c|c} PG. & \\ \hline \end{array} \begin{array}{c} S & \Omega \\ \hline \end{array} \begin{array}{c} O.U.T. \\ \hline \end{array}$$

-Starting Tch

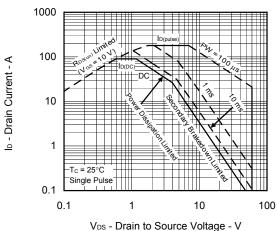
# TYPICAL CHARACTERISTICS (TA = 25°C)



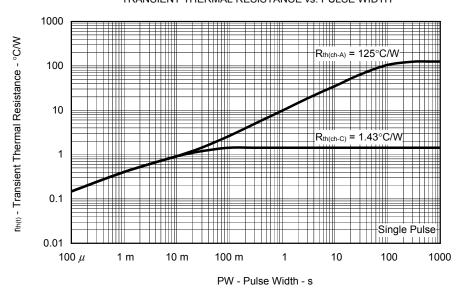




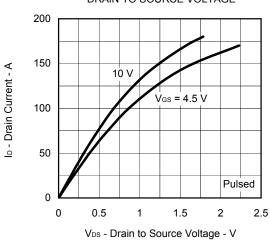
## FORWARD BIAS SAFE OPERATING AREA



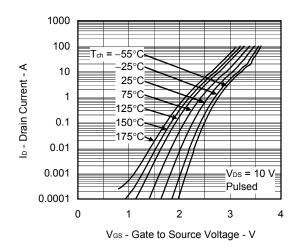




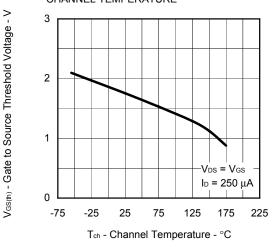
# DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



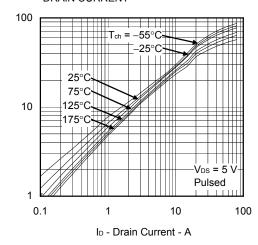
# FORWARD TRANSFER CHARACTERISTICS



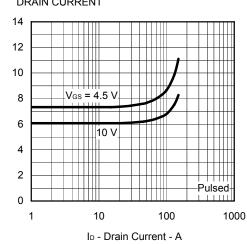
# GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



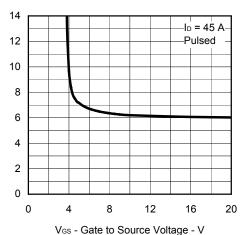
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



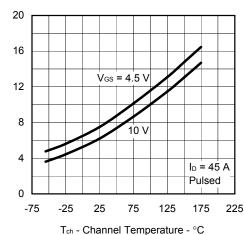
R<sub>DS(m)</sub> - Drain to Source On-state Resistance - mΩ

l y<sub>s</sub> | - Forward Transfer Admittance -

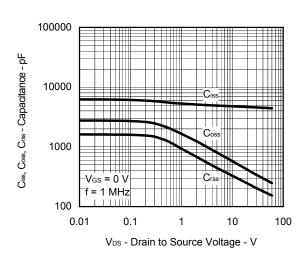
R<sub>DS(m)</sub> - Drain to Source On-state Resistance - mΩ

RDS(on) - Drain to Source On-state Resistance - m\Omega

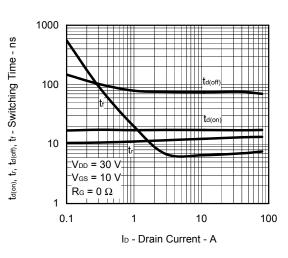
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



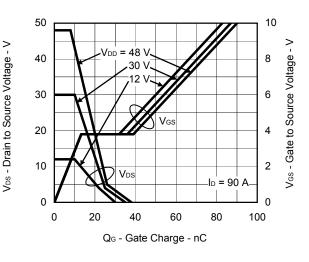
#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



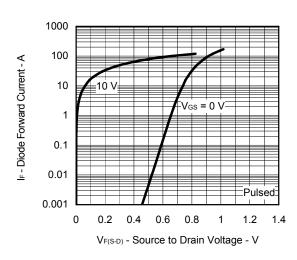
## SWITCHING CHARACTERISTICS



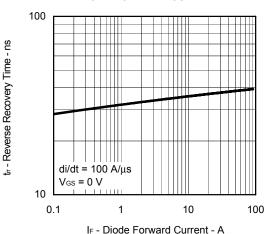
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE

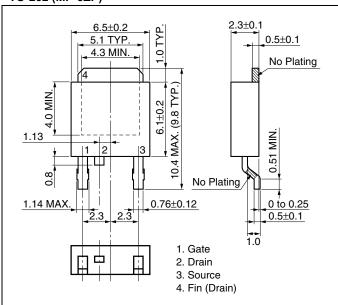


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

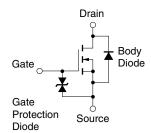


# PACKAGE DRAWING (Unit: mm)

# TO-252 (MP-3ZP)



# **EQUIVALENT CIRCUIT**



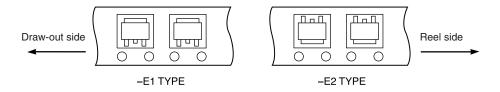
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

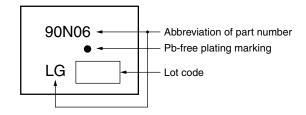
6

## TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



## MARKING INFORMATION



## RECOMMENDED SOLDERING CONDITIONS

The NP90N06VLG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below	IR60-00-3
	Time at maximum temperature: 10 seconds or less	
	Time of temperature higher than 220°C: 60 seconds or less	
	Preheating time at 160 to 180°C: 60 to 120 seconds	
	Maximum number of reflow processes: 3 times	
	Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	
Partial heating	Maximum temperature (Pin temperature): 350°C or below	P350
	Time (per side of the device): 3 seconds or less	
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less	

Caution Do not use different soldering methods together (except for partial heating).

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