Voltage Controlled SAW Oscillator (VCSO) Fundamentals

VCSO Overview

SAW Voltage Controlled Oscillators (VCSO) have been used for many years in telecommunications, military, and commercial applications requiring low phase noise and jitter at fundamental frequencies up to 1000 MHz. They have flown in space, on aircraft, on missiles, and have been a key component in modern telecommunications systems.

VCSOs use a quartz SAW (Surface Acoustic Wave) delay line as the frequency controlling element. The SAW delay lines are fabricated on a 0.5mm thick quartz wafer using planar processing similar to that of an IC. The frequency selective aluminum pattern is on the surface of the quartz allowing the delay line to be securely mounted in its package. This construction provides a small and rugged resonant element, that when used in a VCSO, results in very low vibration sensitivity ($1x10^{-9}$/Gp to $6x10^{-9}$/Gp).

The phase vs. frequency of a SAW delay line is very linear giving VCSOs very linear and repeatable tuning characteristics. In many applications VCSOs are used in a phase lock loop (PLL) to lock the VCSO to a stable low frequency reference, attenuate reference jitter, or track or filter reference modulation. The linear tuning characteristic is critical in many of these applications.

VCSOs in many ways can be considered midrange between voltage controlled crystal oscillators (VCXO) and lumped constant voltage controlled oscillator (LC VCO). VCSOs have much better far out phase noise than VCXOs, and have only somewhat worse in close-in phase noise (< 10kHz offset) than VCXOs. The VCSO noise is lower than that of a LC VCO. VCSOs are much more stable than LC VCOs and not quite as stable as a VCXO. VCSOs typically tune 700 ppm to 1500 ppm, whereas VCXOs tune less than 200 ppm, and LC many thousands of ppm.

In short, when there is a need for a high frequency, low noise, small and rugged oscillator, VCSOs should be given serious consideration. The next sections will provide details of just how a VCSO works and design trade-offs that can be made to optimize performance for a particular application.

The SAW Delay Line

The component that differentiates a VCSO from other oscillators is the SAW delay line. A drawing of a SAW delay line is shown in Figure 1. A typical delay line is 4.5 x 1.3 x 0.5mm and has the transducer pattern metallization on the top surface. The input transducer converts the electrical signal to acoustic energy that propagates on the surface of the quartz to the output transducer that converts the acoustic energy back to an electrical signal. The transducer pattern (much more complicated that shown) determines the center frequency and bandwidth of the delay line. The distance between the centers of the transducers determines the delay.

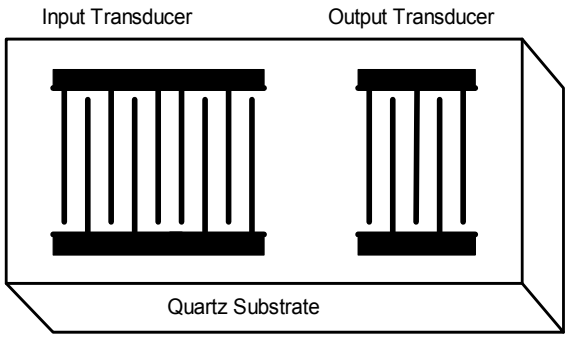


Figure 1 Typical SAW Delay Line

The SAW delay lines used in the VCSOs are designed such that the delay is approximately equal to the inverse of the bandwidth (Td = 1/BW). This results in a linear 360° of phase shift over the -3 dB bandwidth of the SAW delay line. The delay lines are designed for minimum insertion loss to minimize phase noise.

Figure 2 shows the insertion loss and phase of a 777.7 MHz delay line. Note that the phase shifts approximately 360° over the -3 dB bandwidth. The reason for this will be discussed in the oscillator section.

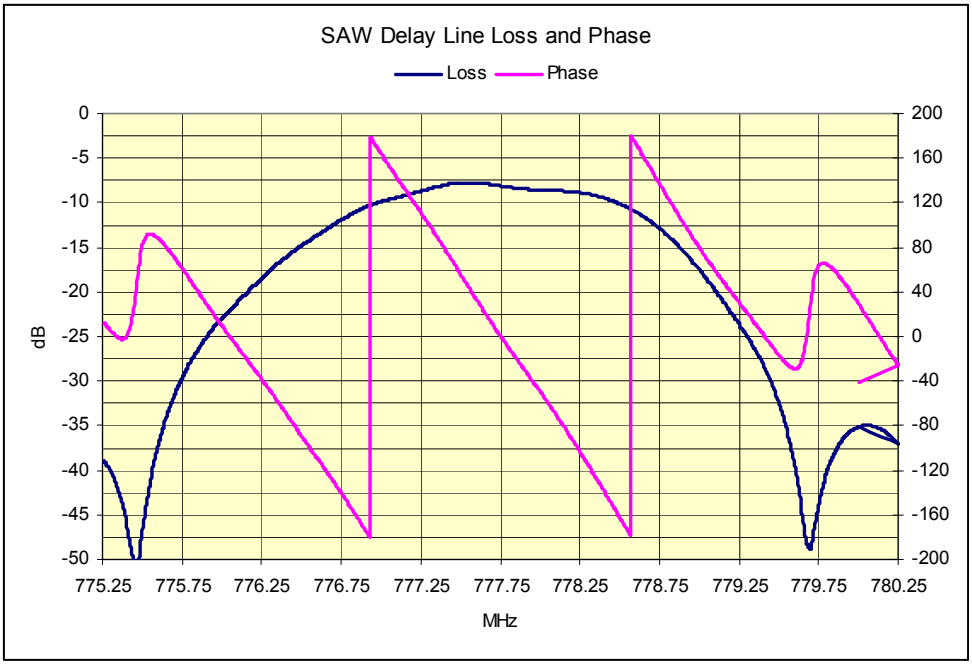


Figure 2 777.7 MHz Delay Line Insertion Loss (blue) and Phase (fuchsia)

Oscillation Criteria

The IDT VCSOs are transmission oscillators, meaning that the oscillator consists of an amplifier and a circuit connected from the amplifier output to the amplifier input. A simple transmission oscillator is shown in Figure 3.

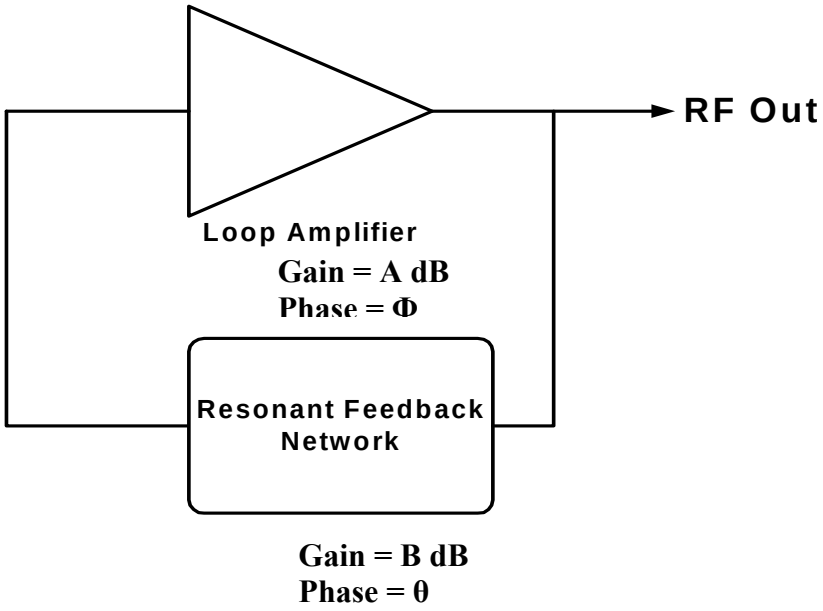


Figure 3 Transmission Oscillator Block Diagram

Two criteria must be met for the circuit in Figure 3 to sustain oscillation; the oscillator loop gain must be equal to, or greater than, 1 (0 dB); and the oscillator loop phase shift must be 0° or a multiple of 360°. The oscillator will oscillate at a frequency the meets the two requirements. Thus, referring to Figure 3, the loop gain, A+B must be greater than 0 dB and the loop phase; Φ+θ must be nx360°. The SAW delay lines are designed to have 360° of phase shift over their -3 dB bandwidth so that only one frequency can meet the phase criteria for the oscillation in the -3 dB bandwidth. When oscillation stabilizes and the amplifier goes into limit, the gain around the loop will be exactly unity.

Using the oscillator in Figure 3, it is possible to qualitatively describe oscillator startup. The delay line shown in Figure 2 will serve as the feedback network. The phase at 777.75 MHz is 0° and the gain is -8 dB. Assume that the amplifier has 360° of phase shift, a gain of 15 dB, and a limit level of 10 dBm. At power up there is white noise at the amplifier input equal to -174 dBm/Hz; the thermal noise floor. This noise is amplified by 15 dB, delayed by the group delay of the SAW delay line (666 ns), and phase shifted by 360° by the oscillator loop, and adds to the noise at 777.75 MHz at the amplifier input. This process continues to add signal at the amplifier input until the amplifier reaches its limit level. Since only the noise at n x 360° adds at the amplifier input, the signal at the oscillator output is at 775.75 MHz and has noise sidebands determined by the loss and Q of the SAW, and the noise figure and output power of the amplifier.

Assume that the oscillator is oscillating at 777.75 MHz and the phase of the loop is changed by -120°. Therefore, the phase shift at 777.775 MHz is no longer 0°, but -120°. The oscillator will shift to a frequency that has a phase of +120° such that the loop phase is 0° (n360°). That frequency, based upon the SAW delay line phase in Figure 2 is 777.25 MHz. Thus, the oscillator frequency can be tuned along the SAW delay line phase slope by changing the loop phase shift.

Since the SAW delay line has only 360° of phase shift over its -3 dB bandwidth, the oscillator cannot attempt to oscillator at multiple frequencies or jump from one frequency to another. For example: if the delay line had 720° of phase shift over its bandwidth, there would always be two frequencies that would have n x 360° of phase shift around the oscillator loop. In this case the oscillator could startup at either frequency, or jump from one to the other, since both meet the oscillation criteria.

VCSO Description

A block diagram of a typical VCSO is shown in Figure 4. The oscillator loop consists of a loop amplifier, a SAW delay line, a voltage controlled phase shifter, and a frequency set phase shifter. An output buffer is used to isolate the oscillator loop from the external load circuit and to provide the desired type of output (sinusoidal, LVPECL, LVDS, etc.)

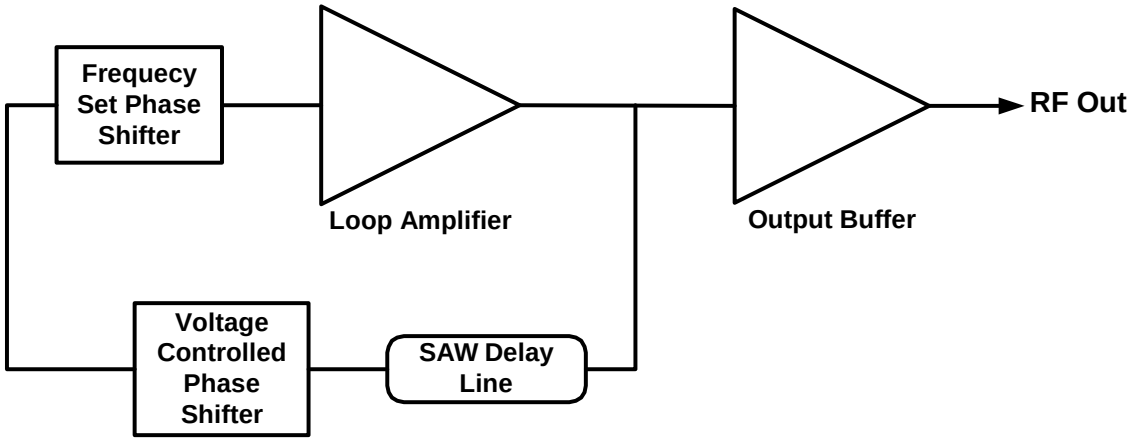


Figure 4 VCSO Block Diagram

The loop amplifier is a low noise wide band amplifier that has adequate gain at all desired oscillator frequencies and an output power level necessary to provide a low phase noise floor. The SAW delay lines are similar to that shown in Figure 2 and are generally in the 400 MHz to 1200 MHz frequency band. The voltage controlled phase shifter provides frequency tuning capability, and the frequency set phase shifter is used at VCSO alignment to accurately set the VCSO center frequency within the pass band of the SAW delay line.

IDT manufactures two types of VCSOs. One is a low cost VCSO that uses an IDT VCSO ASIC to provide the loop amplifier, output buffer, voltage controlled phase shifter and frequency set phase shifter functions in a single IC. The entire VCSO consists of the ASIC, SAW delay line, and a few passive components. This VCSO is available in a 5x7mm LTCC package and can provide two user selectable output frequencies. The VCSO output is a standard differential LVPECL.

The second type of VCSO is a discrete design built on a PCB. Most designs use 50Ω RF IC gain blocks for the loop amplifier and buffer amplifier. The voltage controlled phase shifter is a discrete RF design using two varactor diodes that has a very linear phase versus voltage characteristic. The frequency set phase shifter is similar with the varactors replaced by fixed capacitors.

The discrete VCSOs are larger and more costly than the ASIC based VCSOs. However, they have ultra low phase noise and can also integrate a transistor frequency multiplier to multiply the fundamental VCSO frequency to the 1000 MHz to 3000 MHz range.

Temperature Stability

The temperature stability of the VCSO is determined primarily by the SAW delay line and to a lesser degree by the relatively linear phase variation with temperature of the electronic circuit. The frequency change as a function of temperature of a quartz SAW delay line used in VCSOs is shown in Equation 1.

Equation 1: $\Delta Fppm = -.038(Ta-T0)^2$

Ta = ambient temperature
T0 = SAW turnover temperature

Figure 5 shows temperature characteristics of SAW delay lines having different turnover temperatures. Note the significant difference in frequency variation as a function of T0. The T0 of a quartz wafer is determined by the rotated Y cut angle. Once an angle is selected for a particular T0, T0 is very consistent from wafer-to-wafer. It is obvious from Figure 5 that the best stability is obtained with a T0 of 25°C.

If it wasn't for the phase variation with temperature of the electronics, all VCSOs would use SAW delay lines with a T0 = 25°C. The temperature coefficient (TC) of the electronic circuit causes the T0 of the oscillator to change from that of the SAW delay line. Since the TC of the electronics is nearly linear, the parabolic characteristic of the delay line is not significantly distorted, but the turnover temperature is shifted. In most cases T0 is shifted lower in temperature, since the phase shift of the electronics increases with temperature.

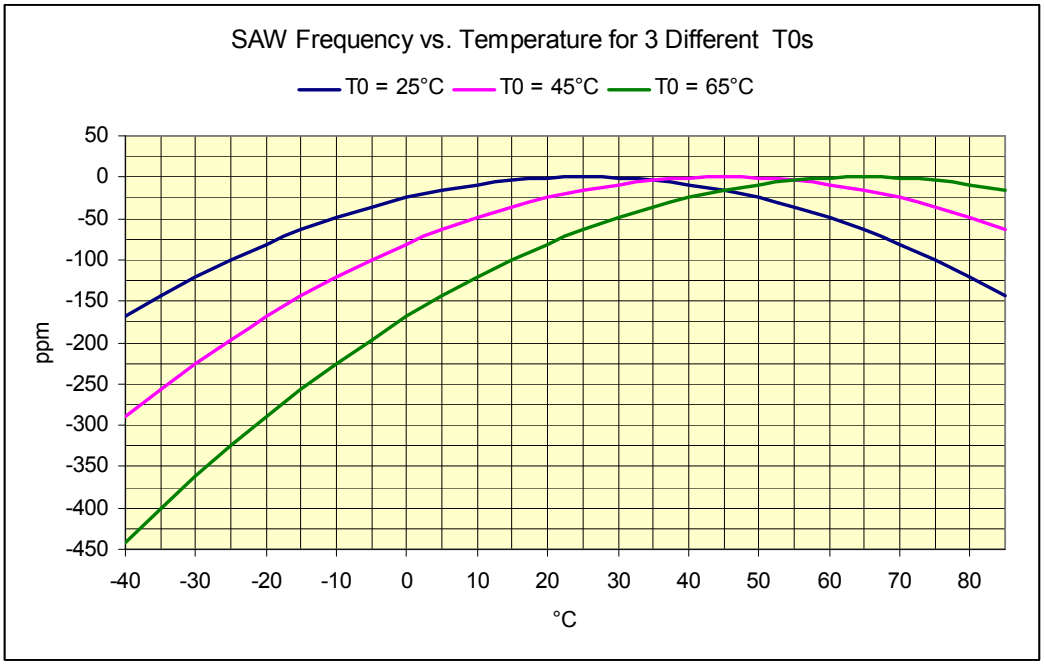


Figure 5 SAW Delay Line Frequency vs. Temperature,
T0 = 25°C (blue), T0 = 45°C (pink), T0 = 65°C (green)

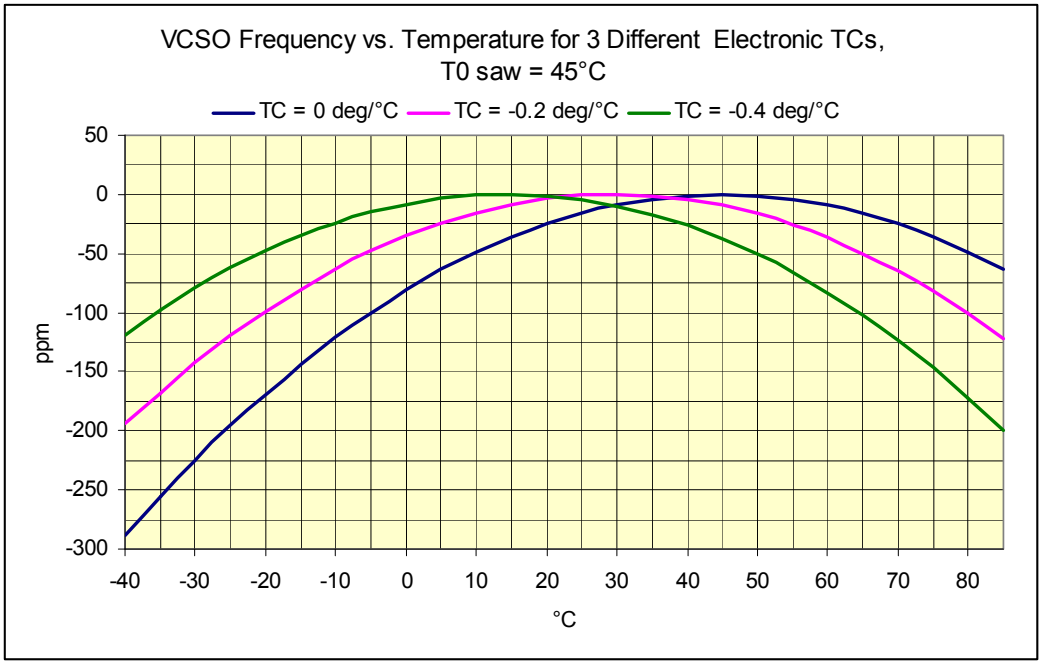


Figure 6 VCSO Frequency vs. Temperature, SAW T0 °C
Electronic TC = 0deg/°C (blue), -0.2 deg/°C (pink), -0.4 deg/°C (green)

The sensitivity of the VCSO turnover temperature on the electronic circuit TC is illustrated in Figure 6. The VCSO T0 is 45°C with a circuit TC of 0 deg/°C; 30°C with a circuit TC of -0.2 deg/°C; and 15°C with a circuit TC of -0.4 deg/°C. It is not uncommon to observe a VCSO unit-to-unit T0 variation of 10°C. The temperature characteristics of the SAW delay line are extremely constant so the variation is due to the electronic circuit and varies somewhat with phase shifter settings; the more phase shift in the VCSO loop, the greater the TC.

Phase Noise

One of the most important reasons for the use of VCSOs is their low phase noise at high fundamental frequencies. If the circuit and SAW delay line characteristics are known, the phase noise of a VCSO can be accurately predicted. This section will use well known phase noise equations to calculate the phase noise of VCSOs and evaluate its sensitivity to circuit parameters.

The well known Leeson's Formula[1] will be used to model the VCSO phase noise. Leeson's Formula is shown in Equation 2 and will be used to calculate the VCSO phase noise.

Equation 2. $L(f_m) = (10^{KNF/10})[1+(Fo/(2f_mQ))^2](1 + f_c/f_m)$

K_{NF} = Noise Floor in dBm/Hz
Fo = Oscillator output frequency
f_m = Offset frequency
Q = Oscillator quality factor (Fo/BW)
f_c = 1/*f* noise corner frequency

The first parameter to be calculated is the noise floor of the oscillator, K_{NF}. The noise floor will be calculated in dBc/Hz using the following equation referencing the VCSO in Figure 4. K_{NF} is really a calculation of the signal to noise ratio at the input of the loop amplifier and is calculated using Equation 3; again referencing the VCSO in Figure 4.

Equation 3. K_{NF} = -174 (thermal noise floor in dBm/Hz) - Pin_{SAW} + IL_{SAW} + IL_{VCPS} + IL_{FSPS} + NF_{AMP}

Pin_{SAW} = RF power at SAW input in dbm
IL_{SAW} = SAW insertion loss in dB
IL_{VCPS} = Voltage Controlled Phase Shifter insertion loss in dB
IL_{FSPS} = Frequency Set Phase Shifter insertion loss in dB
NF_{AMP} = Loop amplifier noise figure in dB

Table 1 shows typical values for the parameters of Equation 3 that will be used for initial phase noise calculations. The resulting VCSO noise floor is -169 dBc/Hz. Table 2 shows the initial parameter values that will be used to calculate the VCSO phase noise using Equation 2.

Table 1 VCSO Noise Floor Parameters

Parameter	Discrete VCSO
PN_T	-174 dBm/Hz
Pin_{SAW}	13 dbm
IL_{SAW}	10 dB
IL_{VCPS}	2 dB
IL_{FSPS}	2 dB
NF_{AMP}	4 db
K_{NF} dBc/Hz	-169 dBc/Hz

Table 2 VCSO Phase Noise Parameters

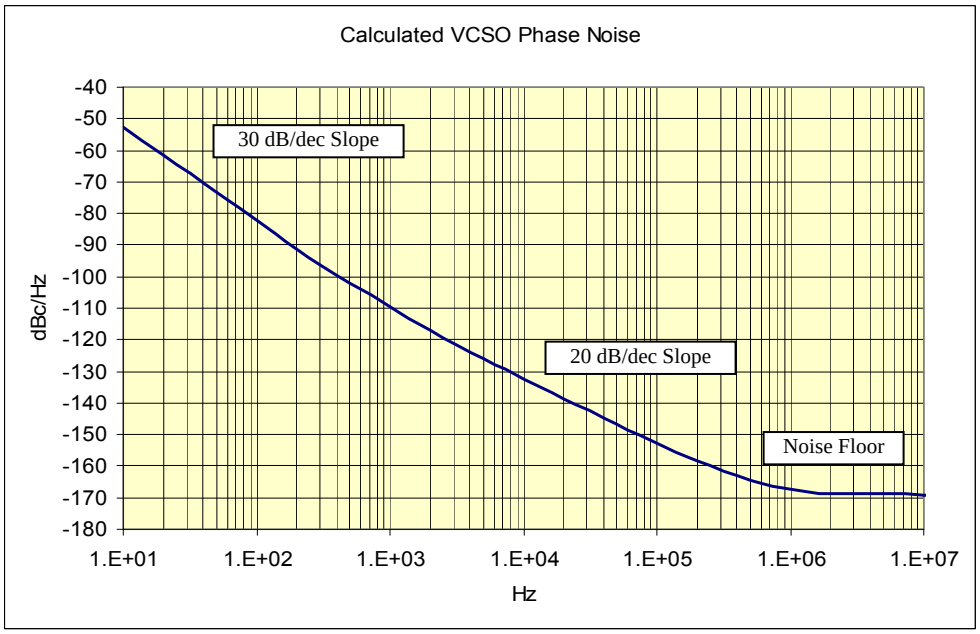
Parameter	Value
Fo	622 MHz
SAW BW	1.3 MHz
fc	5 kHz
KNF	-169 dBc/Hz

Figure 7 shows the VCSO phase that has been calculated using the parameters in Tables 1 and 2. This noise is typical of a discrete IDT VCSO. There are several points of interest in the phase noise plot. Note that at frequencies greater than 1 MHz, the phase noise is at the -169 dBc/Hz noise floor. Between 1 MHz and 10 kHz the phase noise increases from the noise floor at a slope of 20 dB per decade. The noise begins to increase from the noise floor at a frequency of ½ the SAW delay line bandwidth (750 kHz).

At frequencies lower than the 1/f noise corner frequency, the phase noise slope increases to 30 dB per decade. The example in Figure 7 has a 1/f noise corner frequency of 5 kHz and the transition to a 30 dB per decade slope is quite clear.

The 1/f noise corner frequency is a property of the amplifiers used in the VCSO oscillator loop and is a function of the device technology. For most bipolar processes it is in the 1 kHz to 5 kHz range, while FETs can have 1/f noise corner frequencies in excess of 1 MHz. For this reason, bipolar amplifiers are used in most low noise oscillator applications.

Equation 2 can be used to assess the effect of key VCSO parameters on the phase noise. In Figure 8 phase noise plots are shown with specific parameters changed one at a time.



Calculated using the Parameters in Tables 1 and 2 in Equation 2

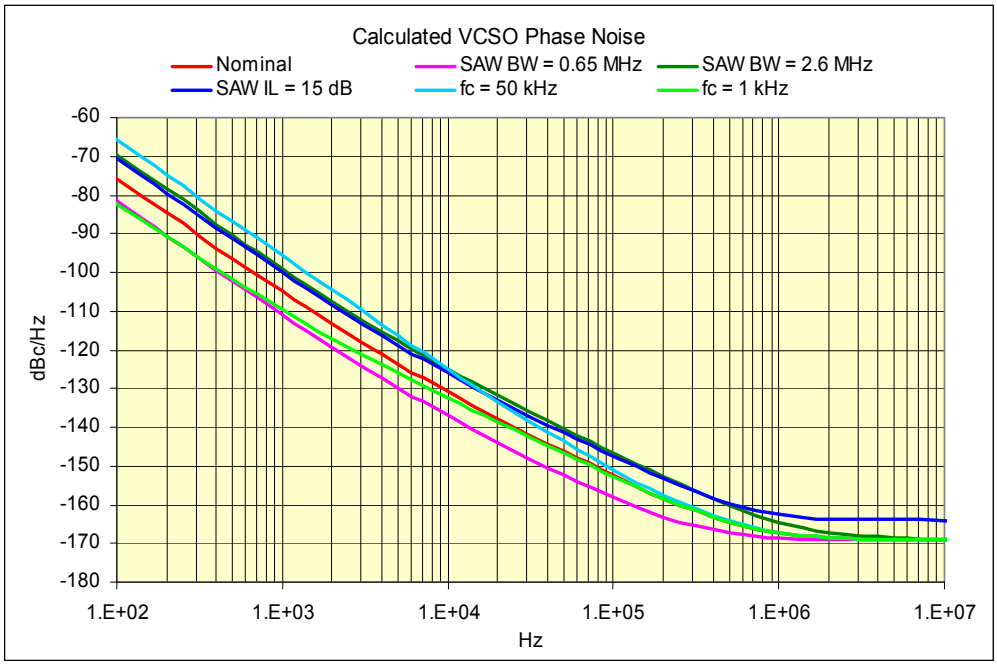


Figure 8 Predicted 622 MHz VCSO Phase Noise
Parameters in Tables 1 and 2 Varied Individually

The following observations can be made from the plots in Figure 8:

1. Decreasing the SAW bandwidth by a factor of 2 to 0.65 MHz (pink plot) lowers the phase noise by 6 dB but, leaves the noise floor unchanged. The nominal phase noise is shown in the red plot.
2. Increasing the SAW bandwidth by a factor of 2 to 2.6 MHz (dark green plot) increases the phase noise by 6 dB, but leaves the noise floor unchanged.
3. Increasing the SAW delay line insertion loss by 5 dB increases the phase noise by 5 dB, including the noise floor (blue plot). Increasing the insertion loss has the same effect as lowering the input power to the SAW delay line.
4. Increasing the 1/f noise corner frequency, fc, from 5 kHz to 50 kHz significantly increases the phase noise below 100 kHz (light blue plot).
5. Decreasing the 1/f noise corner frequency, fc, 5 kHz to 1 kHz significantly decreases the phase noise below 10 kHz (light green plot).

The plots in Figure 8 illustrate the relative importance of the various VCSO parameters that relate to phase noise. In order to minimize phase noise it is important to use low loss techniques in the design of the SAW delay line, and to design the delay line such that the bandwidth is the minimum necessary to provide the required tuning range; typically 2 times the tuning range. It is also important to use a semiconductor process that has a low 1/f noise corner frequency.

If a fundamental frequency VCSO is followed by a frequency multiplier the phase noise at the multiplier output is increased by 20xLog (N), where N = Fout/Fvcso.

IDT Integrated Circuit VCSOs and Discrete VCSOs

Figure 9 IDT 5x7mm Integrated Circuit VCSO and 15x20mm Discrete VCSO

IDT offers a family of single and dual frequency VCSOs that are available in a 5x7mm LTCC package. These VCSOs incorporate a custom IDT VCSO integrated circuit, an IDT low loss SAW delay line, and a few passive components. These VCSOs provide low phase noise, industry standard tuning range and footprint.

For applications requiring ultra low phase noise, IDT offers discrete VCSOs fabricated on an FR4 PCB. The extremely low phase noise is only possible in a discrete design because many of the compromises of an integrated circuit design are eliminated. In addition, the discrete VCSOs are available with a transistor frequency multiplier to provide output frequencies up to 3000 MHz. Discrete VCSOs are currently available in a 15 x 20 mm package. These VCSOs are single frequency VCSOs with sinusoidal outputs.

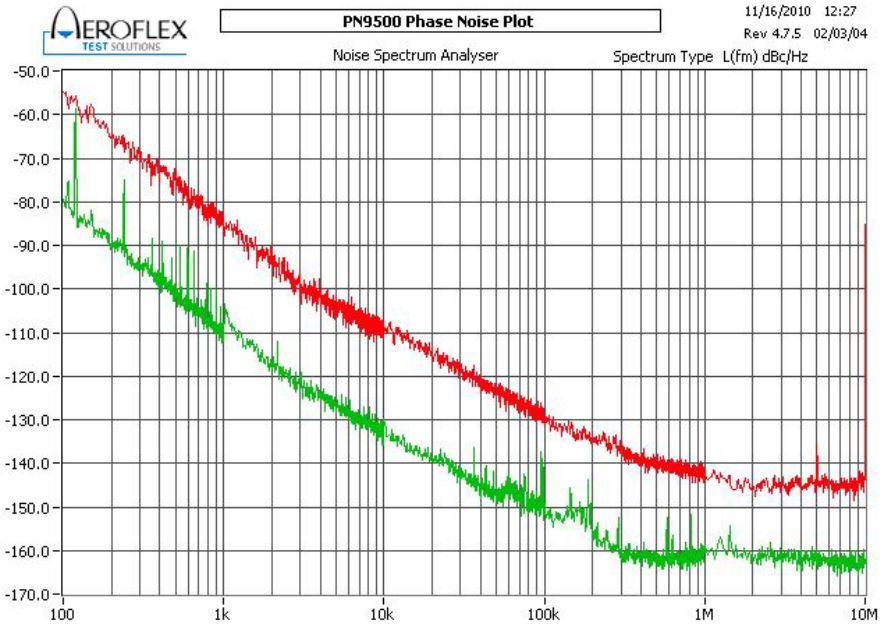


Figure 10 622.08 MHz Phase Noise: M685S02-AA 5x7mm IC VCSO (red) and M624-622.0800 15x20mm Discrete VCSO (green)

Phase noise of an ASIC VCSO and a discrete VCSO are shown in Figure 10. The lower phase noise of the discrete VCSO is quite apparent. Both VCSOs use the same SAW delay line, so the difference in performance relates to the RF VCSO circuitry. The -160 dBc/Hz noise floor of the discrete VCSO is that of the phase noise test set. The actual noise floor is lower than -165 dBc/Hz. ASIC VCSO has LVPECL outputs and the discrete VCSO has a 10 dBm sinusoidal output.

[1] Leeson, D. B., "*A Simple Model of Feedback Oscillator Noise Spectrum*", Proceedings of the IEE, vol. 54, pp 329-330, 1966

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