

RapidIO® Gen2 Technology

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Introduction

The wireless industry continues to look to the RapidIO® specification to address the needs of mobile users and increase the quality of service. The RapidIO Gen2 specification provides users with more usable bits per milliwatt while remaining backward compatible with the RapidIO Gen1 specification. This is accomplished not only by increasing raw bandwidth, but also by providing flow control facilities to manage short- and medium-term congestion and to avoid long-term congestion. The paper provides a description of the RapidIO Gen2 specification, a comparison against the PCI Express® (PCIe®) Gen 2 specification and describes how applications can benefit from using RapidIO Gen2. Lastly, it will provide a preview of the features and capabilities that IDT® will provide as part of the rich RapidIO ecosystem.

RapidIO Gen2

The RapidIO specification is a packet-based technology defined for endpoints, which originate and process packets and switches, which are used to connect endpoints. RapidIO is a layered specification, intuitively divided into a physical layer protocol, packet transport (routing) protocol and multiple protocols at the logical layer. Multiple logical layer protocols define different methods by which endpoints can exchange data. The transport layer defines how all RapidIO packets are routed through a RapidIO switch. The physical layer defines the electrical characteristics and link layer packet transfer protocol that all RapidIO endpoints and switches must follow to guarantee interoperability.

This layered-specification approach facilitates the RapidIO Trade Association's commitment to backward and forward compatibility of the specifications, enabling investments in RapidIO hardware and software to be efficiently leveraged by all members of the RapidIO ecosystem for multiple product generations. The value of this commitment has been proven by the addition of multiple backward-compatible/forward-compatible logical-, transport- and physical-layer extensions in the RapidIO Gen2 specification.

The RapidIO Gen2 physical layer remains compatible with the RapidIO Gen1 physical layer, which exchanges packets delimited by control symbols. Control symbols are also used to ensure reliable packet delivery and to perform physical-layer error recovery in hardware. The usage of control symbols has been extended as described in the Physical Layer Enhancements section below.

The RapidIO Gen2 logical layer maintains all the same capabilities of the RapidIO Gen1 logical-layer specification. Read, write and atomic memory-mapped transactions continue to be supported, as well as messaging and data streaming. The RapidIO Gen2 logical layer enhancements are aimed at improving overall traffic management and to react to congestion, to increase the effective use of raw bandwidth.

Physical Layer Enhancements

The physical layer is extended to support 5.0 Gbaud and 6.25 Gbaud lane rates, allowing a 4x RapidIO port to have up to 20 Gbps of usable bandwidth. The link width options are also extended from 1x and 4x, to include 2x, 8x and 16x. With five possible lane speeds and five possible lane widths, system designers are able to tailor a RapidIO port's raw bandwidth available to anything between 1 Gbps and 80 Gbps.

The widely used 8B/10B encoding scheme successfully used in RapidIO Gen 1 has been maintained in RapidIO Gen2. However, as lane frequencies increase, the protocol must change to support SerDes functionality necessary to maintain signal integrity in the face of increased attenuation, which is expected at higher frequencies. The RapidIO Gen2 physical layer has been enhanced to enable automatic transmit emphasis adjustment between link partners. The use of differential feedback equalization (DFE) is enabled by the RapidIO Gen2 physical layer. These aspects of the protocol have enabled an increase in maximum reach to 100cm of FR4 with two connectors. Also, the required bit error rate for RapidIO 5 Gbaud and 6.25 Gbaud lanes has improved to 1 in 1015 bits, matching industry norms for RapidIO Gen1 parts.

The RapidIO Gen2 physical layer protocol adds eight virtual channels to the RapidIO Gen1 prioritized flows for a total of nine virtual channels. Virtual channels are associated with output bandwidth allocations on a per-port basis, which guarantee minimum throughput for traffic with different quality-of-service requirements. Minimum throughput guarantees are an important tool for system designers faced with complex quality-of-service challenges that cannot be met with pure priority-based systems.

One significant quality-of-service challenge is information exchange that is so time-sensitive that it is better to discard packets rather than wait for error recovery. This is typically seen in voice or video traffic where loss of some packets has minimal impact in the quality of user experience, but where a time lag associated with waiting for packet retries could degrade the user experience. RapidIO Gen2 supports this traffic using virtual channels. Each virtual channel can be configured to support either the “Reliable Traffic” paradigm for guaranteed packet delivery or to use the new “Continuous Traffic” mode for time-sensitive traffic. Virtual channels configured to support Continuous Traffic will never retransmit a packet, ensuring time-critical data always makes predictable forward progress with guaranteed system latency.

The most-efficient networks optimize quality of service while maximizing network utilization. The RapidIO Gen2 specification has defined a “Virtual Output Queue Backpressure” mechanism that enables high network utilization while preserving quality of service. Information about congestion in the network is communicated using control symbols. This information can be used to reduce flows destined for congested areas of the network and to increase flows destined for uncongested areas. The comprehensive RapidIO flow control mechanisms ensure that the raw bandwidth available is utilized most efficiently. Typically, the Virtual Output Queue Backpressure mechanism is used to manage medium-term congestion, which lasts from tens to hundreds of microseconds.

Logical Layer Enhancements

RapidIO Gen2 retains the same read/write and messaging/data streaming capabilities that the RapidIO Gen1 ecosystem has implemented. RapidIO Gen2 logical layer enhancements enable implementation of network- and application-level flow control operations, which are easily supported in the hardware. Network-level flow control can be used to avoid or limit periods of congestion within the network to the short periods that can be handled by link layer flow control and the Virtual Output Queue Backpressure mechanism. Network- and application-level flow control are implemented using two packet formats: data streaming packet extended header and flow control packet flow arbitration protocol.

The data streaming packet format in the RapidIO Gen1 specification allowed multiple “extended header” formats to be defined in the future. The RapidIO Gen2 specification defines one option for this extended header, known as a Traffic Management (TM) packet. The TM packet format supports the paradigm of multiple producers sending to a single consumer, which are communicating through shared buffers. The producers are adding data to the buffer, while the consumer is removing data from the buffer. The consumer needs to control the producers to prevent buffer overflow. The producers need to inform the consumer about how much information the producers have available so that the consumer can prioritize among different producers.

The TM packet format supports three different methods for managing the shared buffer. “Basic” traffic management allows the consumer XON/XOFF control of producers—either a producer can send or it can’t. “Rate-based” traffic management extends the XON/XOFF control to allow the consumer to control the rate at which a producer is sending, speeding up and slowing down the producer as demands on the consumer change. “Credit-based” traffic management also extends the XON/XOFF flow control semantics to limit the amount a producer can transmit to what the consumer can accept, based on the issue of credits to the producer. These management methods can be applied to particular flows or groups of flows between producers and consumers. Even more important, the management methods may be used with the standard RapidIO multicast function to globally control flows handled by a particular consumer.

In the RapidIO Gen1 specification, flow control packets implemented XON/XOFF control capabilities for physical-layer congestion, intended for use by switches and endpoints to control congestion that lasts up to tens of microseconds. The RapidIO Gen2 specification extends this packet format in two ways: it defines XON/XOFF support for virtual channels and also defines the flow arbitration protocol. The flow arbitration protocol is used to request and grant resources within a system. The resources can be data streaming packets, reassembly contexts, mailboxes, semaphores or any other shared hardware or software resource that requires management within a system. The flow arbitration protocol can be supported inexpensively in software or through dedicated hardware support, enabling the efficient management of shared resources throughout the RapidIO system.

Comparing RapidIO Gen2 and PCI Express Gen 2

RapidIO Gen2 has many attributes that enable it to deliver the more usable bits per milliwatt than any other interconnect. Some of these points are discussed in this article: http://www.dspdesignline.com/howto/212701200;jsessionid=D4VFLB3R2G1LSQSNDLRSKH0CJUNN2JVN?_DARGS=/GLOBAL/electronics/designline/shared3/article/rating/showPoll.jhtml.

The remainder of this discussion focuses on the differences between the RapidIO Gen2 and PCIe Gen 2 specifications.

The RapidIO Gen2 and PCIe Gen 2 specifications have about the same number of port widths allowed—1x, 2x, 4x, 8x and 16x. The PCIe specification also allows for 12x and 32x port widths. However, PCIe Gen 2 only supports two possible lane speeds—2.5 Gbaud, and 5.0 Gbaud. RapidIO also supports 1.25, 3.125 and 6.25 Gbaud lane speeds. The additional lane speeds allows system designers to match the raw bandwidth of RapidIO Gen2 ports closely to their application requirements, optimizing the power required for data transfer.

PCIe Gen 1 and Gen 2 define the equivalent of the RapidIO transmitter-based flow control at the link level. RapidIO also allows receiver-based flow control. When only Virtual Channel 0 (VCO) (priority-based) traffic is active, the RapidIO receiver-based flow control almost always results in better throughput and latency than what PCIe can achieve.

PCIe Gen 2 has no equivalent to the RapidIO Gen2 virtual channels, even though PCIe Gen 1 and Gen 2 do define virtual channels. PCIe virtual channels operate much differently than RapidIO Gen2 virtual channels. In PCIe, virtual channels are preemptively scheduled. That is, PCIe treats a PCIe virtual channel number as a priority. The PCIe specification requires that traffic in higher-priority PCIe virtual channels must always be sent ahead of traffic in lower-priority PCIe virtual channels. In this way, the PCIe Gen 2 specification supports eight different priority levels for reads and writes. The VCO in RapidIO Gen1 and Gen2 also support eight priorities, but not all can be used for reads and writes. Practically speaking, it is rare to find support for PCIe virtual channels, whereas, in the RapidIO Gen1 ecosystem, four priorities are the minimum. The IDT RapidIO Gen2 components will commonly support eight different priorities and multiple virtual channels.

From a transport-layer perspective, RapidIO Gen2 and PCIe Gen 2 have not made significant changes from their first-generation specifications. PCIe Gen 2 still only supports tree topologies. The use of PCIe single-root I/O virtualization (SR-IOV) and multi-root I/O virtualization (MR-IOV) allows multiple trees to exist in the “same” system, and non-transparent bridging can enable separate “trees” to communicate. This is not a scalable solution. RapidIO Gen2 continues to be topology agnostic—any system topology can be supported. PCIe Gen 2 has caught up to RapidIO Gen1 by adding a multicast capability. Since the PCIe Gen 2 packet routing is address based, however, this offers less capability than RapidIO Gen1.

At the logical layer, the disparity between RapidIO Gen2 and PCIe Gen 2 becomes clearer. PCIe Gen 2 has added some features, such as atomic transactions. The RapidIO atomic transaction support remains much richer than that for PCIe Gen 2. PCIe Gen 2 still has no support for messaging semantics, so it cannot match the RapidIO Gen2 support for messaging and data streaming.

From a flow-control perspective, PCIe Gen 2 cannot match the comprehensive flow control capabilities of RapidIO Gen2—efficient link-level flow control with optimal control path latency, XON/XOFF flow control for short-term events, network-level flow control to avoid congestion and Virtual Output Queue Backpressure. These flow control capabilities enable the engineering of predictable, low latency for different traffic classes, even in complex networks with rapidly varying traffic patterns. This and the guaranteed bandwidth of the RapidIO Gen2 virtual channels are beyond the capabilities of PCIe Gen 2.

Applications for RapidIO Gen2

Wireless Baseband

Wireless base stations are the key application that drove the adoption of RapidIO. The architecture of wireless baseband processing inherently lends itself to the capabilities of RapidIO in that it uses a cluster of peer-to-peer networked processing elements. This is typically combinations of field programmable gate arrays (FPGAs), digital signal processors (DSPs) and application-specific integrated circuits (ASICs). RapidIO switches are used to pass large quantities of data between processing elements. In wireless baseband, there is the additional constraint of minimizing end-to-end latency and jitter. This makes the traffic management capabilities, latencies and performance of RapidIO Gen2 solutions ideal for wireless.

Next-generation wireless base stations, such as those used to implement 3G, 3G LTE or WiMAX networks, are driven by a few key requirements. They must:

- Maximize the number of subscribers per antenna array/base station
- Support more data bits per subscriber in the form of data and video (beyond narrowband voice)
- Provide real-time data video and voice aggregating to beyond 1 Mbps per subscriber
- Minimize power consumption

In addition to the above requirements, which apply equally to 3G and 4G technologies, more onerous constraints are placed specifically on 4G technologies, such as 3G LTE and WiMAX. These include:

- More data per subscriber, up to 100 Mbps
- More processing per data bit per user by FPGA/ASIC/DSP cluster
- Higher-speed handoffs between base stations
- More onerous Orthogonal Frequency-Division Multiple Access (OFDMA) Physical Layer Protocol (PHY)-based processing compared with current 3G platforms

Figure 1 shows a conceptual block diagram for a wireless base station. RapidIO is typically deployed on the baseband cards and the switch cards. The switch card can be used to pass antenna data to processing elements on baseband cards. This might be in a native-streaming interface off the radio frequency (RF) cards, such as Open Base Station Architecture Initiative (OBSAI) or Common Public Radio Interface (CPRI), or it may be converted to RapidIO and packetized, for example, using an IDT CPRI to RapidIO Functional InterConnect (FIC). The switch card can then pass the data to the baseband cards using the multicast function of the RapidIO switch.

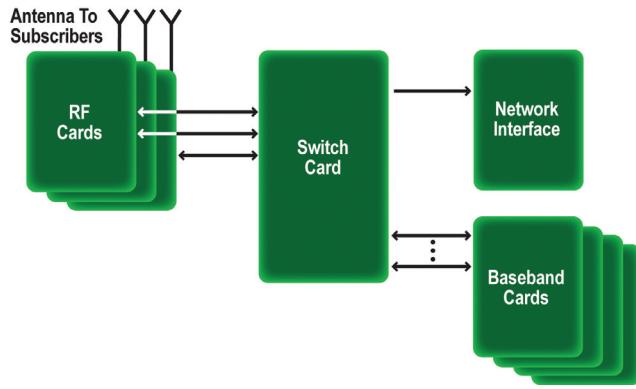


Figure 1. Conceptual block diagram for a wireless base station

Several features of RapidIO Gen2 are used to make the implementation of high-performance switching cards to support 4G wireless easier for system original equipment manufacturers (OEMs). These features apply equally to wireless, military and video applications. Some of the most applicable features of RapidIO Gen2 for these switch cards include:

- Advanced flow control capabilities at the link layer and network level
- Low latency and low jitter distribution of system events
- Virtual channelization and bandwidth allocation
- Support for Reliable Transmission mode and Continuous Traffic mode to ensure maximum performance for time-sensitive and non-time-sensitive traffic across complex backplanes
- Higher baud rates per link
- Lower power per 10 Gbps of data

On the baseband cards (see Figure 2 and Figure 3), the processing elements extract the actual data or voice signals out of the combined stream, leveraging the processing capabilities of FPGAs, DSPs and microprocessors to implement multiple tasks, including OFDMA PHY processing as well as Verterbi and Turbo decoding for voice and data processing.

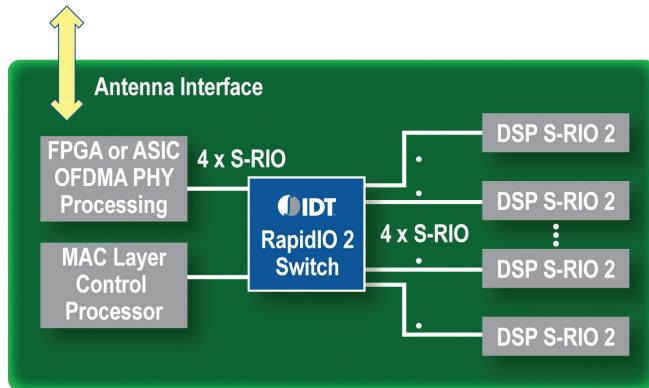


Figure 2. Sample baseband card block diagram

This sequence of processing tasks has already been proven in production systems. System OEMs have developed FPGAs or ASICs with RapidIO 1.3 interfaces to accelerate many processing functions and are now moving to support RapidIO Gen2 rates. DSP vendors have hardened a number of baseband processing tasks in embedded accelerators to improve performance and enable wireless system OEMs. They are all members of the RapidIO Trade Association who have ratified the RapidIO Gen2 standard.

Multiple RapidIO OEMs are members of the RapidIO Trade Association Steering committee and have driven the evolution of RapidIO Gen2 to support the needs of 4G networks.

With the development of 4G systems (WiMAX and 3G LTE), the widespread usage of these RapidIO Gen2 features is expected in baseband:

- Long-reach 100 cm 2 connectors across large backplanes or between chassis for system expansion
- Extensive use of 6.25 Gbaud links to pass more data between processing elements or to reduce the number of serial links between processing elements
- Lower switch power consumption per port, enabling more processing per milliwatt per subscriber
- Advanced traffic management features and water marks to maximize system performance, enhancing the end user broadband experience
- Use of virtual channels to guarantee bandwidth for specific channels and the application of continuous traffic mode for voice and video data where dropping packets is acceptable, but retries that are used in Reliable Traffic mode are not.



Figure 3. Actual baseband card

Military

RapidIO has received widespread adoption in military and critical embedded systems during the past five years. Today, RapidIO is used extensively in real-world military deployments, leveraging its rich set of features and proven reliability. RapidIO is ideal for the implementation of large peer-to-peer networks of microprocessors and FPGAs typically found in radar, sonar, flight control and navigation systems. Figure 4 is an example of one of these payload cards with multiple processors.

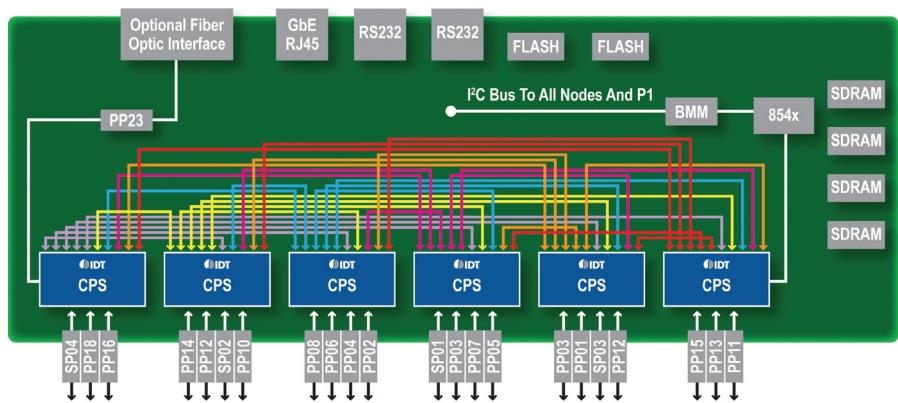


Figure 4. Sample payload card with multiple processors

The VMEbus International Trade Association (VITA) 41 and 46 standard uses RapidIO in the backplane, complimenting the legacy VersaModule Eurocard (VME) interconnect in a variety of VPX systems today. The same features that make RapidIO a natural fit for wireless make it an excellent interconnect for these large processor cluster-based applications found in today's technology-driven battlefield. The reliability features of RapidIO have been instrumental to its adoption in this market.

Today's systems are based on RapidIO 1.3, but all OEMs for these systems that target a variety of defense programs are pushing the silicon vendors in the RapidIO Trade Association for the next node of performance and value-added logical- and transport-layer features that will improve the performance of end applications.

Initially, the VITA standards leveraged RapidIO on cards between processing elements as shown earlier in Figure 4. These cards would then be "aggregated" with four x4 RapidIO links to the backplane, resulting in a mesh of up to five cards.

Obviously, the mesh network presents some limitation to the scalability of the overall solution as adding more cards becomes impossible with this distributed switching approach. To add more cards, centralized switching is needed, be it single-star or dual-star networks for redundancy. Today, military single-board computing vendors are looking at switching cards with connections of 20 or more x4 links to "payload cards." The initial deployment of these 20+ port switch cards used large clusters of RapidIO 1.3 switches.

Moving to RapidIO Gen2 with larger port count switches, faster links, better flow control mechanisms, virtual channels and other feature enhancements, the implementation of complex switches will be substantially simplified, improving performance at the system level.

In many of these military applications, the key elements to a superior end-user experience are based on the following:

- The sampling rate of raw data (for example, Radar Pulse Rate Frequency) and the Nyquist sampling rate
- The size of each frame to be processed in pixels
- The number of frame updates per second
- Keeping up with the actual speed of the aircraft in real time for airborne systems

As any of these requirements increases, the number of FPGAs or microprocessors in the system must be increased, with faster low latency links between processing elements. The reality is that the performance of these systems, to date, has been limited by processor capacity, power consumption and interconnect bandwidth/speed.

These systems require more frame updates per second, providing smoother video, and more pixels per frame, providing better resolution. In addition, they require larger frame sizes, allowing for the coverage of much larger swaths of terrain with the sensor system.

RapidIO Gen2 has been actively pushed by vendors developing the latest high-performance systems for military programs because the processing needs grow exponentially as any of the above requirements increase linearly.

RapidIO Gen2 has many features that enable payload cards and switch cards in military systems, including:

- Large 4x port count switches
- Baud rates per link up to 6.25 Gbaud, doubling RapidIO 1.3
- Low latency and low jitter distribution of system events
- Advanced flow control capabilities at link layer and network level
- Virtual channelization and bandwidth allocation
- Support for Reliable Transmission mode and Continuous Traffic mode to ensure maximum performance for time-sensitive and non-time-sensitive traffic across complex backplanes
- Lower power per 10 Gbps of data
- 100 cm, 2 connector reach support.
- Support for mesh and dual-star topologies

Video

RapidIO saw widespread adoption in the video market during the deployment of RapidIO 1.3 silicon. RapidIO was used in high-end video conferencing systems, TelePresence™ and a variety of image processing applications, such as medical imaging systems. All of these applications required large clusters of DSPs or FPGAs for video frame encoding/decoding or for image processing/transform operations (see Figure 5).

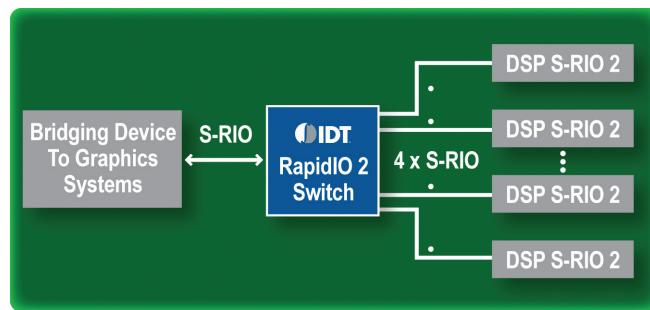


Figure 5. Typical video hardware implementation

The requirements of video and imaging systems are driven by the following key application attributes:

- High-definition video
- More frames per second
- Larger frames/pixels per frame
- More processing per frame
- More links at higher speeds
- Supports larger DSP clusters
- More multicast masks
- Lower latency for real-time applications
- Higher performance multicast
- A means to communicate from an RapidIO-enabled DSP cluster to a PCI or PCIe back-end network

As the number of frames to be processed increases, the size of an individual frame increases or the frames per second increases, the complex of signal processing semiconductors increases to support the system requirements. Growing the requirements of the system in any dimension effectively has a cubic impact on the “volume” of overall signal processing needs.

In most video systems, these frames must be typically put through the following stages:

- Decompress
- Scale
- Distribute
- Process
- Combine
- Compress

The less time spent distributing and combining frames means more performance available to keep up with a real-time feed of high-definition video with large frame sizes and high update rates. RapidIO Gen2 offers many feature enhancements that enable this. Improving the performance of multicast over RapidIO 1.3 is the most important feature that enables the high-end video systems. Coupling this with non-blocking switches that support up to 20 Gbps of raw bandwidth full duplex per port means the ability to support larger DSP clusters in real time to do the six steps identified earlier. With higher-performance RapidIO Gen2-enabled DSP clusters and traffic passing between them using multicast, the ability to manage traffic using end-to-end flow control at both the physical and logical layer will become more important than in RapidIO 1.3.

High-end video applications will use multiple processing cards aggregated with large non-blocking switch cards across high-performance backplanes, leveraging the 6.25 Gbaud rates per link. Again, the non-blocking nature of the latest Gen2 switches, combined with the RapidIO traffic management features that leverage virtual channels and Continuous Transmission mode, will be ideal to implementing systems that are obviously real-time and both latency and jitter sensitive. Finally, the ability of designers to use tools, such as on-die scope to establish clean eye diagrams across long backplanes over 2 connectors and 100 cm reach, will ensure ease of design, deterministic performance and faster time to market.

In today's RapidIO 1.3-based systems, IDT offers a hardware means to bridge directly from a DSP or FPGA cluster to a PCI network using the Tsi620. In addition to the above, it is possible to go from RapidIO 1.3 to PCIe Gen 1 using a combination of the Tsi620 and the Tsi384 PCI-to-PCIe bridge. This solution can be coupled with the vast array of IDT PCIe switches for a complete end-to-end video solution. As we move forward to RapidIO Gen2, IDT is working on bridging solutions that will enhance the existing 1.3 capabilities for the video market.

Architecting Other Systems

Architecting a new system, even with a proven technology, such as RapidIO, is a difficult technical challenge. IDT supports two approaches when assisting customers who need to answer difficult architectural questions.

The first approach is through prototyping using the extensive RapidIO board and software ecosystem, allowing different system concepts to be tested in the lab before building the real system. This approach is commonly used by those who are first learning about RapidIO and want to get hands-on experience to become comfortable with the technology.

Sometimes, though, an even simpler (or less expensive) "proof of concept" is needed to demonstrate system feasibility. In this case, customers can make use of the IDT RapidIO System Modeling Tool to investigate the performance characteristics of their proposed system. The RapidIO System Modeling Tool will support the IDT RapidIO Gen2 switch family offering, as well as the Tsi switch family of RapidIO Gen1 parts, to enable customers to choose which particular RapidIO switch best meets their needs.

Perhaps more importantly, the RapidIO System Modeling Tool allows customers to investigate the impact of different processing algorithms on the RapidIO fabric. The tool has been trusted by major OEMs to provide "proof of concept" for both hardware and software aspects of the system. The RapidIO System Modeling Tool enables customers to architect systems using RapidIO Gen1 parts and to understand how to increase the capabilities of those systems using RapidIO Gen2.

IDT RapidIO Gen2 Product Roadmap

IDT continues to invest strongly to meet the demands of the rapidly growing RapidIO market. IDT has combined its own Central Packet Switch (CPS) family of Gen 1 RapidIO switches and endpoint devices with the highly successful Tundra Tsi family of Gen 1 switches to build the broadest portfolio of switches. As part of its roadmap, IDT has also combined Tundra's Gen2 developments with its own to create a deep and rich product offering. That roadmap includes a robust family of Gen2 switches, complemented by RapidIO Gen2 endpoint intellectual property (IP) and bridging solutions.

RapidIO Switch Roadmap

The IDT RapidIO Gen2 switch roadmap builds upon the success of its Gen1 CPS and Tsi line of devices—taking the best of these devices and building on them to meet Gen2 performance requirements. The new switches will offer next-generation levels of performance while simultaneously reducing the overall power per Gbit transferred. Initial offerings will double the raw throughput of today's highest performing Gen 1 switches while only consuming approximately 300 milliwatt for every 10 Gbps of data transferred.

Gen2 Switches

To meet next-generation performance requirements, the Gen2 switches were enhanced in all major functional areas, including the switch core, the protocol stack and the SerDes blocks. The entire switch portfolio, including all the aforementioned functional blocks, are fully developed, designed and supported by IDT.

The next-generation switches provide even greater debug capability, from improved PRBS generation and checking capabilities, several loopback modes, the aforementioned on-die scope capabilities, run-time BER measurements with any RapidIO endpoint, enhanced counters and performance monitors, and a variety of built-in self-test modes. Combined, the features allow faster system bring-up, hardware signal integrity characterization, debug, system performance optimization and failure analysis. Ultimately, this means RapidIO-based designs get to market faster.

Switch Fabric

The Gen2 switch core is a third-generation fabric from IDT. It is a non-blocking fabric supporting line-rate throughput from all ports at up to 20G of throughput per port. The portfolio offers enhanced features for congestion management for unicast and multicast traffic. The number of multicast flows has also been increased for the Gen2 devices, allowing more robust support for video and imaging applications, among others.

The fabric provides configurable scheduler modes, allowing the user to ensure fairness per priority and flow—on a per-packet basis or on overall data transferred.

Next-generation packet buffer management algorithms are employed to ensure optimum utilization of the fabric under complex traffic flows. The implementation employed improves the availability of buffer space by dynamically adjusting according to run-time traffic, efficiently accommodating multi-priority traffic of any traffic shape.

Gen2 SerDes

To meet the RapidIO Gen2 physical layer enhancements, the IDT internally-developed Gen2 SerDes has been radically enhanced over the Gen1 offering. It has been purpose-built to provide 6.25 Gbaud per lane with transmitter- and receiver-based equalization to support transmission over 100cm FR4 plus two connectors with a Bit Error Rate (BER) of 10-15. To support analyzing signal integrity, on-die scope is employed, which allows viewing the received waveform before and after receive equalization. This can be performed on any arbitrary waveform, such as on a stringent pseudo-random bit sequence (PRBS) pattern, or at run-time on an active RapidIO link. Thus, the user can quickly analyze signal integrity at the receiver to assist in characterizing a channel in a lab setting or check a signal in the field after hot-swapping a Field Replaceable Unit (FRU)—without the need for error-prone mid-bus probing with a high-end oscilloscope.

RapidIO Gen2 Protocol and Ports

The initial IDT Gen2 switch offerings will support 1x, 2x and 4x ports at up to 20 Gbps, effectively doubling the raw bandwidth. These port configurations will meet the vast majority of application requirements and are also aligned with the majority of Gen1 devices on the market today.

The IDT Gen2 offerings are compliant with the optional Error Management Extensions of the RapidIO Gen2 specification. This functional set allows RapidIO error event detect, capture and reporting. Since it is a specification standard, standard software can be written in support of fault-management, hot-swap support and congestion management, among others.

Error Handling was standard in the IDT Gen1 Central Packet Switch (CPS) family of devices and proved invaluable for debug of error events. Error Handling increases the resolution and types of errors that can be captured and reported, and provides enhanced debug capabilities beyond the RapidIO specification.

Feature Offerings

The Gen2 switch offerings from IDT support a rich feature set. All offerings support the aforementioned fabric, protocol and SerDes capabilities. The CPS Gen2 family of devices is the foundation of the switching portfolio. They offer cost-effective, next-generation performance.

In addition to standard features, IDT is implementing a family of virtual channel-enabled devices. With its per-virtual channel guaranteed bandwidth provisioning and continuous transmission, this family will support next-generation Quality of Service (QoS) demands, including real-time support for multi-media applications. This is ideal for switch-to-switch links or for endpoints supporting virtual channels. These switches incorporate IDT-proprietary “Virtual Channel Migration” features that will allow Gen1 devices and Gen2 devices that do not natively support virtual channels to leverage the virtual channel capabilities through the switch fabric.

The upcoming IDT Gen2 switches also support lane polarity swap and lane swap capabilities, allowing the printed circuit board (PCB) designer to minimize vias and shorten trace lengths. This allows clean trace layout to ensure best possible signal integrity, which is key to supporting the next-generation lane rates.

The IDT CPS Gen1 packet trace and filter capabilities enabled ultra-high reliability design by allowing designers to block particular packet types on different switch ports. In this way, malicious entities were locked out of a system. The Gen2 product line has a variant that adds further features for ultra-high reliability design, including standards-based encryption.

RapidIO Gen2 Endpoint IP

Complementing the broad Gen2 switch portfolio, IDT offers RapidIO Gen2 endpoint IP. Developed, tested and supported by IDT, interoperability is ensured with the IDT switch portfolio.

The IP will also support up to 20 Gbps line-rate throughput on a 4x port, with 2x and 1x ports also supported. As with the IDT switches, the endpoint supports RapidIO Error Management extensions. It has features allowing seamless hot-swap and error recovery.

Validating the IDT leadership in RapidIO IP, the Gen2 endpoint has been selected by multiple endpoint providers, including Texas Instruments, which has selected the IP for next-generation digital signal processors (DSPs). The endpoint IP can be delivered for 65 nm and lower, and will be tested for interoperability pre silicon against the RapidIO Trade Association Bus Functional Model as well as the IDT RapidIO Gen2 switch portfolio.

Putting It All Together

Building on and leveraging the highly successful Gen 1 Tsi and CPS lines of switches and endpoints, IDT leads the way with RapidIO Gen2 switches and endpoint IP. These products are developed and supported fully by the combined forces from IDT and the former Tundra, ensuring the best-of-the-best in solutions and support.

The devices and IP will be complemented by the combined world-class documentation, software, models (power calculators, BSDL, IBIS and high-speed PCB design kit), evaluation platforms, third-party commercial off-the-shelf solutions and software support—building upon what is already available for the Gen1 devices. The IDT System Modeling Tool, which allows modeling system traffic and optimizing performance through switch fabric, will be extended to support Gen2 switches in addition to the existing Gen 1 support.

These solutions will provide next-generation performance with lower power per gigabit. As such, they will enable WCDMA, 3G+, 3G LTE and WiMAX, and next-generation medical and military imaging, video conferencing, industrial controls, military communications, and storage. This will be achieved while also significantly reducing system-level cost—both in reduced bill of materials as well as operational costs.

The improved debug features and combined expert IDT engineering support will minimize time to getting systems into production.

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