

致尊敬的顾客

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2010年4月1日
瑞萨电子公司

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高速 CMOS 逻辑 HD74HC 系列

应用说明

1. 输入保护电路

高速 CMOS 逻辑采用 Si 栅极工艺，具有比传统的 Al 栅极 CMOS 逻辑更薄的栅氧化层，并且由更细微的图形构成。因此，为了防止从输入引脚进入的电涌，需要保护栅极的输入保护电路。如图 1(a) 所示，因为在 Al 栅极 CMOS 逻辑中将扩散电阻用作输入保护电阻，所以电涌产生的输入过电流直接流入电源，有可能破坏保护二极管。相反地，如图 1(b) 所示，在高速 CMOS 逻辑中，通过将多晶硅用作输入保护电阻，使输入保护电路对于输入过电压而言，起了电流限制元件的作用。

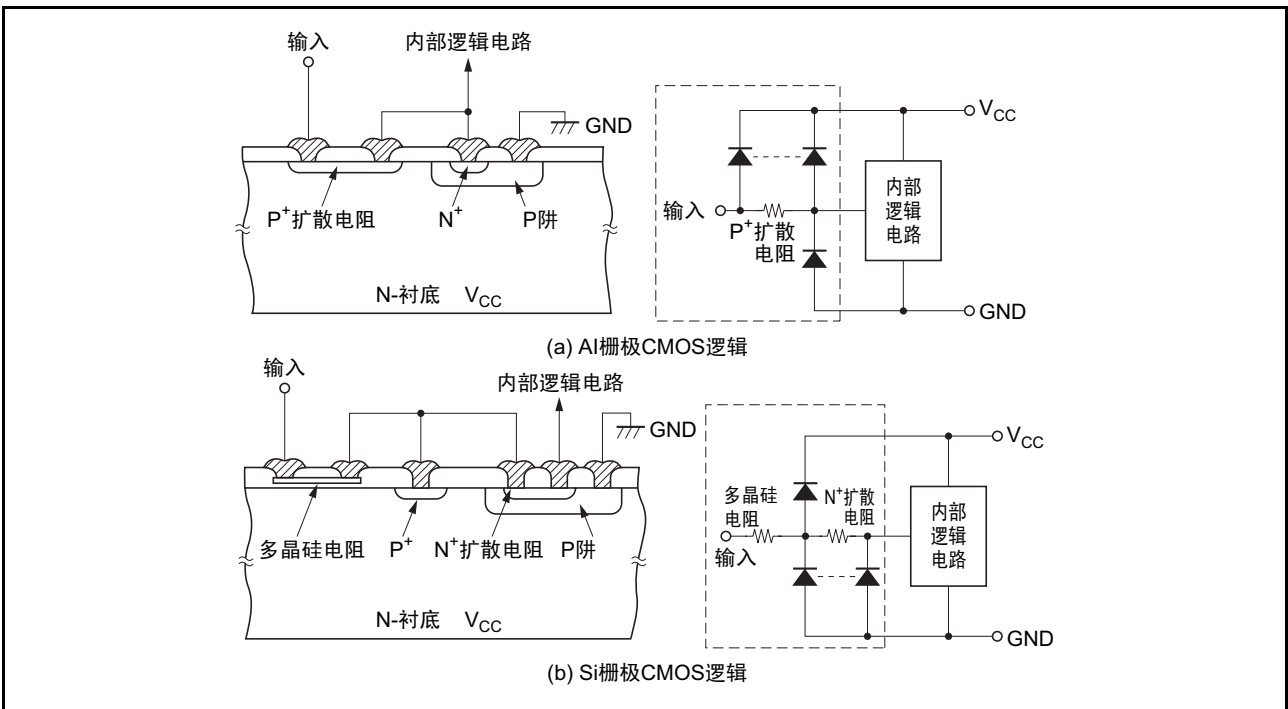


图 1 输入保护元件和等效电路

2. 抗静电击穿能力

使用图 2 的试验电路所示的电容器充电法对抗静电击穿能力进行评价。另外，考虑到人体的静电电容，假设电容器的电容为 200pF。瑞萨集成电路各产品系列的抗静电击穿能力的例子如图 3 所示。高速 CMOS 逻辑的抗静电击穿能力至少为 ±200V，达到了 LS-TTL 同等水平以上的程度。

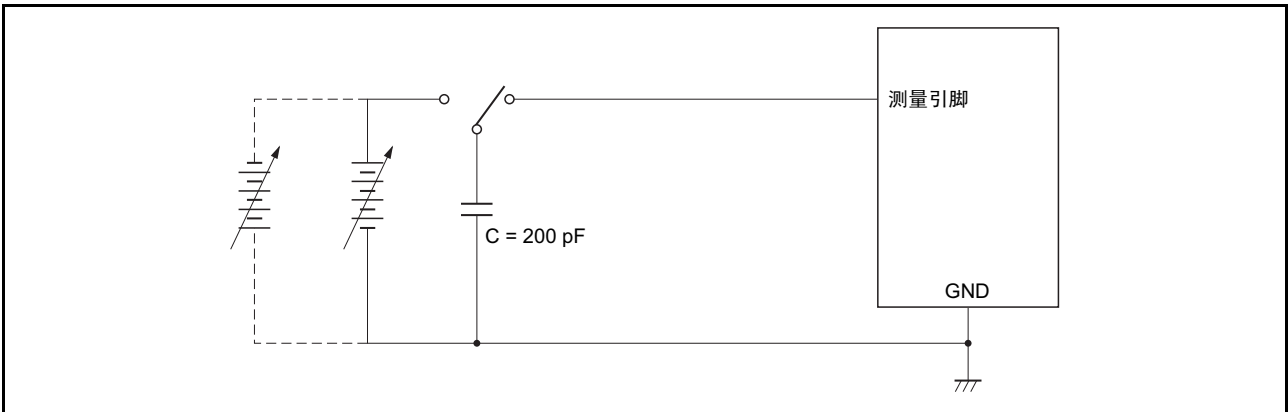


图 2 抗静电击穿能力的试验电路

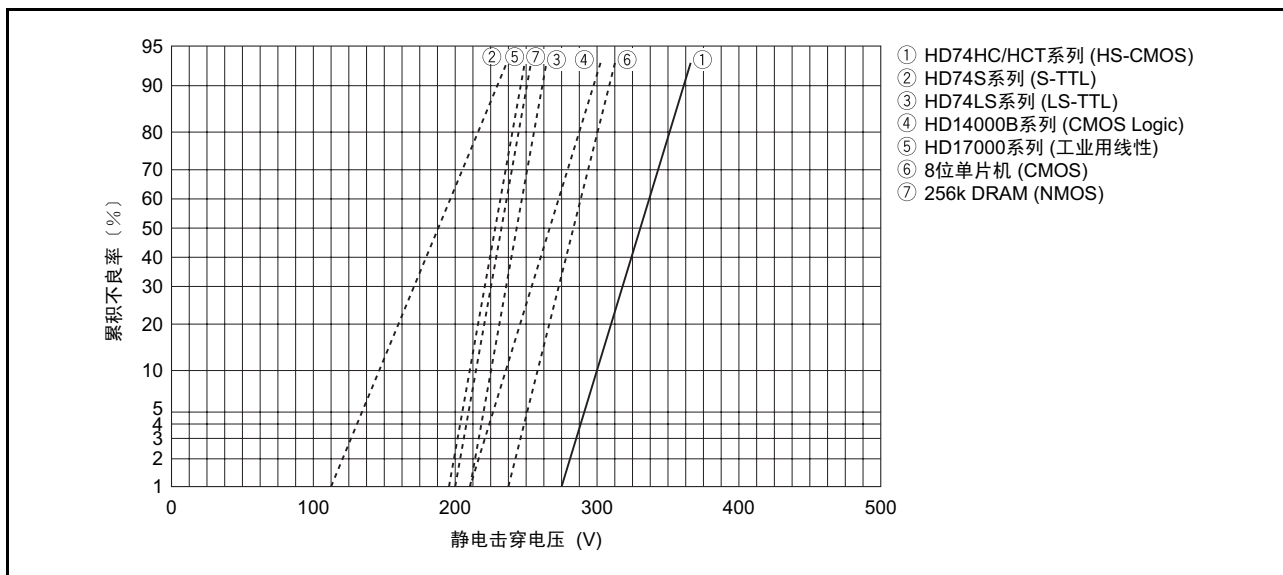


图3 各产品系列的抗静电击穿能力

3. 闩锁

3.1 闩锁现象

在CMOS逻辑的结构上，闩锁是无法避免的现象。因为在CMOS电路中，PMOS晶体管和NMOS晶体管在同一个芯片内，形成NPN晶体管和PNP晶体管，这2个晶体管相互连接形成PNPN结构，构成寄生晶闸管（参照图4）。如果在IC工作时从输入引脚或者输出引脚侵入过大的噪声，寄生晶闸管就会导通，异常电流从电源引脚流到GND。如果切断电源就能恢复正常，但是有时芯片内的A1布线会熔断，甚至会破坏元件。

闩锁现象的防止对策有：

- (1) 拉开PMOS晶体管和NMOS晶体管的距离。
- (2) 通过在布局方面下工夫，将形成寄生晶闸管的PNP晶体管和NPN晶体管之间的电通路切断。
- (3) 用绝缘物隔开各MOS晶体管，防止寄生晶闸管的形成。

瑞萨高速CMOS逻辑采用了上述第2种对策。

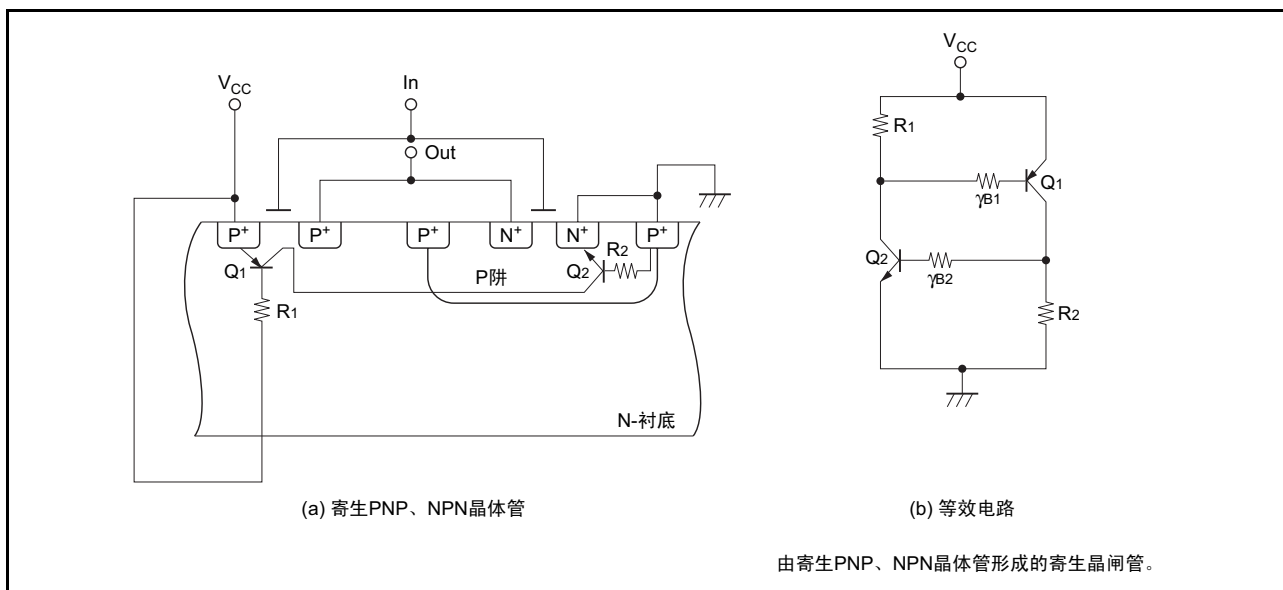


图4 寄生晶闸管

3.2 耐门锁

用图5的试验电路所示的外加电压法对耐门锁进行评价。瑞萨高速CMOS逻辑的耐门锁的试验结果例子如表1所示。高速CMOS逻辑的门锁开始电压至少为±300V，在实际使用时不会出现问题。

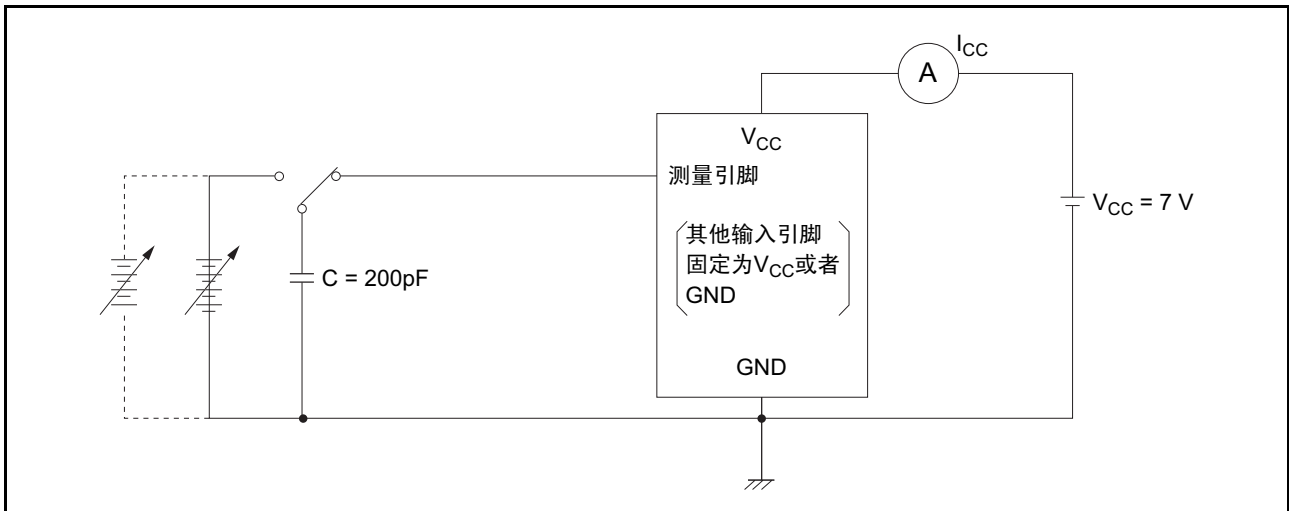


图5 耐门锁的试验电路

表1 门锁开始电压的测量结果

| | 门锁的开始电压 |
|----|---------|
| 正向 | ≥ 300V |
| 反向 | ≥ 300V |

4. 电特性

高速CMOS逻辑电特性的典型项目如下所示。

4.1 直流特性

(1) 逻辑阈值电压 (V_{TH})

为了使噪声容限达到最大，瑞萨高速CMOS逻辑（HD74HC型）的逻辑阈值电压（V_{TH}）基本上是V_{CC}的1/2。输入/输出特性如图6所示。

(2) 输出电流特性

瑞萨高速CMOS逻辑的I_{OH}特性和I_{OL}特性具有对称性。因此，即使连接比较大的负载电容，也基本上保证了t_{PLH}和t_{PHL}的平衡。输出电流特性如图7和图8所示。

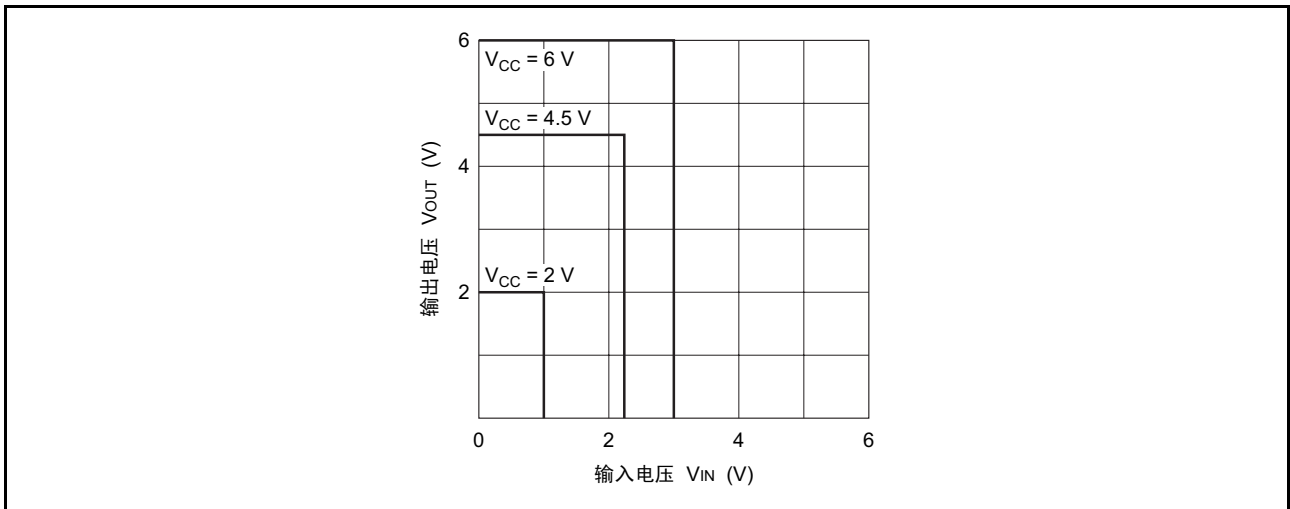


图6 输入/输出特性

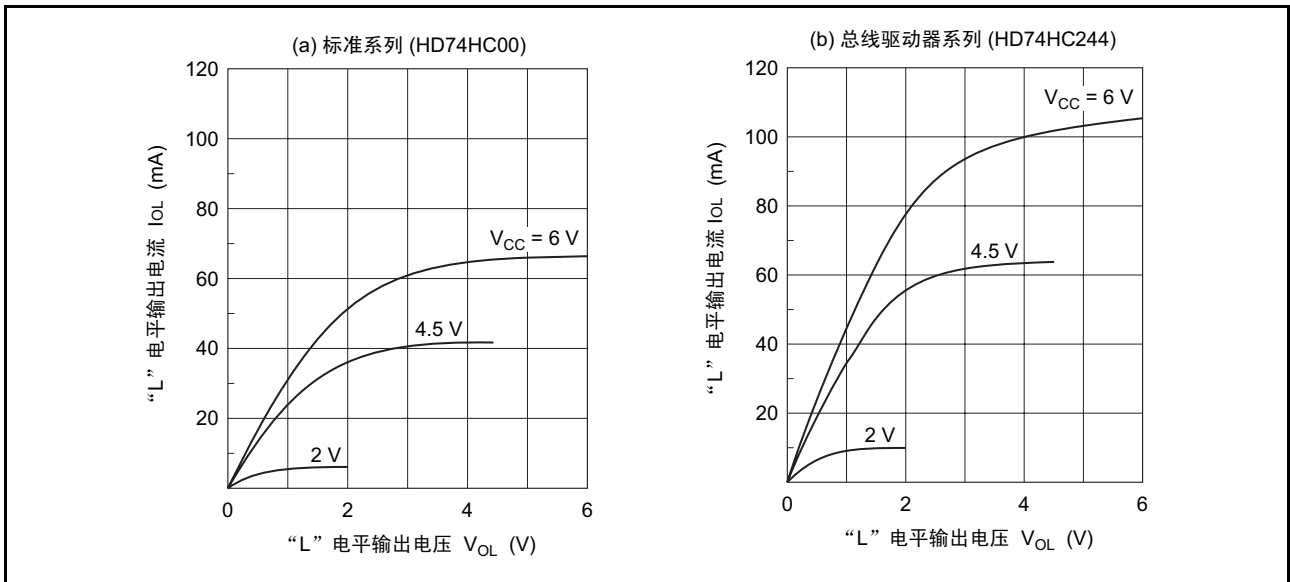


图7 输出电流特性（“L”电平）

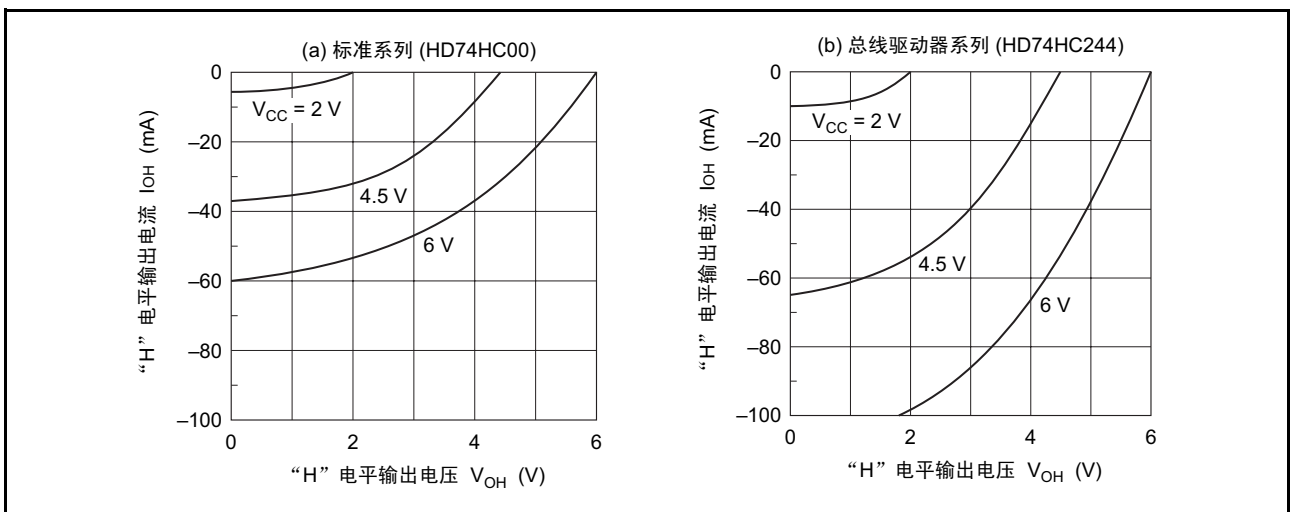


图8 输出电流特性（“H”电平）

4.2 交流特性

为了便于系统时序的设计，瑞萨高速 CMOS 逻辑的 t_{PLH} 和 t_{PHL} 基本相同。

(1) 传播延迟时间、输出的上升时间和下降时间-电源电压的特性

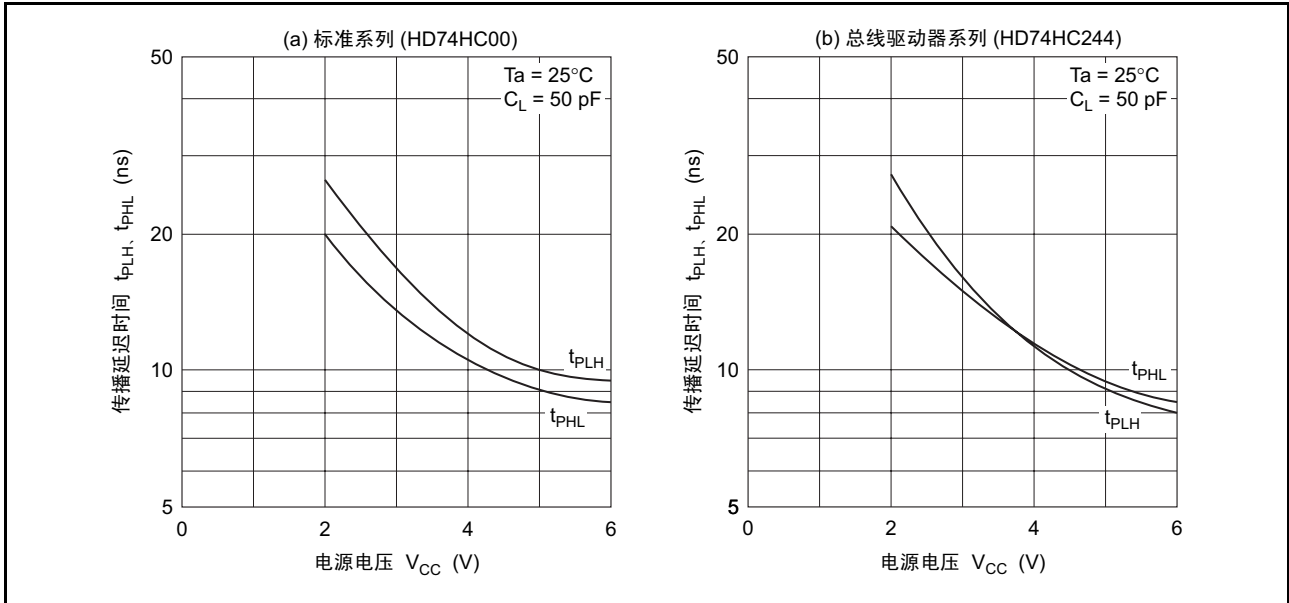


图9 传播延迟时间-电源电压的特性

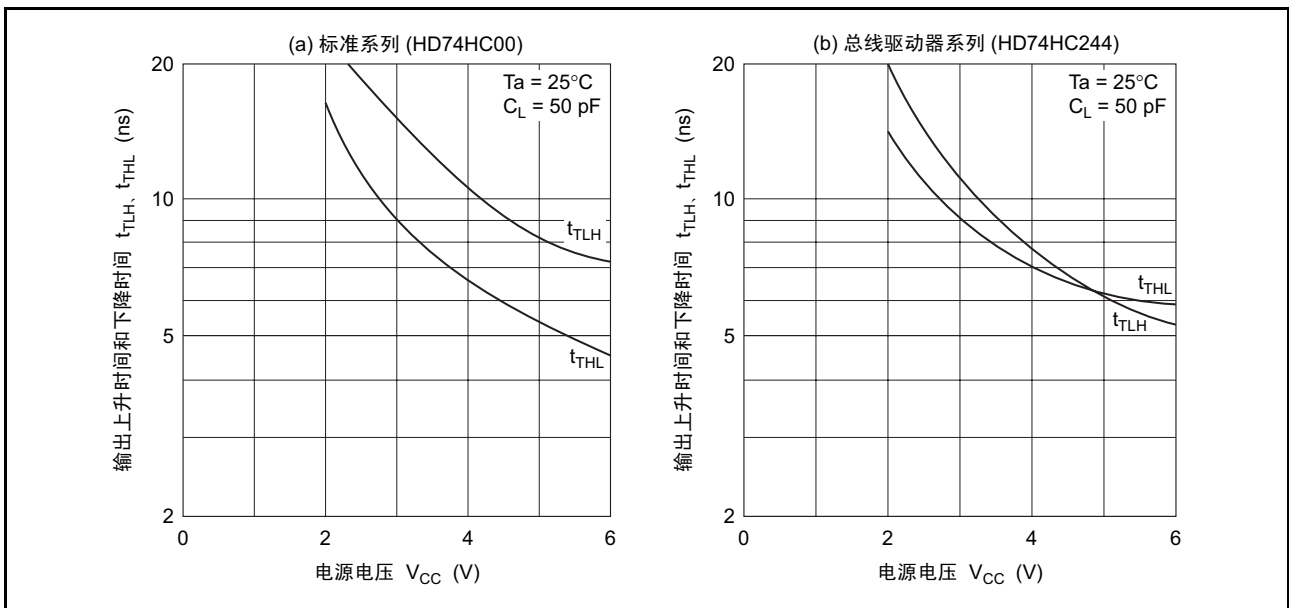


图10 输出的上升时间和下降时间-电源电压的特性

(2) 传播延迟时间、输出的上升时间和下降时间-负载电容的特性

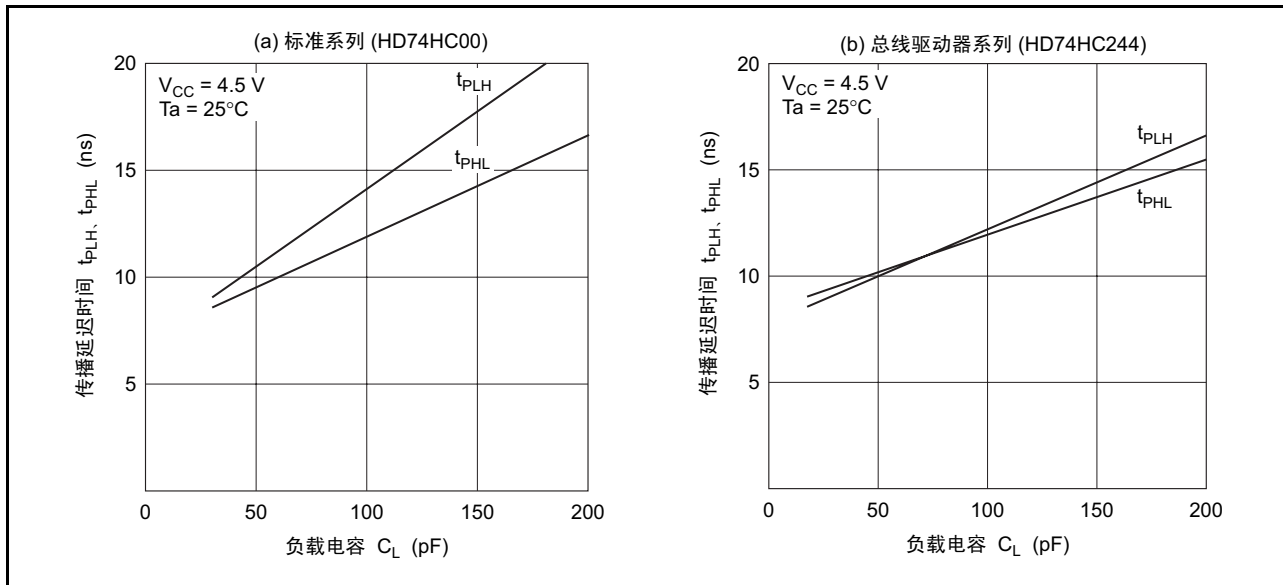


图 11 传播延迟时间-负载电容的特性

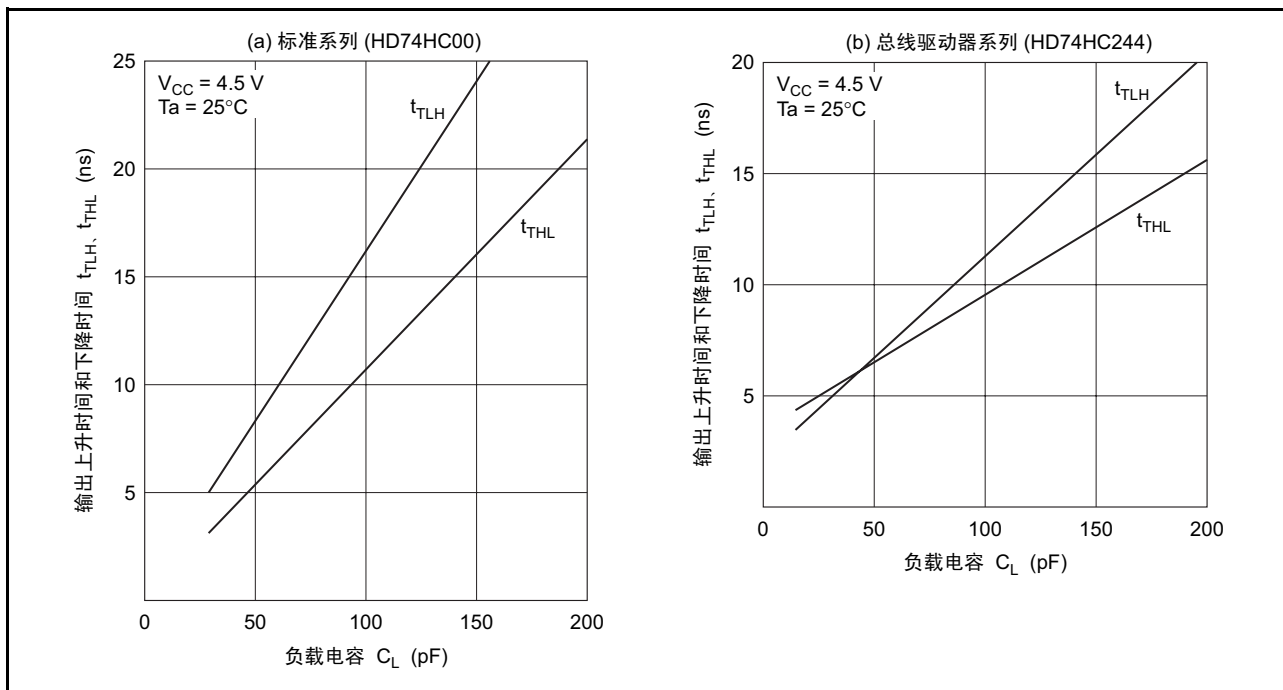


图 12 输出的上升时间和下降时间-负载电容的特性

5. 功耗

5.1 功耗的计算方法

用式(1)求高速CMOS逻辑的功耗 P_T 。即，功耗取决于负载电容、内部等效电容、工作频率和电源电压。

$$P_T = (C_L + C_{pd}) \cdot f \cdot V_{CC}^2 \quad (1)$$

在此， C_L ：负载电容， C_{pd} ：内部等效电容， f ：工作频率， V_{CC} ：电源电压

工作频率和消耗电流的特性例子如图13所示。

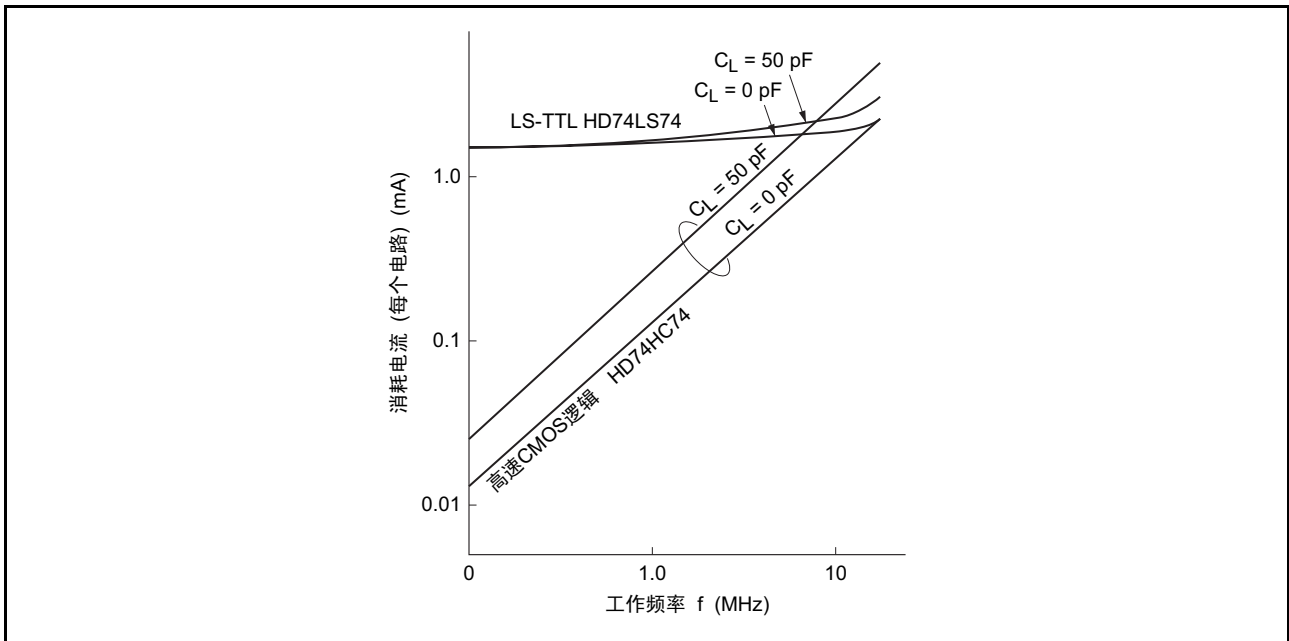


图 13 工作频率和消耗电流

5.2 内部等效电容

用以下等效式计算内部等效电容 C_{pd} :

$$P_{T1} = C_{pd} \cdot V_{CC}^2 \cdot f_1 = I_{CC1} \cdot V_{CC} \quad (2)$$

$$P_{T2} = C_{pd} \cdot V_{CC}^2 \cdot f_2 = I_{CC2} \cdot V_{CC} \quad (3)$$

由式(2)、(3)可得

$$\begin{aligned} C_{pd} &= \frac{P_{T2} - P_{T1}}{V_{CC}^2 \times (f_2 - f_1)} \\ &= \frac{I_{CC2} - I_{CC1}}{V_{CC} \times (f_2 - f_1)} \quad (4) \end{aligned}$$

在此， I_{CC1} : 频率 f_1 时的电源电流

I_{CC2} : 频率 f_2 时的电源电流

瑞萨高速 CMOS 逻辑的内部等效电容的例子如表 2 所示。

另外， C_{pd} 因输入条件而不同，其典型例子如表 3 所示。

表 2 瑞萨高速 CMOS 逻辑的内部等效电容 (C_{pd})

| 功能 | 产品型号 | 注 1 | 内部等效电容 typ.(pF) | 功能 | 产品型号 | 注 1 | 内部等效电容 typ.(pF) | |
|------------|----------|----------|--------------------|----------|-------------|-----------|--------------------|----|
| Gate | HD74HC00 | * | 27 | DECORDER | HD74HC138 | P | 90 | |
| | HD74HC04 | * | 24 | COUNTER | HD74HC161 | P | 57 | |
| Flip-Flop | D-type | HD74HC74 | * | 41 | BUFFER | HD74HC240 | * | 42 |
| | J-K-type | HD74HC76 | * | 49 | MULTIPLEXER | HD74HC258 | P | 78 |
| COMPARATOR | HD74HC85 | P | 48 | LATCH | HD74HC373 | P | 57 | |

【注】 1. *表示每个电路的值，P表示每个封装的值。

2. 测量电路如图 14 所示。

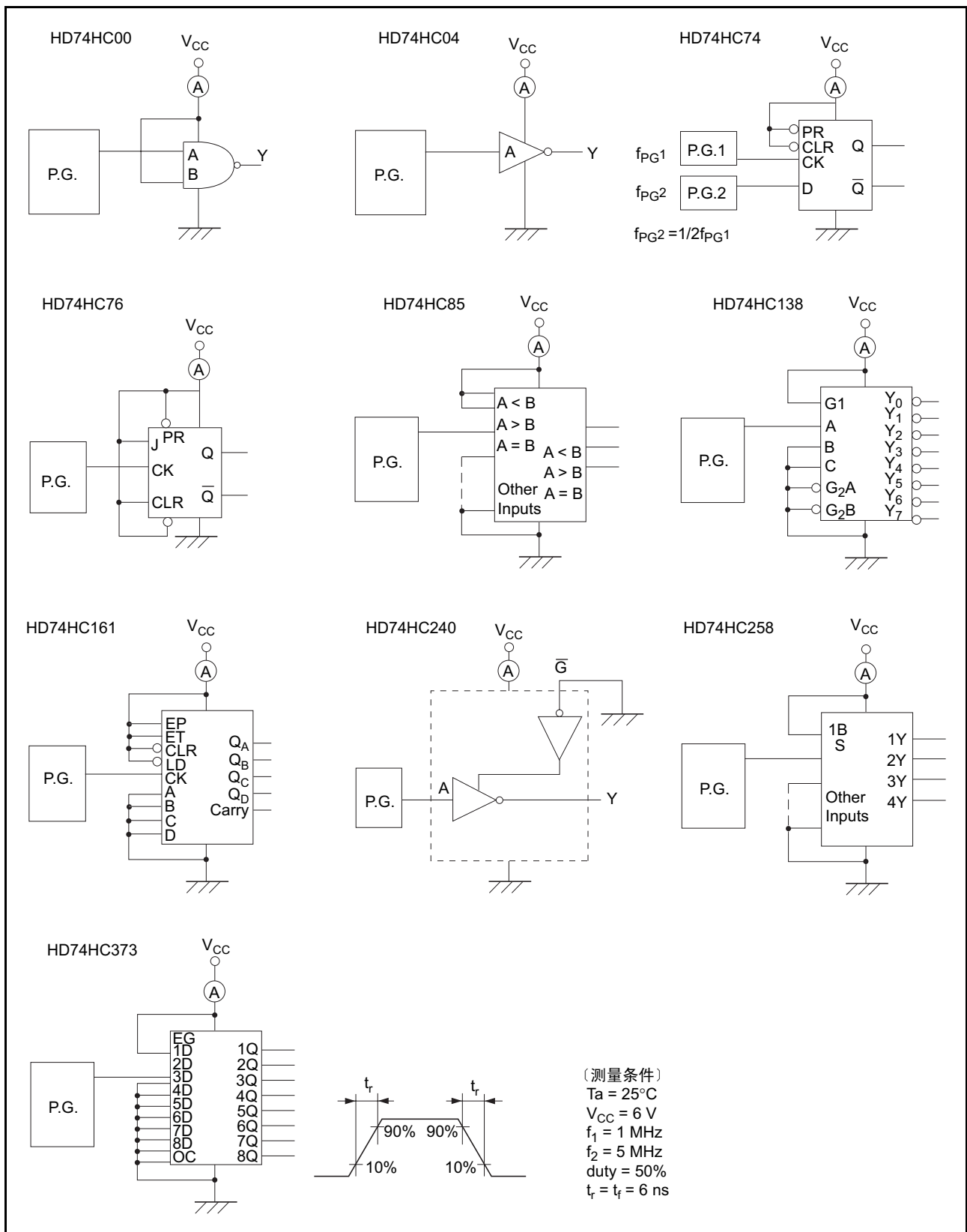
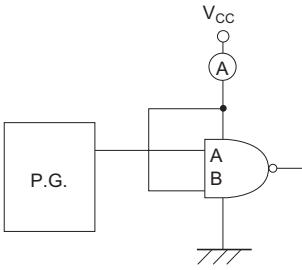
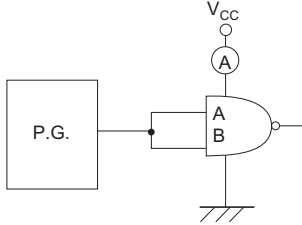
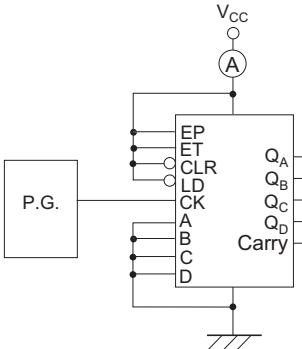
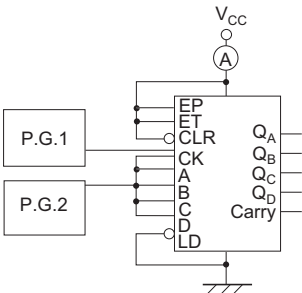


图 14 工作消耗电流的测量电路

表3 不同输入条件产生的内部等效电容 (Cpd)

| 产品型号 | 输入条件 | 内部等效电容(pF) |
|-----------|--|------------|
| HD74HC00 | <ul style="list-style-type: none"> 1个输入  | 27 |
| | <ul style="list-style-type: none"> 2个输入  | 27 |
| HD74HC161 | <ul style="list-style-type: none"> 计数状态  | 57 |
| | <ul style="list-style-type: none"> 预置状态  | 113 |

6. 去耦

CMOS逻辑在开关时有峰值电流流过，这是在每次将输出引脚从“Low”变为“High”或者从“High”变为“Low”时对输出的电容进行反复充放电而产生的电流。此峰值电流引起 V_{CC} 和GND的电位发生波动，如图15(a)所示，在开关时流过大的峰值电流，因此在输出产生振铃。为了防止此现象的发生，必须在 V_{CC} -GND之间外加约0.01~0.1 μ F的去耦电容。如图15(b)所示，通过此去耦电容，能吸收瞬间流过的电流和输出的振铃。

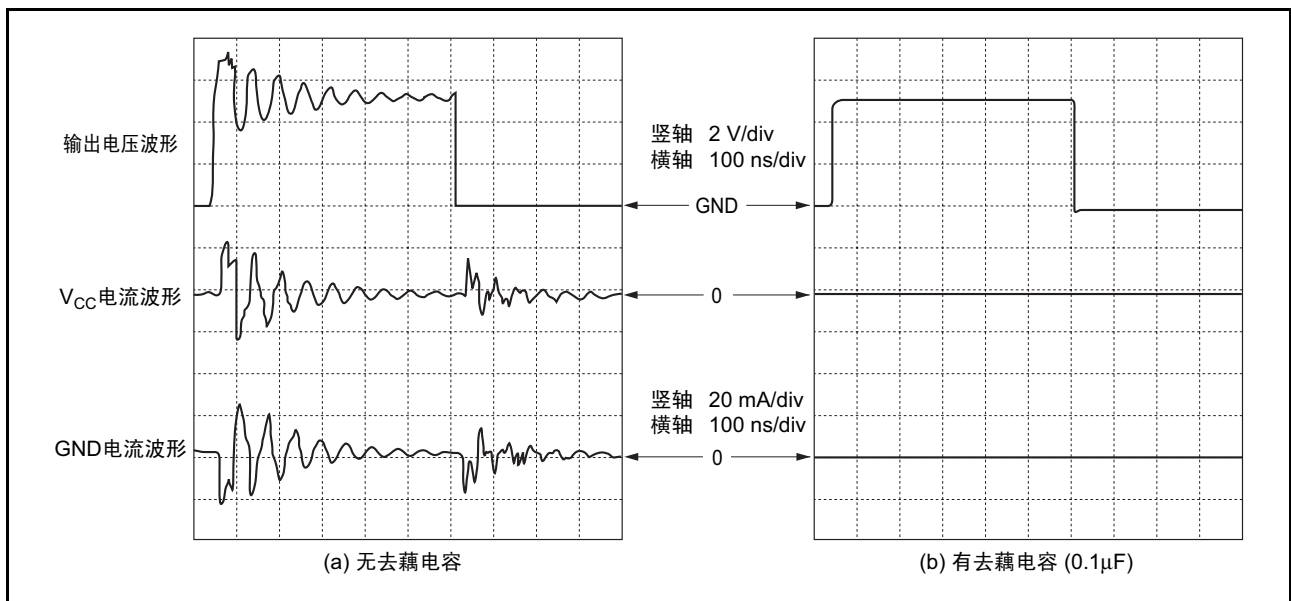


图 15 HD74HC00峰值电流的波形例子

7. 布线设计的注意事项

在进行系统设计时，因为高速CMOS逻辑和传统的标准逻辑（A1栅极CMOS逻辑和TTL等）的开关速度、输出电流特性等电特性不同，所以需要适合高速CMOS逻辑的贴装技术。在此将说明高速CMOS逻辑和LS-TTL的接口技术。

7.1 传送线的反射

(1) 使用 Bergeron 曲线图分析传送信号

在分析高速数字系统中的传送信号时，一般使用 Bergeron 曲线图。实际传送线模型（图 16）的分析结果如图 17 所示。分析条件是：使用通常的系统电路板 $Z_0=125\Omega$ ，布线长度 $l=1.5m$ 。当 HD74HC04 的输出为“High”电平时，发送端的输出阻抗为 $I_{OH}-V_{OH}$ 特性曲线，此时接收端的阻抗为 $I_{IH}-V_{IH}$ 特性曲线；当 HD74HC04 的输出为“Low”电平时，输出阻抗为 $I_{OL}-V_{OL}$ 特性曲线，接收端的阻抗为 I_F-V_F 特性曲线。能用 Z_0 的斜率描绘负载线，对这些输入/输出阻抗进行传送信号的反射分析。在图 17 的各交点坐标中，偶数点（0、2T、4T）表示线路发送端每隔 2T（T 为信号从发送端到接收端的所需时间）的电压和电流，奇数点（T、3T、5T）表示线路接收端的电压和电流。接收端波形的分析结果如图 18 所示。

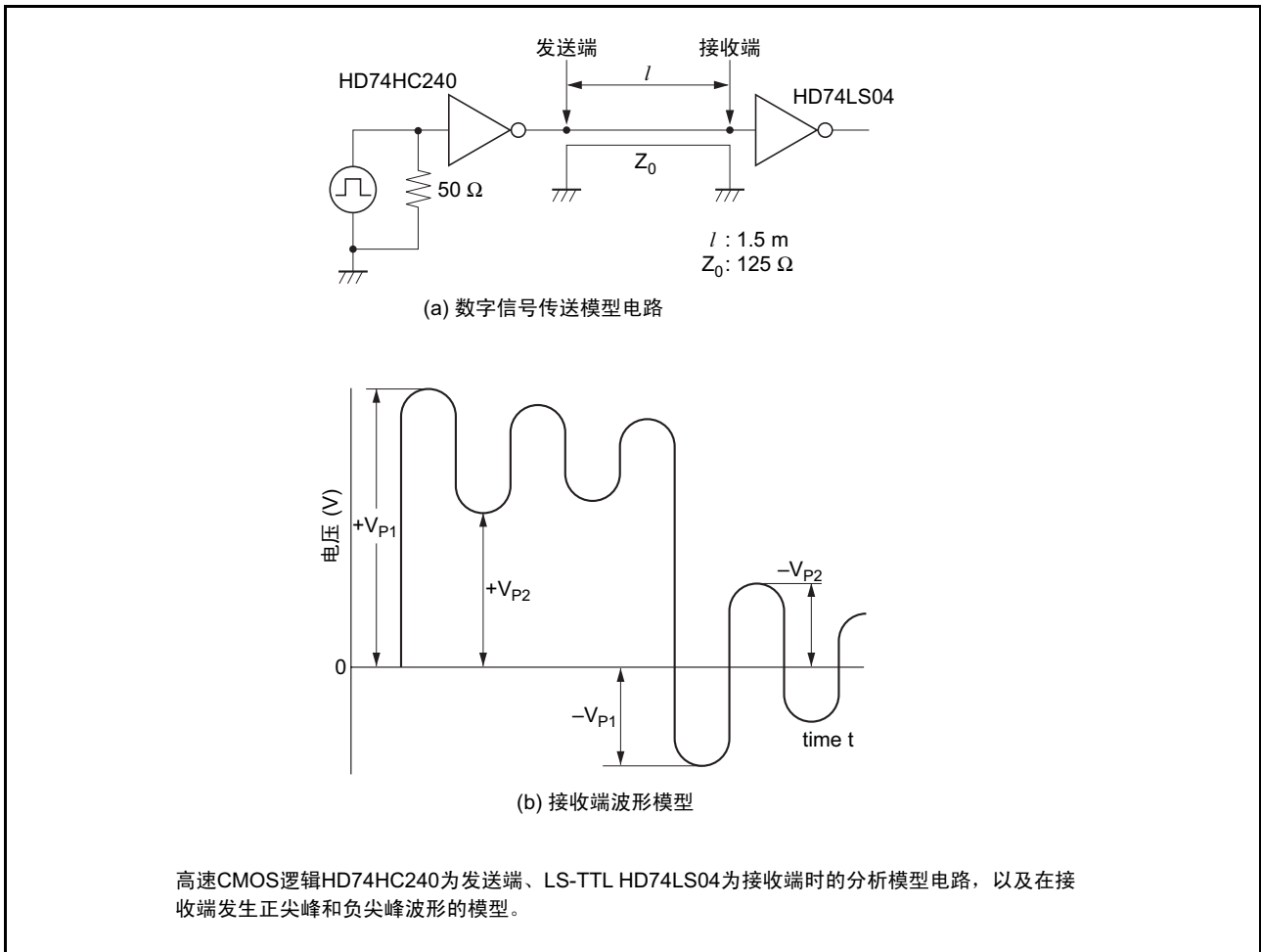
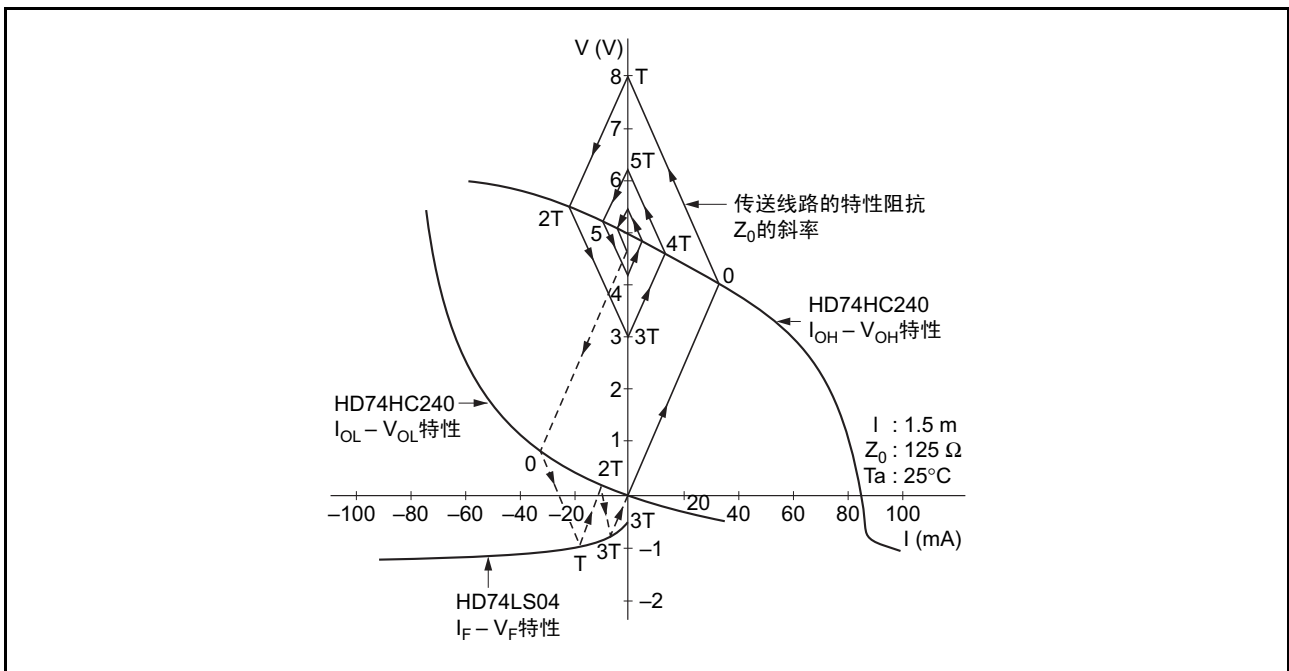


图 16 数字信号的传送



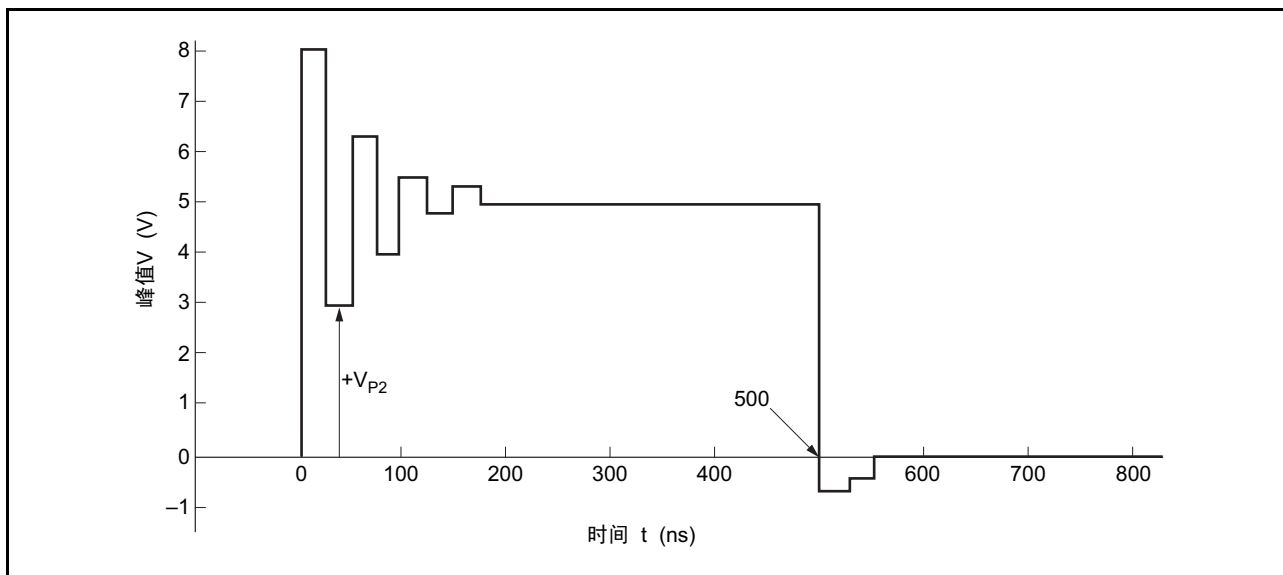


图 18 接收端波形的分析结果

(2) 传送线反射的测量例

同轴线（特性阻抗 $Z_0=50\Omega$ ）、双绞线（ $Z_0=120\Omega$ ）和引线（ $Z_0=150\sim 200\Omega$ ）这三种传送线的反射特性的测量结果如图 19 所示。

确认了在布线长不超过 2m 时发送端和接收端都能正常工作，但是在实际进行系统设计时，必须考虑布线阻抗。

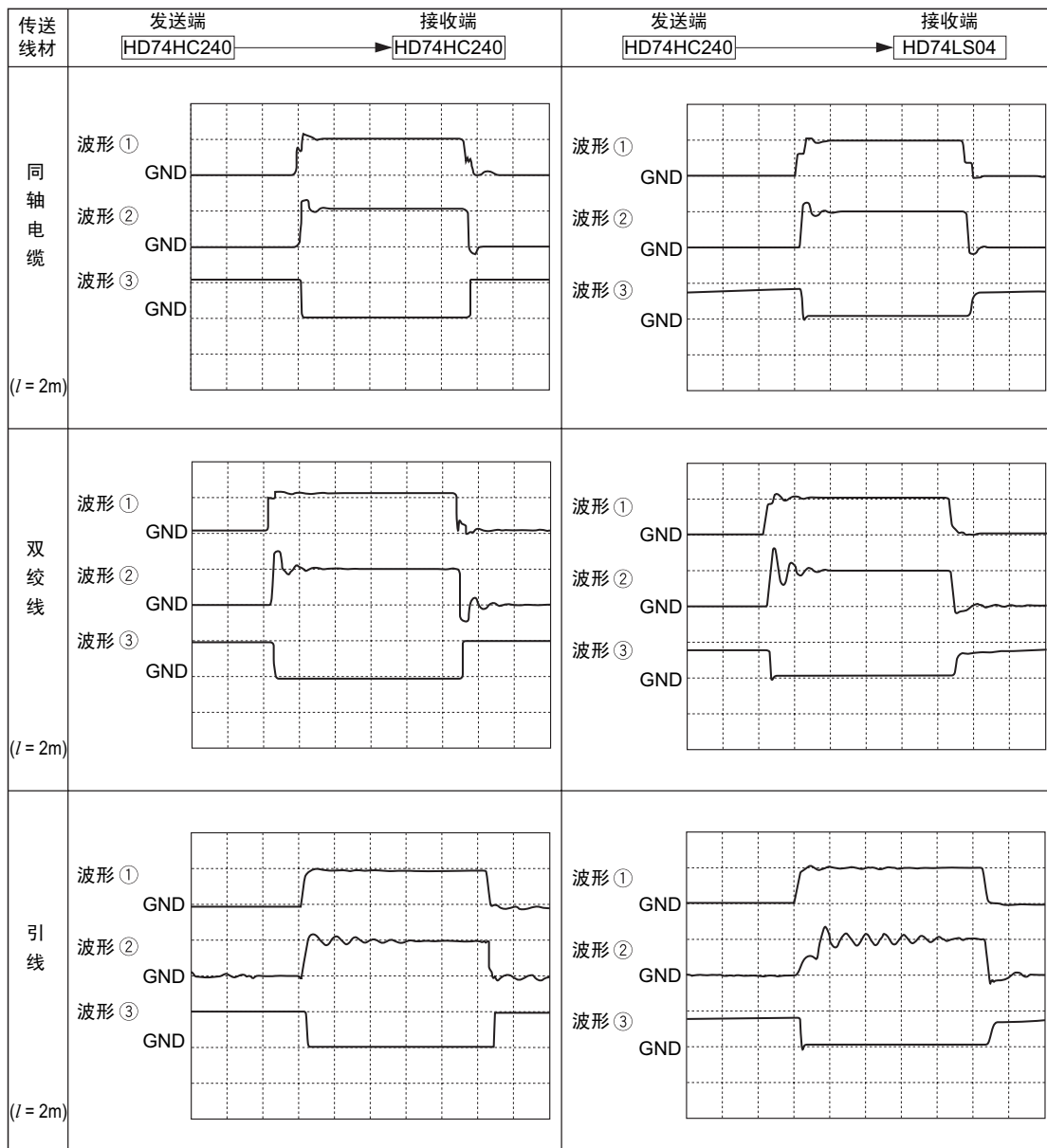
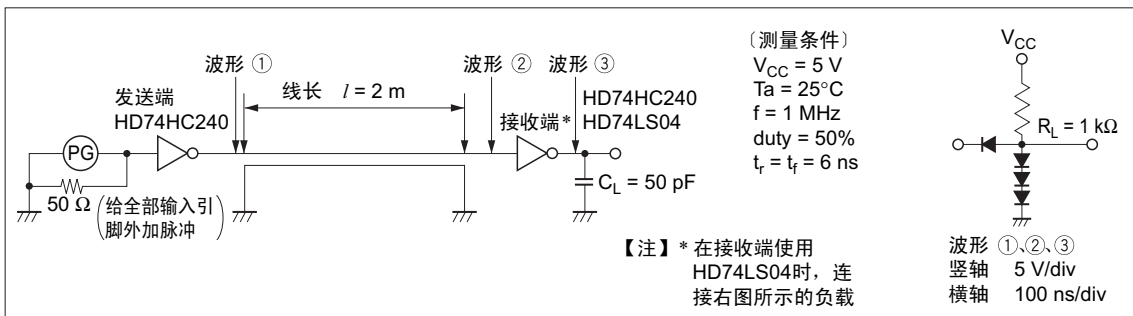


图 19 反射和振铃的波形（当发送端为总线驱动器系列的 HD74HC240 时）

7.2 串扰噪声

串扰噪声是由传送线的特性阻抗和邻近传送线的耦合阻抗引起的。双绞线引起的串扰噪声电平的典型例子如图20所示。

结果表明：当布线长度 $\geq 1\text{m}$ 时，会产生误动作；在缩小布线的间隔时，必须注意串扰。

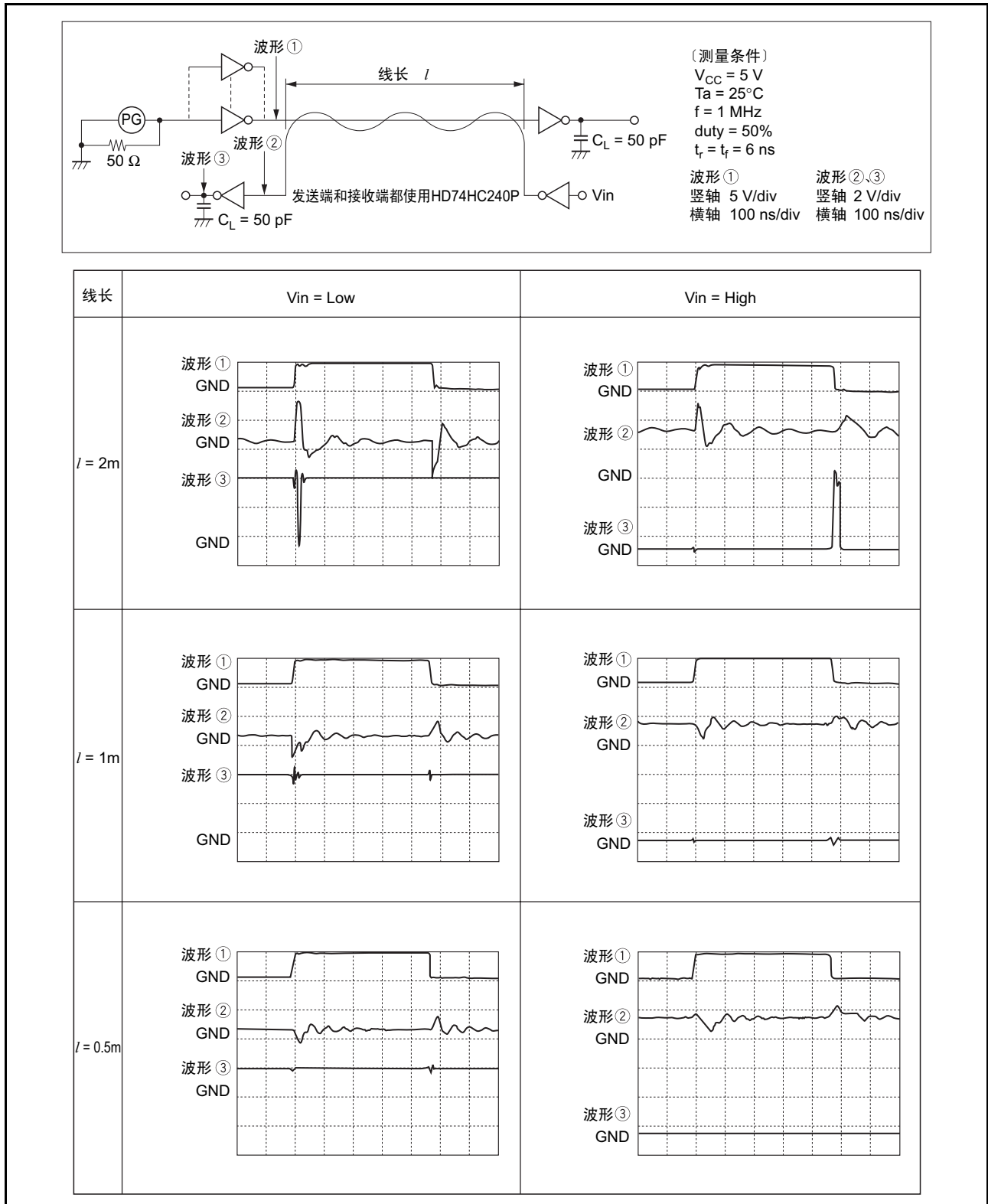


图20 串扰噪声的波形（总线驱动器系列的HD74HC240）

8. 接口

根据输入电平，瑞萨高速 CMOS 逻辑分为 74HC 型和 74HCT 型 2 种。74HC 型的输入引脚为 CMOS 电平，74HCT 型的输入引脚为 TTL 电平。以下说明高速 CMOS 逻辑和其他器件的接口。

8.1 从高速 CMOS 逻辑输出到 LS-TTL

在由高速 CMOS 逻辑驱动 LS-TTL 时，因为高速 CMOS 逻辑的输出电平是 CMOS 电平，所以不需要插入接口电路。对于输入电平为 TTL 电平的单片机或者存储器，同样也不需要接口电路。

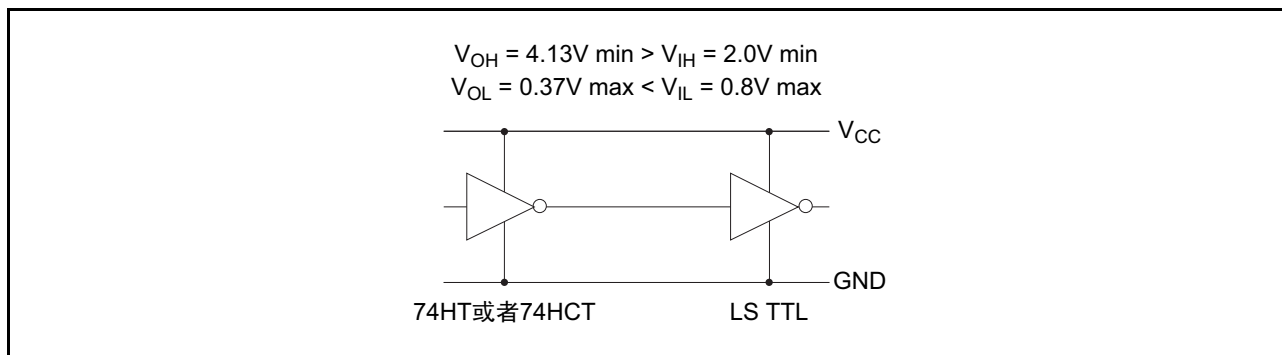


图 21 从高速 CMOS 逻辑输出到 LS-TTL

8.2 从 LS-TTL 输出到高速 CMOS 逻辑（74HCT 型）

在由 LS-TTL 驱动 74HCT 型高速 CMOS 逻辑时，不需要插入接口电路。

对于输出电平为 TTL 电平的单片机或者存储器，同样也不需要接口电路。

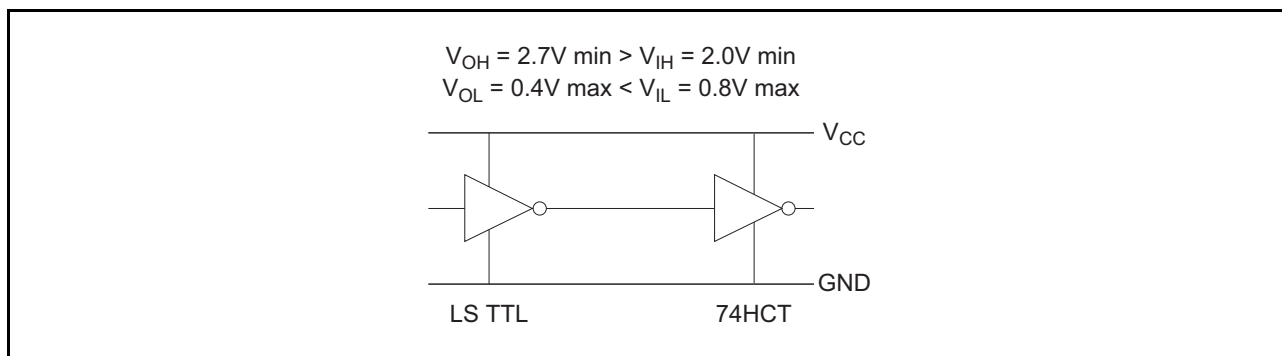


图 22 从 LS-TTL 输出到 74HCT

8.3 从 LS-TTL 输出到高速 CMOS 逻辑电路（74HC 型）

如图 23 所示，在由 LS-TTL 驱动高速 CMOS 逻辑（74HC 型）时，需要插入上拉电阻。这是因为当 LS-TTL 的输出电压 $V_{OH(min.)}=2.7V$ 时，74HC 型高速 CMOS 逻辑的输入电压 $V_{IH(min.)}=3.15V$ ，LS-TTL 的输出电平无法直接驱动 74HC 型高速 CMOS 逻辑。

对于输出电平为 TTL 电平的单片机或者存储器，也同样需要插入上拉电阻。

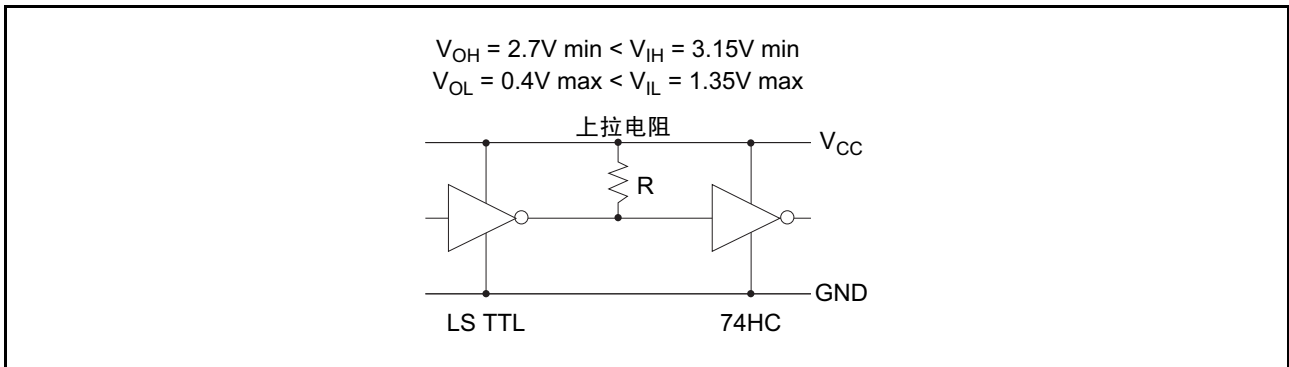


图23 从LS-TTL输出到74HC

8.4 从三态输出LS-TTL输出到高速CMOS逻辑

如图24所示，在由三态输出LS-TTL驱动高速CMOS逻辑时，需要插入上拉电阻或者下拉电阻。这是因为当LS-TTL的输出处于高阻抗状态时，下一段的高速CMOS逻辑的输入会处于不稳定状态。

另外，具有三态输出引脚的全部器件都需要相同的接口。

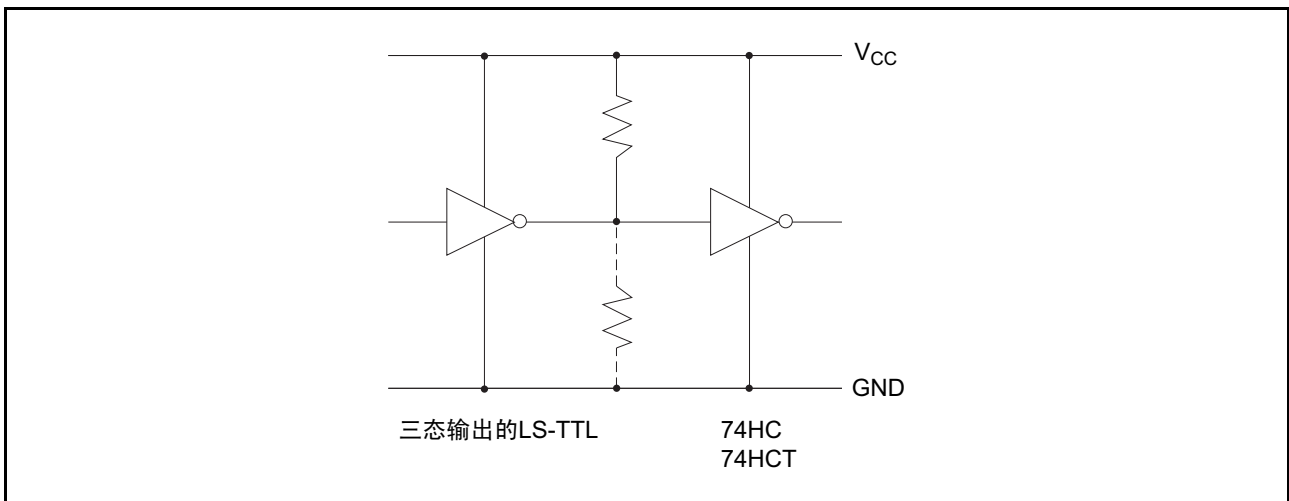


图24 从三态输出LS-TTL输出到高速CMOS逻辑

9. 贴装

9.1 SOP的贴装技术

为了维持小型IC封装的性能和质量，以下说明贴装SOP时的注意事项。

(1) 使用浸焊法贴装SOP

使用浸焊法将SOP贴装到电路板的模型例子如图25所示。

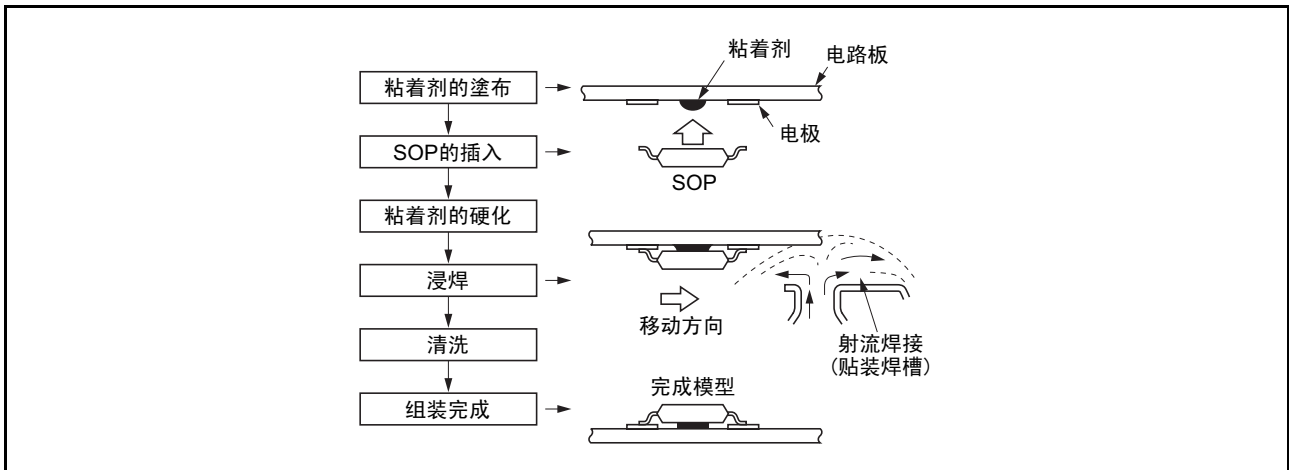


图 25 SOP 的贴装模型例子

与回流焊接法相比，浸焊的热传播系数大1个数量级，对芯片的热应力非常大。因此对耐湿性影响也很大，尤其在使用浸焊法进行贴装时，必须注意热冲击的缓和。表4总结了浸焊处理中的管理要点，请参照。如图26所示，在使用浸焊法时，为了缓和作业时产生的热冲击，推荐设有预热区的温度分布。必须将浸焊温度控制在最大260°C，浸焊时间控制在最大10sec（最好在2~4sec之间）。

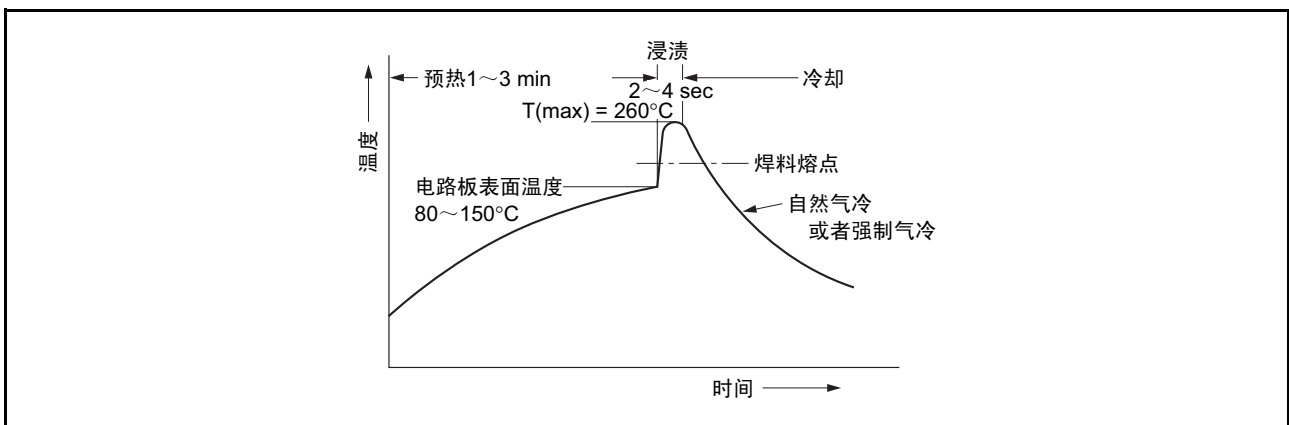


图 26 焊接的推荐温度分布（电路板的表面温度）

(2) 使用回流焊接法贴装SOP

在将SOP贴装到电路板时，基本的工程是使丝网印刷的焊膏进行回流焊接。使用标准配比Sn:Pb=6:4的焊料，或者是用添加了3%左右的Ag并且熔点是183~193°C的焊料（用于混合IC），用助焊膏和有机溶剂将上述焊料调成适合印刷粘度的糊状。

（例如，SOLDER CREAM SP210-2（糊状焊膏）TAMURA KAKEN公司的产品）

必须在低温和短时间的条件下进行贴装，电路板的表面温度（焊接部）不能超过230°C，作业时间必须在15sec以内。

表4 SOP浸焊组装的基本流程

| 工序 | 使用部件、材料、设备 | 管理要点 |
|-------------|--|--|
| 电 路 板 | 电路板材质有①环氧玻璃②酚醛纸③混合型④陶瓷，必须按目的用途选定。 | <ul style="list-style-type: none"> ●作为电路板的使用条件，必须考虑热应力的影响（收缩，弯曲）。 ●电极图形尺寸的推荐值如下（参照图27）： 对于引脚拉出方向 宽 W = 0.6~0.7 mm 长 L = 1.0~2.0 mm |
| 粘 着 剂 的 涂 布 | 环氧类粘着脂 (推荐例：热硬化环氧类) | 作为限制电路板的附着量，有电极图形附着防止。 |
| S O P 插 入 | 供给SOP | 瑞萨SOP的包装规格有塑料料条包装和带包装，请在订货时指定。 |
| 粘 着 剂 的 硬 化 | 隧道炉、烤炉等 | 必须在适合粘着剂的条件下进行硬化处理。（但是，硬化温度不能超过150°C） |
| (其他部件的供给) | — | — |
| 助 焊 剂 的 供 给 | 松香助焊剂 | 为了进行高可靠性的贴装，请使用松香助焊剂。氯类的助焊剂会降低可靠性。 |
| 预 热 | 用隧道炉、烤炉等将周围空气加热。 | 为了缓和浸焊时的热冲击，建议设置预热区。SOP贴装温度分布例子如图26所示，请参考。 |
| 浸 焊 | <p>为了降低组装后的不良率，建议使用贴装焊槽。在发生引脚间的焊桥时，请使用下述的修正工具等。</p> <ul style="list-style-type: none"> ●焊料吸取器 (千住金属工业公司： 型号MS2200F) | <p>从维持IC可靠性的观点出发，必须在极低的温度和短时间的条件下进行处理。推荐浸焊条件如下（参照图26）：</p> <ul style="list-style-type: none"> ●浸焊最高温度 260°C ●浸焊最大处理時間 10sec (最好在2~4 sec之间) |
| 冷 却 | 自然气冷或者强制气冷 | |
| 清 洗 | 用氟利昂等溶剂清洗 | |

(3) 电路板的电极尺寸和焊接性

焊接不良的发生率受SOP焊盘尺寸的影响。SOP引脚之间的焊桥不良以及焊料不足不良对焊盘尺寸的依赖性如图27所示。建议按照图中安全区内的焊盘尺寸进行设定。

另外，在使用回流焊接法进行贴装时，建议焊膏的印刷厚度至少为0.2mm^t。

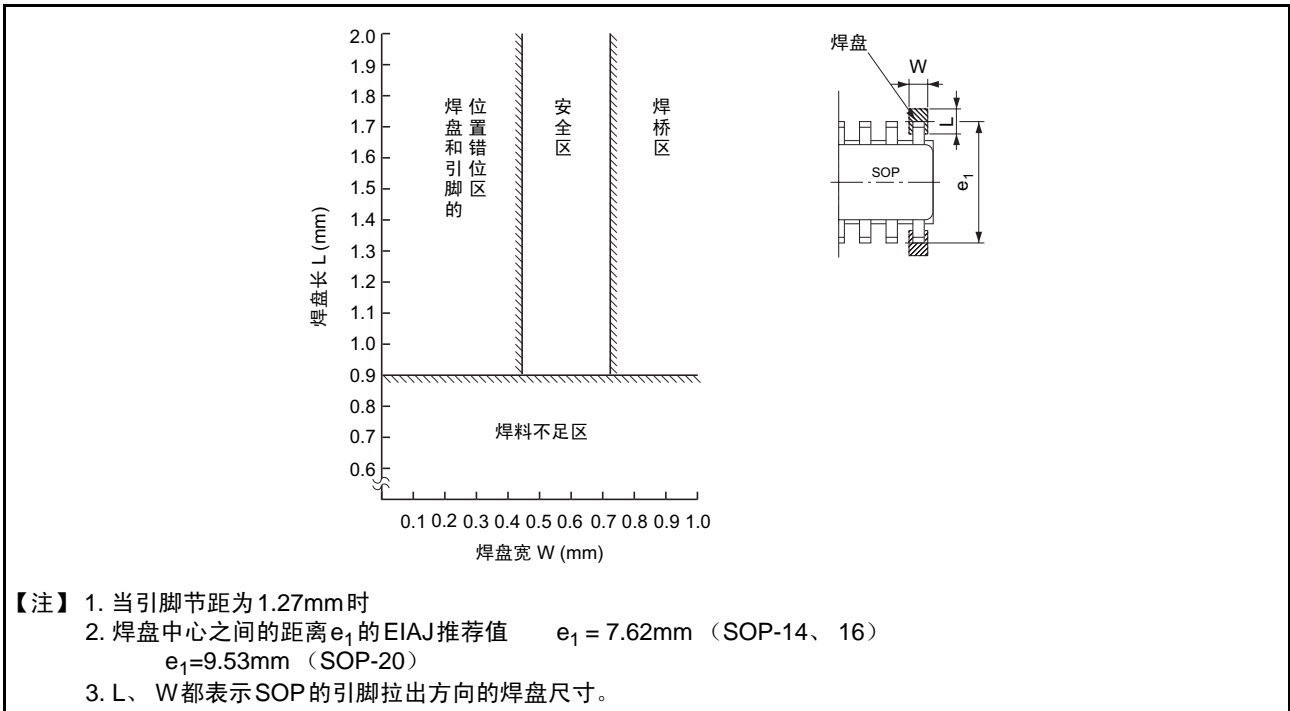


图27 焊盘尺寸的推荐值

(4) SOP 的热阻

在高速 CMOS 逻辑电路中，SOP 的减额曲线以及此时的热阻 (θ_{j-a}) 分别如图 28 和表 5 所示。

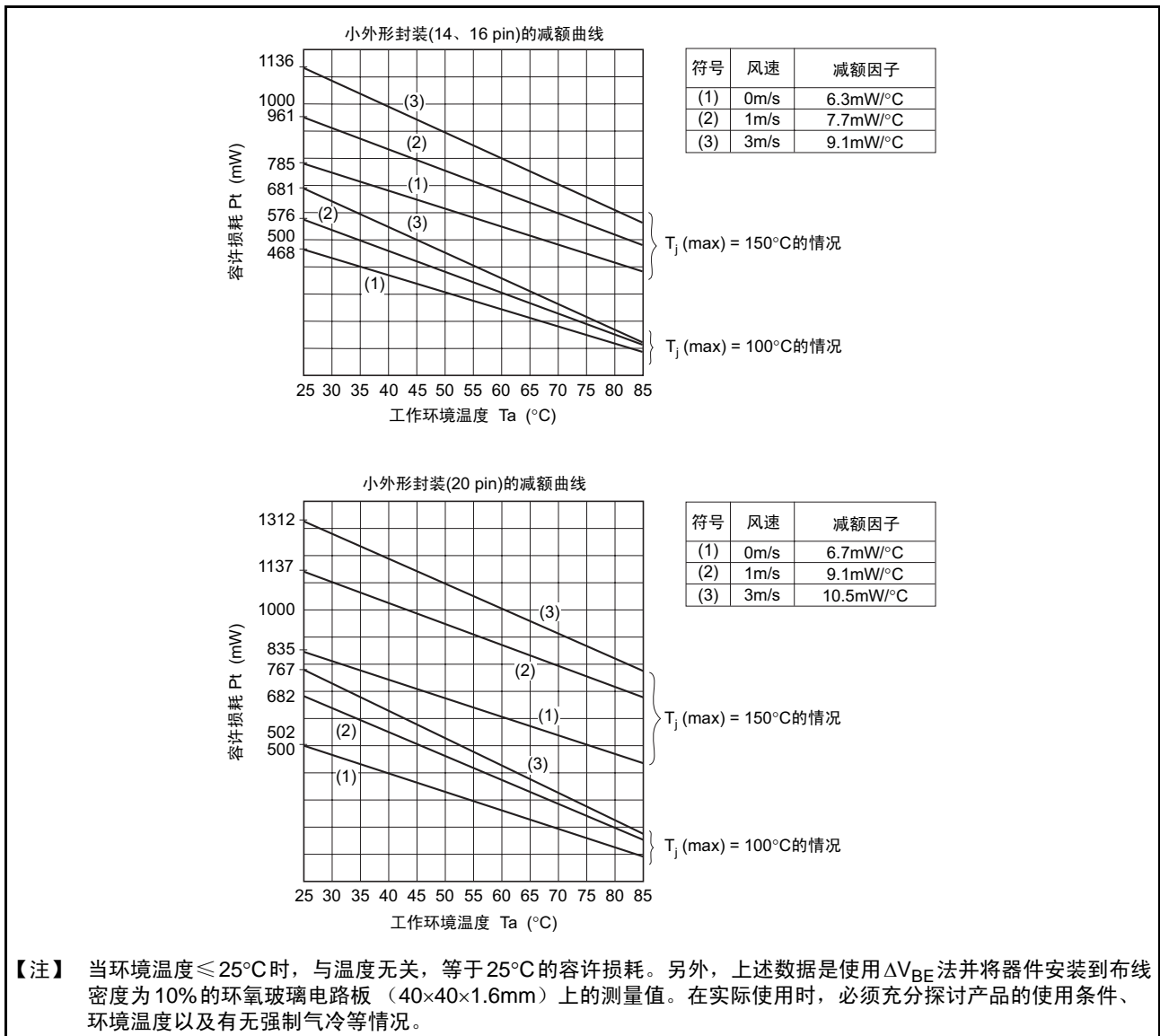


图28 SOP的减额曲线

表5 SOP封装的热阻

| 引脚数 | 风速 | 减额因子 | 热阻 | 容许损耗 Ta = 25°C | |
|-------|------|-----------|---------|----------------------------|----------------------------|
| | | | | T _{j(max)} =150°C | T _{j(max)} =100°C |
| 14、16 | 0m/s | 6.3mW/°C | 160°C/W | 785mW | 468mW |
| | 1m/s | 7.7mW/°C | 130°C/W | 961mW | 576mW |
| | 3m/s | 9.1mW/°C | 110°C/W | 1136mW | 681mW |
| 20 | 0m/s | 6.7mW/°C | 150°C/W | 835mW | 502mW |
| | 1m/s | 9.1mW/°C | 110°C/W | 1137mW | 682mW |
| | 3m/s | 10.5mW/°C | 95°C/W | 1312mW | 787mW |

(5) 薄型SSOP的热阻

在HD74HC系列中，TSSOP的减额曲线如图29所示，此时的热阻（ θ_{j-a} ）和贴装方法分别如表6和图30所示。

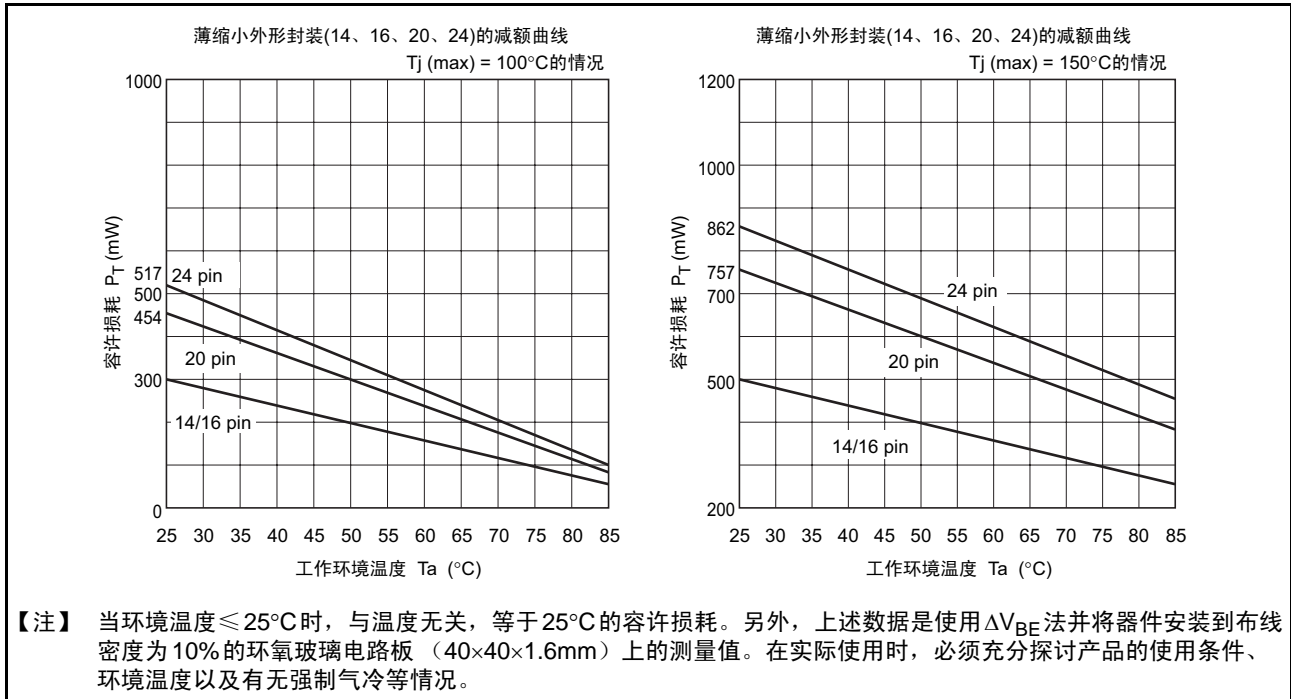


图29 TSSOP的减额曲线

表6 TSSOP封装的热阻

| 引脚数 | 风速 | 减额因子 | 热阻 | 容许损耗 Ta = 25°C | |
|-------|------|----------|---------|----------------------------|----------------------------|
| | | | | T _{j(max)} =150°C | T _{j(max)} =100°C |
| 14、16 | 0m/s | 4.0mW/°C | 250°C/W | 500mW | 300mW |
| 20 | 0m/s | 6.1mW/°C | 165°C/W | 757mW | 454mW |
| 24 | 0m/s | 6.9mW/°C | 145°C/W | 862mW | 517mW |

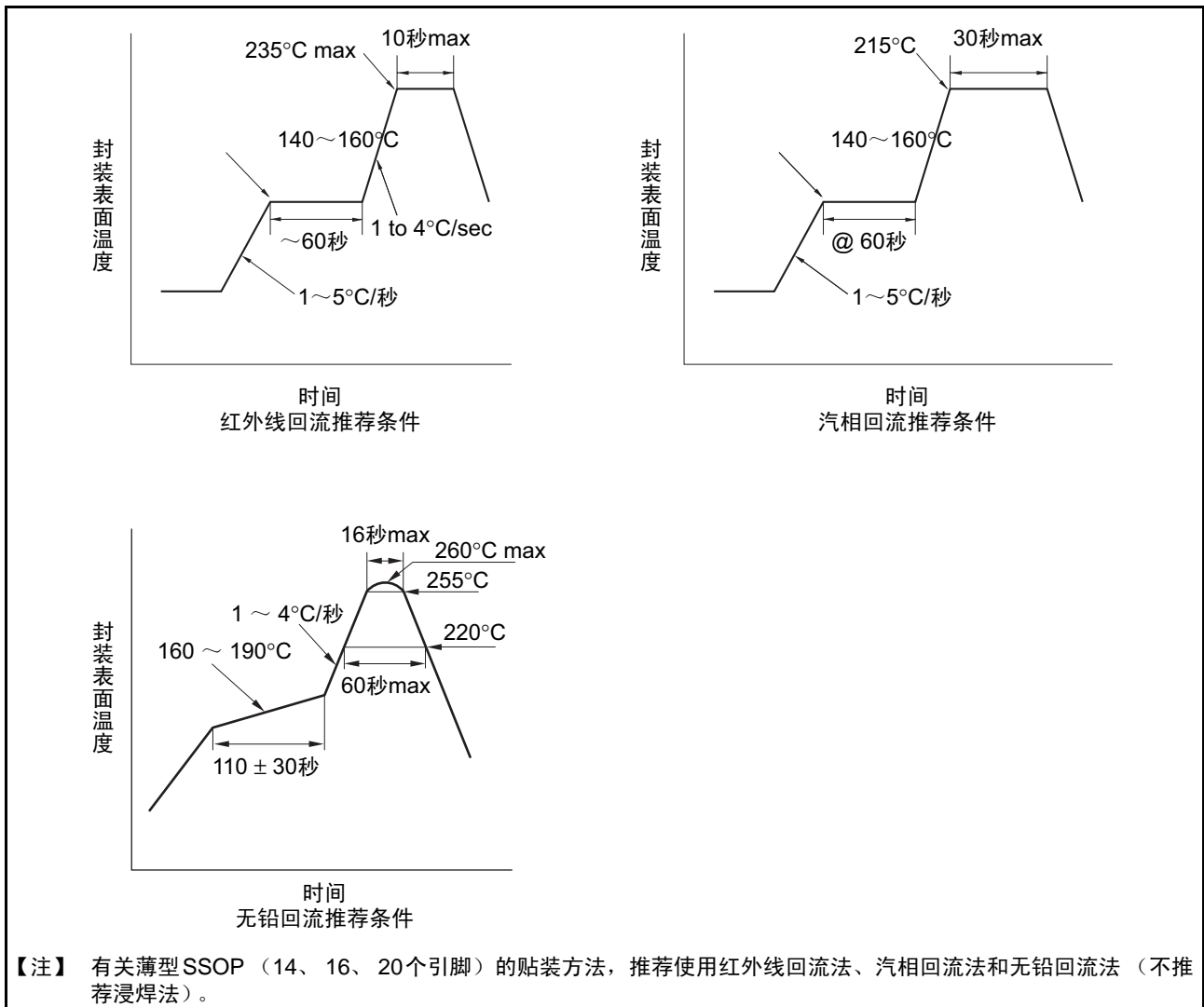
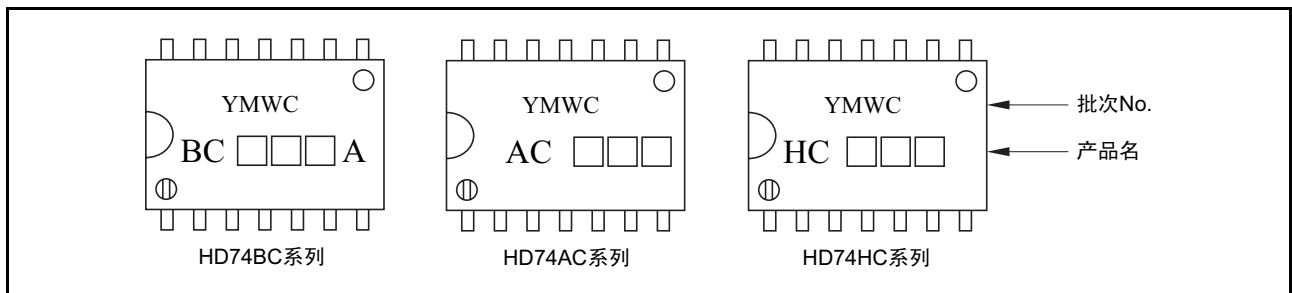


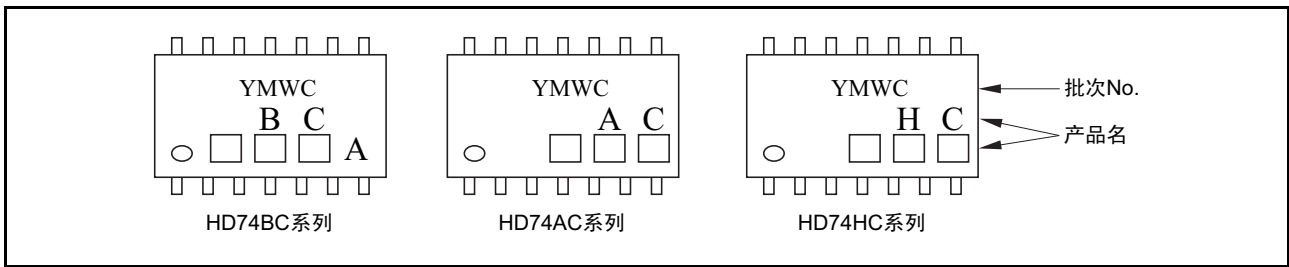
图30 TSSOP的贴装方法

10. 封装上的标记

10.1 小外形封装（SOP）14、16、20个引脚



10.2 薄缩小外形封装（TSSOP）14、16、20个引脚



【注】 标记规格的含义

器件名（例）：HD74BC245AT

Y: 年代码（公历的最后一位）

M: 月代码

W: 星期代码

C: 本公司的管理代码

产品名: 表示除HD74和封装代码（T）以外的器件名

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| Rev. | 发行日 | 修订内容 | |
|------|------------|------|------|
| | | 页 | 修订处 |
| 1.00 | 2008.03.25 | 一 | 初版发行 |

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