[Notes]

Renesas Starter Kit for RX63T (64-pin) Sample Code
Renesas Starter Kit for RX63T (144-pin) Sample Code

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Outline

This issue is a note concerning usage of sample code for the Renesas Starter Kit for RX63T (64-pin) and the Renesas Starter Kit for RX63T (144-pin). When using the sample code of the Renesas Starter Kit for RX63T (64-pin) and Renesas Starter Kit for RX63T (144-pin), take note of the problem described in this note regarding the following point.

1. The system clock control register (SCKCR) setting

   Applicable products: Renesas Starter Kit for RX63T (64-pin) and Renesas Starter Kit for RX63T (144-pin)

1. The System Clock Control Register (SCKCR) Setting

1.1 Applicable Products and List of Sample Code

Product name	Renesas Starter Kit for RX63T (64-pin)	Renesas Starter Kit for RX63T (144-pin)
Applicable products	・Sample code in attached installers ・Sample code as attachments to the following application notes posted on the Web - R20AN0275JJ0100 (CS+) - R20AN0275EJ0100 (CS+) - R01AN1793EG0100 (HEW) - R01AN1794EG0100 (e^2 studio)	Sample code in attached installers Sample code as attachments to the following application notes posted on the Web - R01AN2046EG0100 (e^2 studio) - R01AN2062EG0100 (CS+)
Affected sample code	・ADC_Oneshot ・ADC_Repeat ・Application ・Async_Serial ・CAC ・CRC ・DMAC ・DTC ・IIC_Master ・IIC_Slave ・IWDT ・LIN_Master ・LIN_Slave ・Power_Down ・PWM ・SPI ・Sync_Serial ・Timer_Capture ・Timer_Compare ・Timer_Event ・Timer_Mode ・Tutorial ・Voltage_Detect ・WDT	・ADC_Oneshot ・ADC_Repeat ・Application ・Async_Serial ・CAC ・CAN ・CRC ・DMAC ・DTC ・IIC_Master ・IIC_Slave ・IWDT ・Power_Down ・PWM ・SPI ・Sync_Serial ・Timer_Capture ・Timer_Compare ・Timer_Event ・Timer_Mode ・Tutorial ・Voltage_Detect ・WDT

1.2 Renesas Starter Kit for RX63T (64-pin)

1.2.1 Details

We have identified an error in the setting of the system clock control register (SCKCR).

- CAC sample code SCKCR register setting: 0x00000660
  - PCLKD, PCLKA, BCLK, ICLK, and FCLK are set for frequency division by one, so note 10 on the SCKCR register in Rev2.10 of the RX63T Group User's Manual: Hardware was not observed.
  - PCLKB is set for frequency division by 64 and BCLK is set for frequency division by one, which is not in agreement with note 11 on the SCKCR register in Rev2.10 of the RX63T Group User's Manual: Hardware.

Note 1. Make a setting such that the frequencies satisfy the relation PCLKB:PCLKD = N:1, where N is an integer.
Note 2. Make a setting such that the frequencies satisfy the relation PCLKB:PCLKC = N:1 or 1:N, where N is an integer.
Note 3. Make a setting such that the frequencies satisfy the relation ICLK:PCLKB = N:1 or 1:N, where N is an integer.
Note 4. Make a setting such that the frequencies satisfy the relation ICLK:PCLKA = N:1 or 1:N, where N is an integer.
Note 5. Make a setting such that the frequencies satisfy the relation PCLKA:PCLKB = N:1, where N is an integer.
Note 6. The setting for division by one is prohibited if the PLL is selected.
Note 7. Do not make a setting such that the ICLK runs at a lower frequency than the external bus clock.
Note 8. When operation of the external bus clock is selected, the PE5 I/O port pin function is not available because it is multiplexed on the same pin as the BCLK pin function.
Note 9. Make a setting such that the frequencies satisfy the relation ICLK:FCLK = N:1 or 1:N, where N is an integer.
Note 10. The setting for division by one or two is prohibited if the SCKCR3.CKSEL[2:0] bits are set to 010b (the main clock oscillator is selected)
Note 11. In 64- and 48-pin products, set the same value as the highest division ratio among the settings of the ICK[3:0] and PCKB[3:0] bits.

Figure 1 Excerpt 1 from Rev2.10 of the RX63T Group User's Manual: Notes on setting of the SCKCR register

- SCKCR register settings other than in sample code for the CAC: 0x21821211
  - PCLKD is set to 96 MHz, which exceeds the maximum frequency of 50 MHz.
  - PCLKB is set for frequency division by four and PCLKC for frequency division by two, which is not in agreement with note 11.

Note 1. Make a setting such that the frequencies satisfy the relation PCLKB:PCLKD = N:1, where N is an integer.
Note 2. Make a setting such that the frequencies satisfy the relation PCLKB:PCLKC = N:1 or 1:N, where N is an integer.
Note 3. Make a setting such that the frequencies satisfy the relation ICLK:PCLKB = N:1 or 1:N, where N is an integer.
Note 4. Make a setting such that the frequencies satisfy the relation ICLK:PCLKA = N:1 or 1:N, where N is an integer.
Note 5. Make a setting such that the frequencies satisfy the relation PCLKA:PCLKB = N:1, where N is an integer.
Note 6. The setting for division by one is prohibited if the PLL is selected.
Note 7. Do not make a setting such that the ICLK runs at a lower frequency than the external bus clock.
Note 8. When operation of the external bus clock is selected, the PE5 I/O port pin function is not available because it is multiplexed on the same pin as the BCLK pin function.
Note 9. Make a setting such that the frequencies satisfy the relation ICLK:FCLK = N:1 or 1:N, where N is an integer.
Note 10. The setting for division by one or two is prohibited if the SCKCR3.CKSEL[2:0] bits are set to 010b (the main clock oscillator is selected)
Note 11. In 64- and 48-pin products, set the same value as the highest division ratio among the settings of the ICK[3:0] and PCKB[3:0] bits.

Figure 2 Excerpt 2 from Rev2.10 of the RX63T Group User's Manual: Notes on setting of the SCKCR register

1.2.2 Workaround

Correct the function ConfigureOperatingFrequency in hwsetup.c in the following way.

Correct the settings in blue text to those in red text within the function.

- Setting of the SCKCR register in the CAC sample code

- Before modification

```
void ConfigureOperatingFrequency (void)
{
//Omit
SYSTEM.SCKCR.LONG = 0x00000660;

/* Set the clock source to Main Clock (EXTAL) */
SYSTEM.SCKCR3.WORD = 0x0200;

/* Protection on */
SYSTEM.PRCR.WORD = 0xA500;
}
```

- After modification

```
void ConfigureOperatingFrequency (void)
{
//Omit
SYSTEM.SCKCR.LONG = 0x22862666;

/* Set the clock source to Main Clock (EXTAL) */
SYSTEM.SCKCR3.WORD = 0x0200;

/* Protection on */
SYSTEM.PRCR.WORD = 0xA500;
}
```

➢ SCKCR register setting other than in the CAC sample code

- Before modification

```
void ConfigureOperatingFrequency (void)
 {
 //Omit
 SYSTEM.SCKCR.LONG = 0x21821211;

 /* Set the clock source to PLL */
 SYSTEM.SCKCR3.WORD = 0x0400;

 /* Protection on */
 SYSTEM.PRCR.WORD = 0xA500;
 }
```

- After modification

```
void ConfigureOperatingFrequency (void)
 {
 //Omit
 SYSTEM.SCKCR.LONG = 0x21821222;

 /* Set the clock source to PLL */
 SYSTEM.SCKCR3.WORD = 0x0400;

 /* Protection on */
 SYSTEM.PRCR.WORD = 0xA500;
 }
```

1.3 Renesas Starter Kit for RX63T (144-pin)

1.3.1 Details

We have identified an error in the setting of the system clock control register (SCKCR).

- CAC sample code SCKCR register setting: 0x00000660
- PCLKD, PCLKA, BCLK, ICLK, and FCLK are set for frequency division by one, so note 10 on the SCKCR register in Rev2.10 of the RX63T Group User's Manual: Hardware was not observed.

Note 1. Make a setting such that the frequencies satisfy the relation PCLKB:PCLKD = N:1, where N is an integer.
Note 2. Make a setting such that the frequencies satisfy the relation PCLKB:PCLKC = N:1 or 1:N, where N is an integer.
Note 3. Make a setting such that the frequencies satisfy the relation ICLK:PCLKB = N:1 or 1:N, where N is an integer.
Note 4. Make a setting such that the frequencies satisfy the relation ICLK:PCLKA = N:1 or 1:N, where N is an integer.
Note 5. Make a setting such that the frequencies satisfy the relation PCLKA:PCLKB = N:1, where N is an integer.
Note 6. The setting for division by one is prohibited if the PLL is selected.
Note 7. Do not make a setting such that the ICLK runs at a lower frequency than the external bus clock.
Note 8. When operation of the external bus clock is selected, the PE5 I/O port pin function is not available because it is multiplexed on the same pin as the BCLK pin function.
Note 9. Make a setting such that the frequencies satisfy the relation ICLK:FCLK = N:1 or 1:N, where N is an integer.
Note 10. The setting for division by one or two is prohibited if the SCKCR3.CKSEL[2:0] bits are set to 010b (the main clock oscillator is selected)
Note 11. In 64- and 48-pin products, set the same value as the highest division ratio among the settings of the ICK[3:0] and PCKB[3:0] bits.

Figure 3 Excerpt 3 from Rev2.10 of the RX63T Group User's Manual: Notes on setting of the SCKCR register

- SCKCR register setting other than in sample code for the CAC: 0x21821211
  - PCLKD is set to 96 MHz, which exceeds the maximum frequency of 50 MHz.

1.3.2 Workaround

Correct the function ConfigureOperatingFrequency in hwsetup.c in the following way.

Correct the settings in blue text to those in red text within the function.

- Setting of the SCKCR register in the CAC sample code

  - Before modification

```
void ConfigureOperatingFrequency (void)
 {
 //Omit
 SYSTEM.SCKCR.LONG = 0x00000660;

 /* Set the clock source to Main Clock (EXTAL) */
 SYSTEM.SCKCR3.WORD = 0x0200;

 /* Protection on */
 SYSTEM.PRCR.WORD = 0xA500;
 }
```

- After modification

```
void ConfigureOperatingFrequency (void)
 {
 //Omit
 SYSTEM.SCKCR.LONG = 0x22862666;

 /* Set the clock source to Main Clock (EXTAL) */
 SYSTEM.SCKCR3.WORD = 0x0200;

 /* Protection on */
 SYSTEM.PRCR.WORD = 0xA500;
 }
```

➢ SCKCR register settings other than in the CAC sample code

- Before modification

```
void ConfigureOperatingFrequency (void)
 {
 //Omit
 SYSTEM.SCKCR.LONG = 0x21821211;

 /* Set the clock source to PLL */
 SYSTEM.SCKCR3.WORD = 0x0400;

 /* Protection on */
 SYSTEM.PRCR.WORD = 0xA500;
 }
```

- After modification

```
void ConfigureOperatingFrequency (void)
 {
 //Omit
 SYSTEM.SCKCR.LONG = 0x21821212;

 /* Set the clock source to PLL */
 SYSTEM.SCKCR3.WORD = 0x0400;

 /* Protection on */
 SYSTEM.PRCR.WORD = 0xA500;
 }
```

1.4 Schedule for Fixing the Problem

We will rectify the problem with the sample code as attachments to the application notes on the Web in the next version.

We do not plan to fix the sample code in the attached installers because you can get the latest version of the sample code by downloading it from the Web.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 16, 2016	-	First edition issued

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