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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A009A/E	Rev.	1.00
Title	Usage Notes on the Multi-Function Timer Pulse Unit 3 (MTU3)		Information Category	Technical Notification		
Applicable Product	RX62T Group	Lot No. —	Reference Document	RX62T Group User's Manual: Hardware		

We would like to inform you of some points on usage of the multi-function timer pulse unit 3 (MTU3). When using this module, please apply the countermeasures listed below. The descriptions in the manual will be corrected in accord with these notes.

1. Timer Output Master Enable Register (TOER)

1.1 Usage Note

When the corresponding bit in the TOER register is changed from 1 (MTU output enabled) to 0 (MTU output disabled) while the counter is operating, a PWM waveform with a duty cycle different from that set up by the settings may be output when the corresponding bit is set to 1 again. Therefore, be sure to stop the counter first before changing a bit in the TOER register to 0.

1.2 Countermeasure

When a bit in the TOER register is changed from 1 to 0 after the counter is started, follow the procedure below.

(1) Set the bit in the timer start register (TSTR) that corresponds to the counter to 0 (which stops counting).

(2) Set the bit in the TOER register to 0.

1.3 Correction in the Manual

The following sentences are to be added to section 15.2.17, Timer Output Master Enable Register (TOER). The part in red will be added.

[After correction]

TOERA enables or disables output settings for output pins MTIOC4D, MTIOC4C, MTIOC3D, MTIOC4B, MTIOC4A, and MTIOC3B.

TOERB enables or disables output settings for output pins MTIOC7D, MTIOC7C, MTIOC6D, MTIOC7B, MTIOC7A, and MTIOC6B.

These pins do not output correctly if the TOER bits have not been set. In channels 3, 4, 6, and 7, set TOER prior to setting TIOR.

Set the MTU.TOERA register after setting the CST3 and CST4 bits in the MTU.TSTRA register.

Set the MTU.TOERB register after setting the CST0 and CST1 bits in the MTU.TSTRB register (see Figure 15.36 and Figure 15.39).

2. Timer Output Control Registers 1 (TOCR1A and TOCR1B), Timer Output Control Registers 2 (TOCR2A and TOCR2B)

2.1 Usage Note

When dead time is not to be generated, the level of the inverse-phase output is the exact inverse of the positive-phase output. At this time, only the OLSP bit is valid in the TOCR1A (TOCR1B) register, and the value of the OLSN bit is ignored. In addition, only the OLSiP bit (i = 1 to 3) is valid in the TOCR2A (TOCR2B) register, and the value of the OLSiN bit is ignored.

2.2 Countermeasure

When dead time is not to be generated, use the OLSP and OLSiP bits to control the levels of the positive-phase and inverse-phase outputs.

2.3 Correction in the Manual

Note 3 has been added to the table in section 15.2.18, Timer Output Control Registers 1 (TOCR1A and TOCR1B).

[After correction] (Only the changed parts are shown.)

Bit	Symbol	Bit Name	Description	R/W
b0	OLSP	Output Level Select P*1, *3	See Table 15.38.	R/W
b1	OLSN	Output Level Select N*1, *3	See Table 15.39.	R/W

Note 3. When dead time is not to be generated, the level of the inverse-phase output is the exact inverse of the positive-phase output. At this time, only the OLSP bit is valid.

Note 2 has been added to the table in section 15.2.19, Timer Output Control Registers 2 (TOCR2A and TOCR2B).

[After correction] (Only the changed parts are shown.)

Bit	Symbol	Bit Name	Description	R/W
b0	OLS1P	Output Level Select 1P*1, *2	This bit selects the output level on MTIOC3B or MTIOC6B in reset-synchronized PWM mode and complementary PWM mode. See Table 15.40.	R/W
b1	OLS1N	Output Level Select 1N*1, *2	This bit selects the output level on MTIOC3D or MTIOC6D in reset-synchronized PWM mode and complementary PWM mode. See Table 15.41.	R/W
b2	OLS2P	Output Level Select 2P*1, *2	This bit selects the output level on MTIOC4A or MTIOC7Ain reset-synchronized PWM mode and complementary PWM mode. See Table 15.42.	R/W
b3	OLS2N	Output Level Select 2N*1, *2	This bit selects the output level on MTIOC4C or MTIOC7C in reset-synchronized PWM mode and complementary PWM mode. See Table 15.43.	R/W
b4	OLS3P	Output Level Select 3P*1, *2	This bit selects the output level on MTIOC4B or MTIOC7B in reset-synchronized PWM mode and complementary PWM mode. See Table 15.44.	R/W
b5	OLS3N	Output Level Select 3N*1, *2	This bit selects the output level on MTIOC4D or MTIOC7D in reset-synchronized PWM mode and complementary PWM mode. See Table 15.45.	R/W
b7, b6	BF[1:0]	TOLBR Buffer Transfer Timing Select	These bits select the timing for transferring data from TOLBRj toTOCR2j. See Table 15.46 for details	R/W

Note 2. When dead time is not to be generated, the level of the inverse-phase output is the exact inverse of the positive-phase output. At this time, only the OLSiP bit is valid. (i = 1, 2, 3)

3. Connection of Cascaded Operation

3.1 Usage Note

In the case of simultaneous input capture to MTU1.TCNT and MTU2.TCNT (n = 1, 7; m = 2, 8) during cascaded operation, the signals on the corresponding input pins can be selected as input-capture conditions. In this case, the input-capture condition is an edge of the signal obtained by taking the logical OR of the two input signals. Accordingly, if the level of either signal changes while the other is being driven high, input capture does not proceed.

3.2 Countermeasure

None

3.3 Correction in the Manual

The following sentences are to be added under Table 15.59. The part in red is to be added.

[After correction]

For simultaneous input capture of MTU1.TCNT and MTU2.TCNT during cascaded operation, additional input capture input pins can be specified by the input capture control register (TICCR). The input-capture condition is detection of an edge in the signal obtained by taking the logical OR of the levels being input on the original input pin and on the additional input pin. Accordingly, if the level of either signal changes while the other is being driven high, input capture does not proceed. For details, refer to the description under (4) Cascaded Operation Example (c) in section 15.3.4, Cascaded Operation. For input capture in cascade connection, refer to section 15.6.21, Simultaneous Input Capture in MTU1.TCNT and MTU2.TCNT in Cascade Connection.

A usage note has been added to Figure 15.24.

[Before correction]

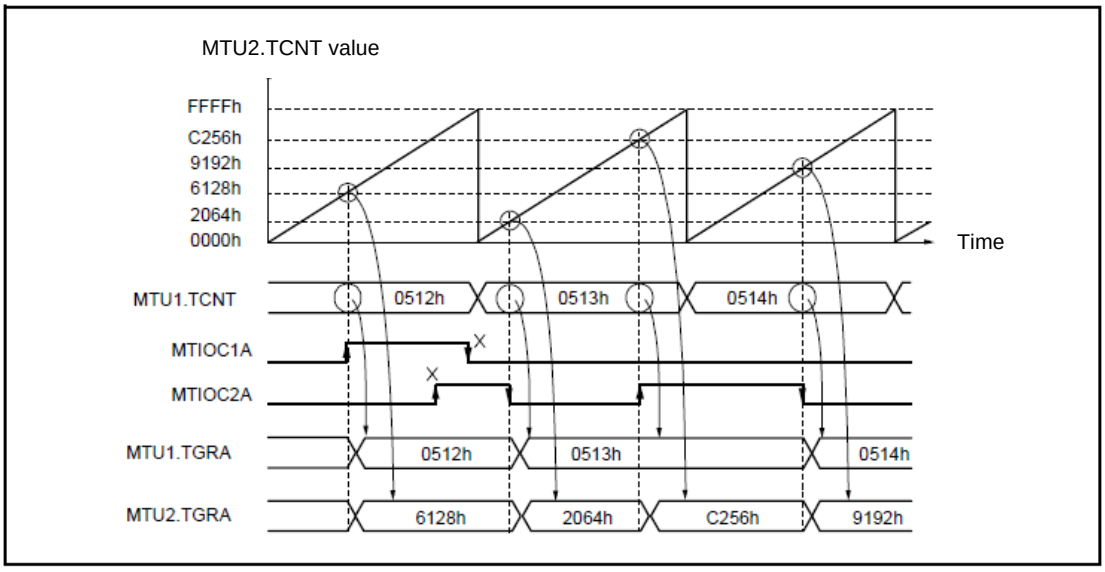
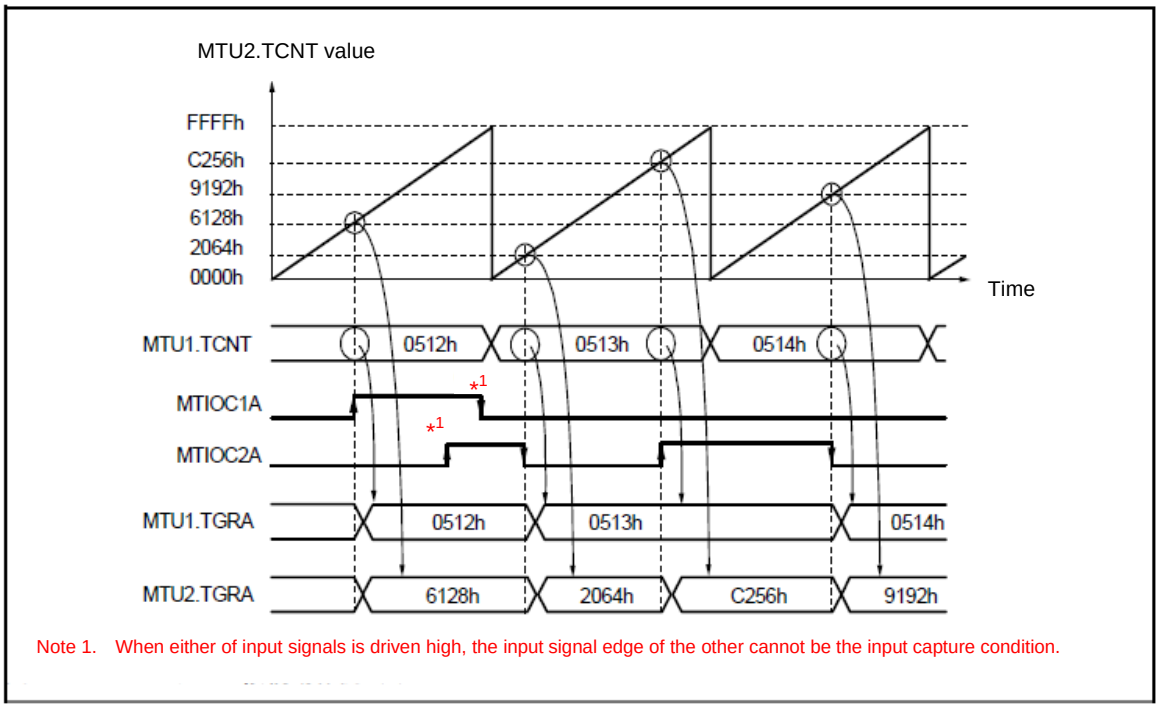


Figure 15.24 Cascaded Operation Example (c)

[After correction]



Note 1. When either of input signals is driven high, the input signal edge of the other cannot be the input capture condition.

Figure 15.24 Cascaded Operation Example (c)

4. Interrupt Timing

4.1 Usage Note

For channel 5, the TGF flag can be set even while the TCNT is stopped.

4.2 Countermeasure

None

4.3 Correction in the Manual

A note has been added to Figure 15.118, TGI Interrupt Timing (Compare Match) (Channel 5).

[After correction]

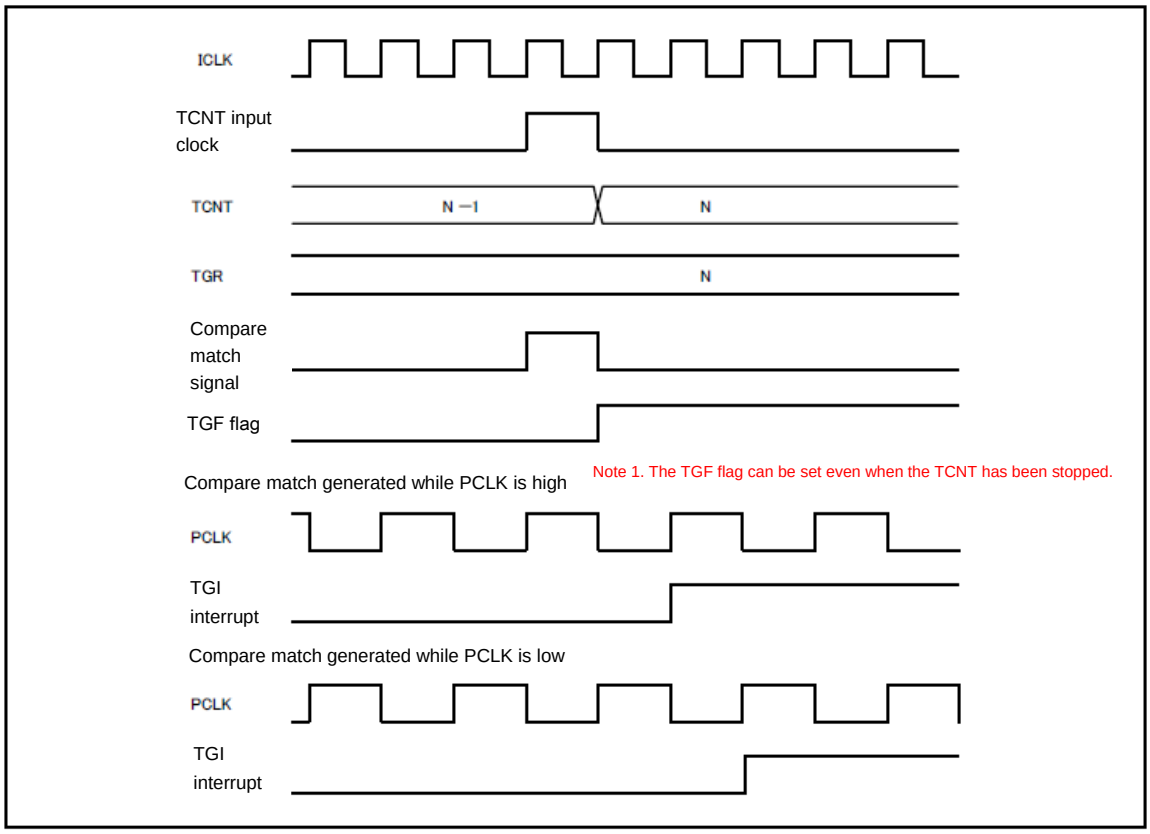


Figure 15.118 TGI Interrupt Timing (Compare Match) (Channel 5)

[Applicable Products and Related Documents]

Family	Group	Related Documents	Rev.	Control Code
RX	RX62T	RX62T Group User's Manual: Hardware	1.10	R01UH0034EJ0110