

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A011A/E	Rev.	1.00
Title	Usage Notes on the Multi-Function Timer Pulse Unit 2 (MTU2)		Information Category	Technical Notification		
Applicable Product	RX62N, RX621 Group RX630 Group RX63N, RX631 Group	Lot No.	Reference Document	Refer to the table below.		
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We would like to inform you of some points on usage of the multi-function timer pulse unit 2 (MTU2). When using this module, please apply the countermeasures listed below. The descriptions in the manual will be corrected in accord with these notes.

The corrections are explained using the RX62N Group, RX621 Group User's Manual: Hardware as an example. For the corresponding sections in other manuals, refer to Table 1, Section Numbers for the MTU2 in Manuals (listed below).

1. Timer Output Master Enable Register (TOER)

1.1 Usage Note

When the corresponding bit in the TOER register is changed from 1 (MTU output enabled) to 0 (MTU output disabled) while the counter is operating, a PWM waveform with a duty cycle different from that set up by the settings may be output when the corresponding bit is set to 1 again. Therefore, be sure to stop the counter first before changing a bit in the TOER register to 0.

1.2 Countermeasure

When a bit in the TOER register is changed from 1 to 0 after the counter is started, follow the procedure below.

- (1) Set the bit in the timer start register (TSTR) that corresponds to the counter to 0 (which stops counting).
- (2) Set the bit in the TOER register to 0.

1.3 Correction in the Manual

The following sentences are to be added to section 17.2.17, Timer Output Master Enable Register (TOER). The part in red will be added.

[After correction]

TOERA enables or disables output settings for output pins MTIOC4D, MTIOC4C, MTIOC3D, MTIOC4B, MTIOC4A, and MTIOC3B.

TOERB enables or disables output settings for output pins MTIOC10D, MTIOC10C, MTIOC9D, MTIOC10B, MTIOC10A, and MTIOC9B.

These pins do not output correctly if the TOER bits have not been set. In channels 3, 4, 9, and 10, set TOER prior to setting TIOR.

Set the MTUA.TOER register after setting the CST3 and CST4 bits in the MTUA.TSTR register.

Set the MTUB.TOER register after setting the CST0 and CST1 bits in the MTU.TSTRB register (see Figure 17.36 and Figure 17.39).

2. Timer Output Control Register 1 (TOCR1), Timer Output Control Register 2 (TOCR2)

2.1 Usage Note

When dead time is not to be generated, the level of the inverse-phase output is the exact inverse of the positive-phase output. At this time, only the OLSP bit is valid in the TOCR1 register, and the value of the OLSN bit is ignored. In addition, only the OLSiP bit (i = 1 to 3) is valid in the TOCR2 register, and the value of the OLSiN bit is ignored.

2.2 Countermeasure

When dead time is not to be generated, use the OLSP and OLSiP bits to control the levels of the positive-phase and inverse-phase outputs.

2.3 Correction in the Manual

Note 3 has been added to the table in section 17.2.18, Timer Output Control Register 1 (TOCR1).

[After correction] (Only the changed parts are shown.)

Bit	Symbol	Bit Name	Description	R/W
b0	OLSP	Output Level Select P ^{*2, *3}	See Table 17.32.	R/W
b1	OLSN	Output Level Select N ^{*2, *3}	See Table 17.33.	R/W

Note 3. When dead time is not to be generated, the level of the inverse-phase output is the exact inverse of the positive-phase output. At this time, only the OLSP bit is valid.

Note 2 has been added to the table in section 17.2.19, Timer Output Control Register 2 (TOCR2).

[After correction] (Only the changed parts are shown.)

Bit	Symbol	Bit Name	Description	R/W
b0	OLS1P	Output Level Select 1P ^{*1, *2}	This bit selects the output level on MTIOC3B in reset-synchronized PWM mode and complementary PWM mode. See Table 17.34.	R/W
b1	OLS1N	Output Level Select 1N ^{*1, *2}	This bit selects the output level on MTIOC3D in reset-synchronized PWM mode and complementary PWM mode. See Table 17.35.	R/W
b2	OLS2P	Output Level Select 2P ^{*1, *2}	This bit selects the output level on MTIOC4A in reset-synchronized PWM mode and complementary PWM mode. See Table 17.36.	R/W
b3	OLS2N	Output Level Select 2N ^{*1, *2}	This bit selects the output level on MTIOC4C in reset-synchronized PWM mode and complementary PWM mode. See Table 17.37.	R/W
b4	OLS3P	Output Level Select 3P ^{*1, *2}	This bit selects the output level on MTIOC4B in reset-synchronized PWM mode and complementary PWM mode. See Table 17.38.	R/W
b5	OLS3N	Output Level Select 3N ^{*1, *2}	This bit selects the output level on MTIOC4D in reset-synchronized PWM mode and complementary PWM mode. See Table 17.39.	R/W
b7, b6	BF[1:0]	TOLBR Buffer Transfer Timing Select	These bits select the timing for transferring data from TOLBRj to TOCR2. See Table 17.40 for details.	R/W

Note Only unit 0 is described here because channels 9 and 10 (unit 1) have the same functions as those of channels 3 and 4 (unit 0), respectively.

Note 1. Setting the TOCR1.TOCS bit to 1 makes this bit setting valid.

Note 2. When dead time is not to be generated, the level of the inverse-phase output is the exact inverse of the positive-phase output. At this time, only the OLSiP bit is valid. (i = 1, 2, 3)

3. Synchronous Counter Clearing Output Waveform Control in Complementary PWM Mode

3.1 Usage Note

When the TWCR.WRE bit is 1 (the output levels of the waveform directly before synchronous clearing are retained) in complementary PWM mode, the following phenomena will occur if the respective condition (1) or (2) is satisfied.

Condition (1): For the initial-output suppression interval labeled (10) in Figure 1, synchronous clearing is generated in the dead-time interval for PWM output.

Condition (2): If any of the duty-cycle registers (MTU3.TGRB, MTU4.TGRA, MTU4.TGRB, MTU9.TGRB, MTU10.TGRA, MTU10.TGRB) is set to a value less than that in the dead-time register (TDDR), synchronous clearing is generated in the initial-output suppression interval labeled (10) and (11) in Figure 2.

Phenomena

- The dead time interval is shortened (or eliminated) on the PWM output pin.
- The active level is output on the PWM inverse-phase output pin beyond the period for output of the active level.

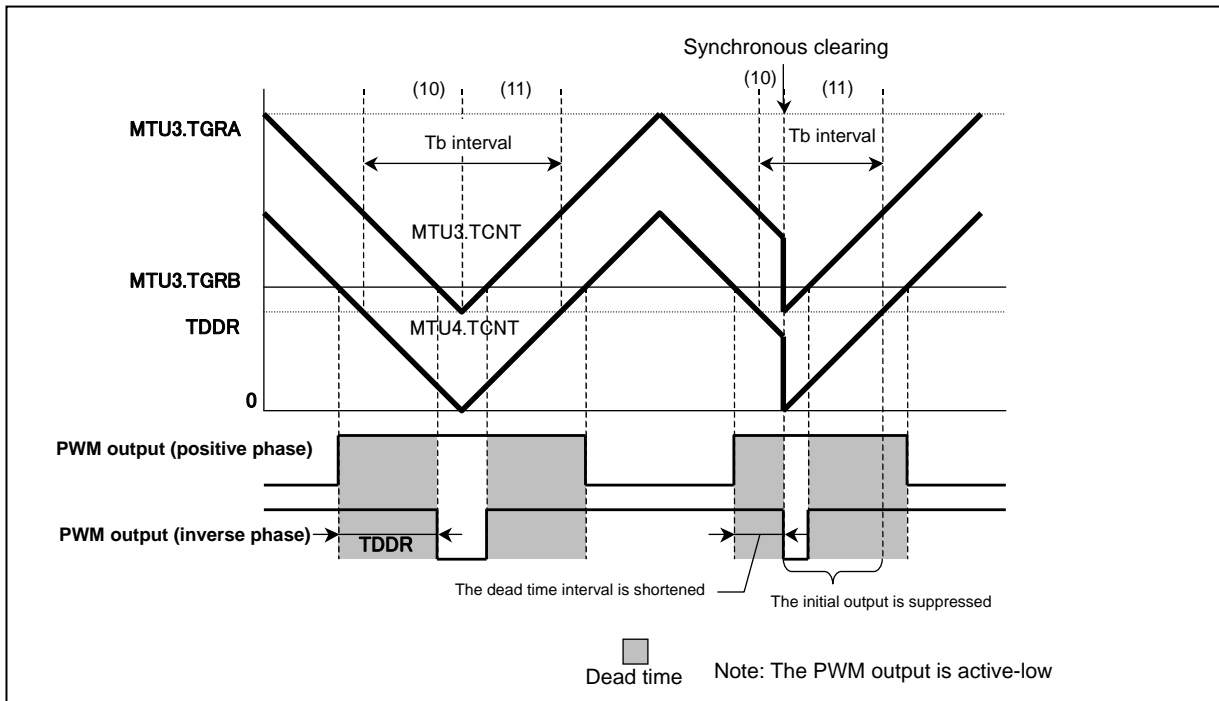


Figure 1 Synchronous Clearing under Condition (1)

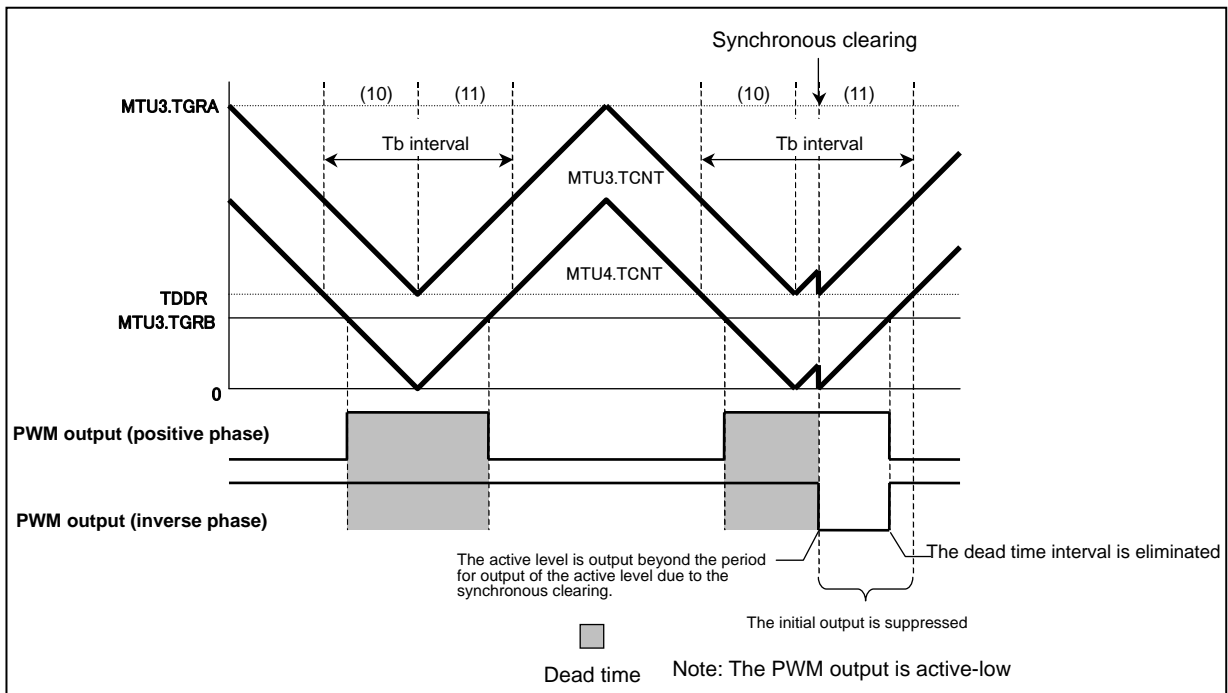


Figure 2 Synchronous Clearing under Condition (2)

3.2 Countermeasure

When the value of the TWCR.WRE bit is 1, ensure that synchronous clearing proceeds when the values of the registers satisfy the conditions below.

$$MTU3.TGRB \geq TDDR \times 2, MTU4.TGRA \geq TDDR \times 2, MTU4.TGRB \geq TDDR \times 2$$

3.3 Correction in the Manual

- The descriptions of the WRE bit under "Bit Name" and "Description" in section 17.2.30, Timer Waveform Control Register (TWCR), have been changed as shown below.

[Before correction] (Only the changed parts are shown.)

Bit	Symbol	Bit Name	Description	R/W
b0	WRE	Waveform Retain Enable	0: Initial value specified in TOCR is output 1: Waveform output immediately before synchronous clearing is retained	R/(W)

[After correction] (Only the changed parts are shown.)

Bit	Symbol	Bit Name	Description	R/W
b0	WRE	Initial Output Suppression Enable	0: Initial value specified in TOCR is output 1: The initial output is suppressed.	R/(W)

- The description of the WRE bit in section 17.2.30, Timer Waveform Control Register (TWCR), has also been changed.

[Before correction] (Only the changed parts are shown.)

WRE Bit (Waveform Retain Enable)

This bit selects the waveform output when synchronous counter clearing occurs in complementary PWM mode.

The output waveform is retained only when synchronous clearing occurs within the T_b interval at the trough in complementary PWM mode.

[After correction] (Only the changed parts are shown.)

WRE Bit (Initial Output Suppression Enable)

This bit selects the waveform output when synchronous counter clearing occurs in complementary PWM mode.

The initial output is prevented with this function only when synchronous clearing occurs within the T_b interval at the trough in complementary PWM mode.

4. Connection of Cascaded Operation

4.1 Usage Note

In the case of simultaneous input capture to MTUn.TCNT and MTUm.TCNT ($n = 1, 7; m = 2, 8$) during cascaded operation, the signals on the corresponding input pins can be selected as input-capture conditions. In this case, the input-capture condition is an edge of the signal obtained by taking the logical OR of the two input signals. Accordingly, if the level of either signal changes while the other is being driven high, input capture does not proceed.

4.2 Countermeasure

None

4.3 Correction in the Manual

The following sentences are to be added under Table 17.46. The part in red is to be added.

[After correction]

For simultaneous input capture of MTUn.TCNT and MTUm.TCNT during cascaded operation, additional input capture input pins can be specified by the input capture control register (TICCR). **The input-capture condition is detection of an edge in the signal obtained by taking the logical OR of the levels being input on the original input pin and on the additional input pin. Accordingly, if the level of either signal changes while the other is being driven high, input capture does not proceed. For details, refer to the description under (4) Cascaded Operation Example (c) in section 17.3.4, Cascaded Operation.** For input capture in cascade connection, refer to section 17.6.20, Simultaneous Input Capture in MTUn.TCNT and MTUm.TCNT in Cascade Connection.

- A usage note has been added to Figure 17.23.

[Before correction]

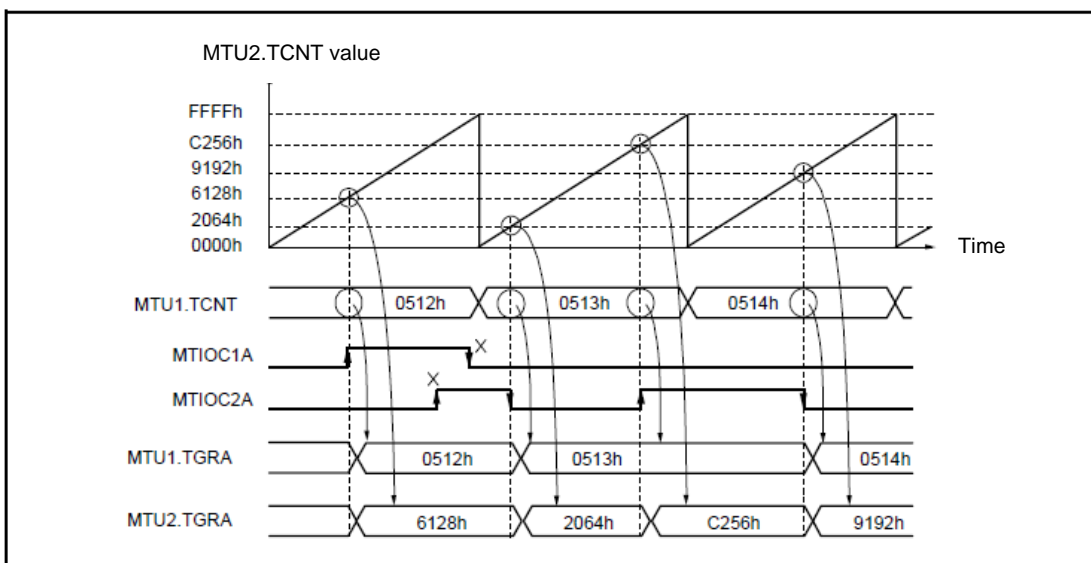
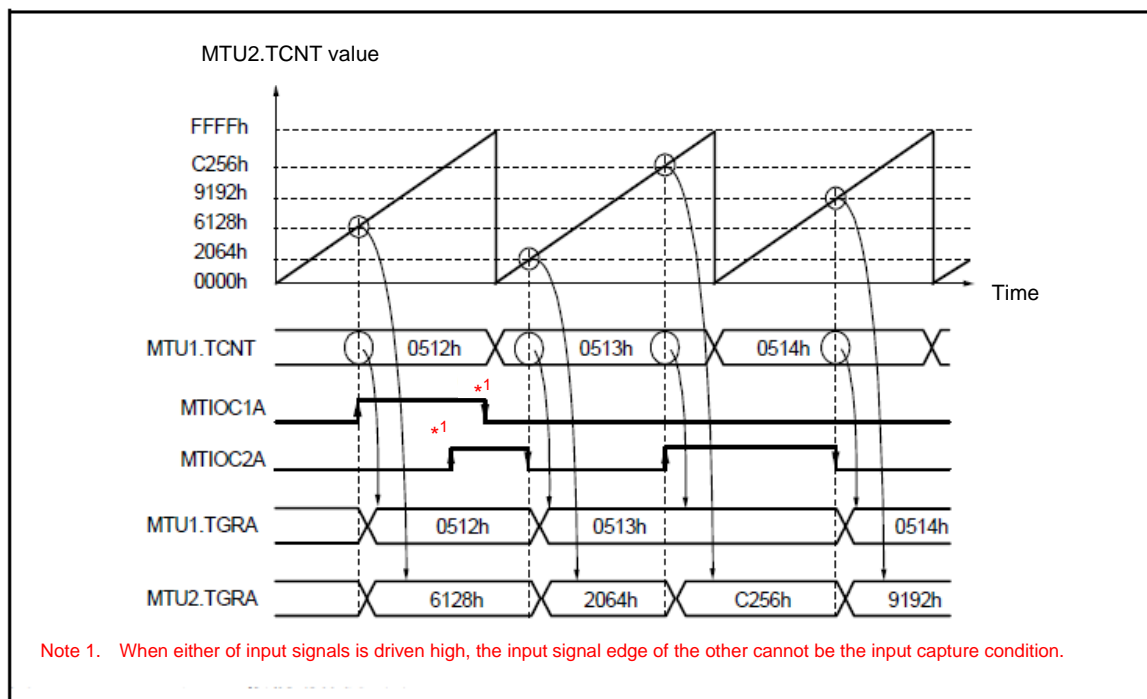


Figure 17.23 Cascaded Operation Example (c)

[After correction]



Note 1. When either of input signals is driven high, the input signal edge of the other cannot be the input capture condition.

Figure 17.23 Cascaded Operation Example (c)

5. Complementary PWM Mode

5.1 Usage Note

Data from the buffer register are transferred to the temporary register in the interval over which buffer transfer is enabled. Accordingly, if a new value is written to the buffer during the interval from an interrupt request to within one cycle of the carrier, the data are immediately transferred to the temporary register, and transfer to the compare register proceeds if the value in TCNTS matches that in MTUn.TGRA the next time the former counts up.

If a new value is written to the buffer after one cycle of the carrier following the generation of an interrupt request, the data are transferred to the temporary register during the interval over which buffer transfer is enabled, and transfer to the compare register proceeds if the value in TCNTS matches that in MTUn.TGRA the next time the former counts up.

5.2 Countermeasure

None

5.3 Correction in the Manual

Figure 17.71, Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE1 = 1 and BTE0 = 0) (Unit 0), was incorrect and is thus corrected as shown below.

[Before correction]

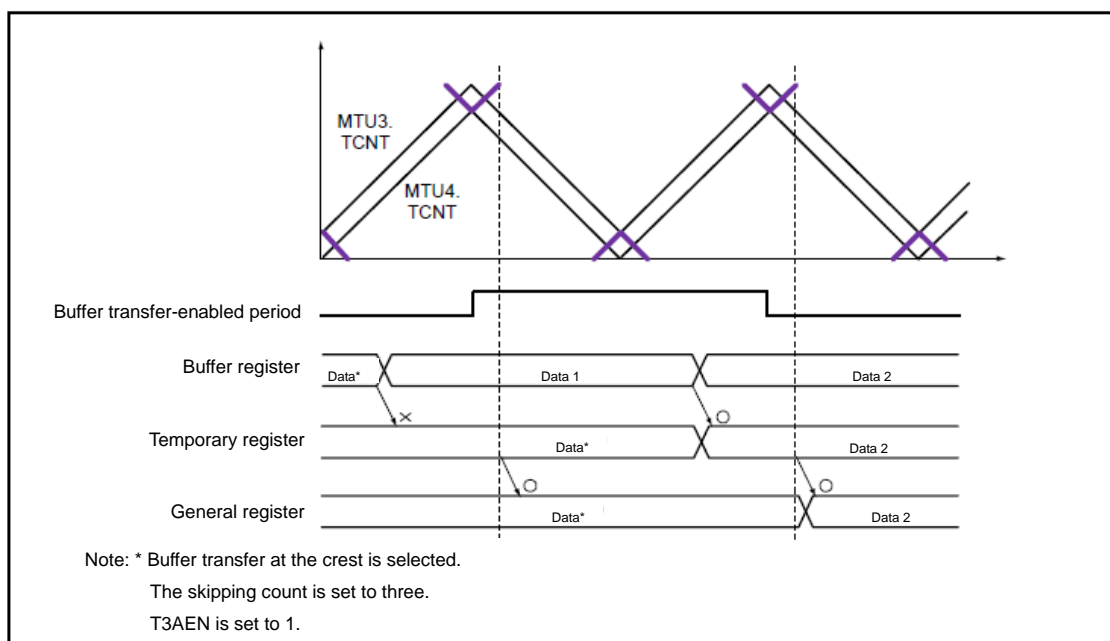


Figure 17.71 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE1 = 1 and BTE0 = 0) (Unit 0)

[After correction]

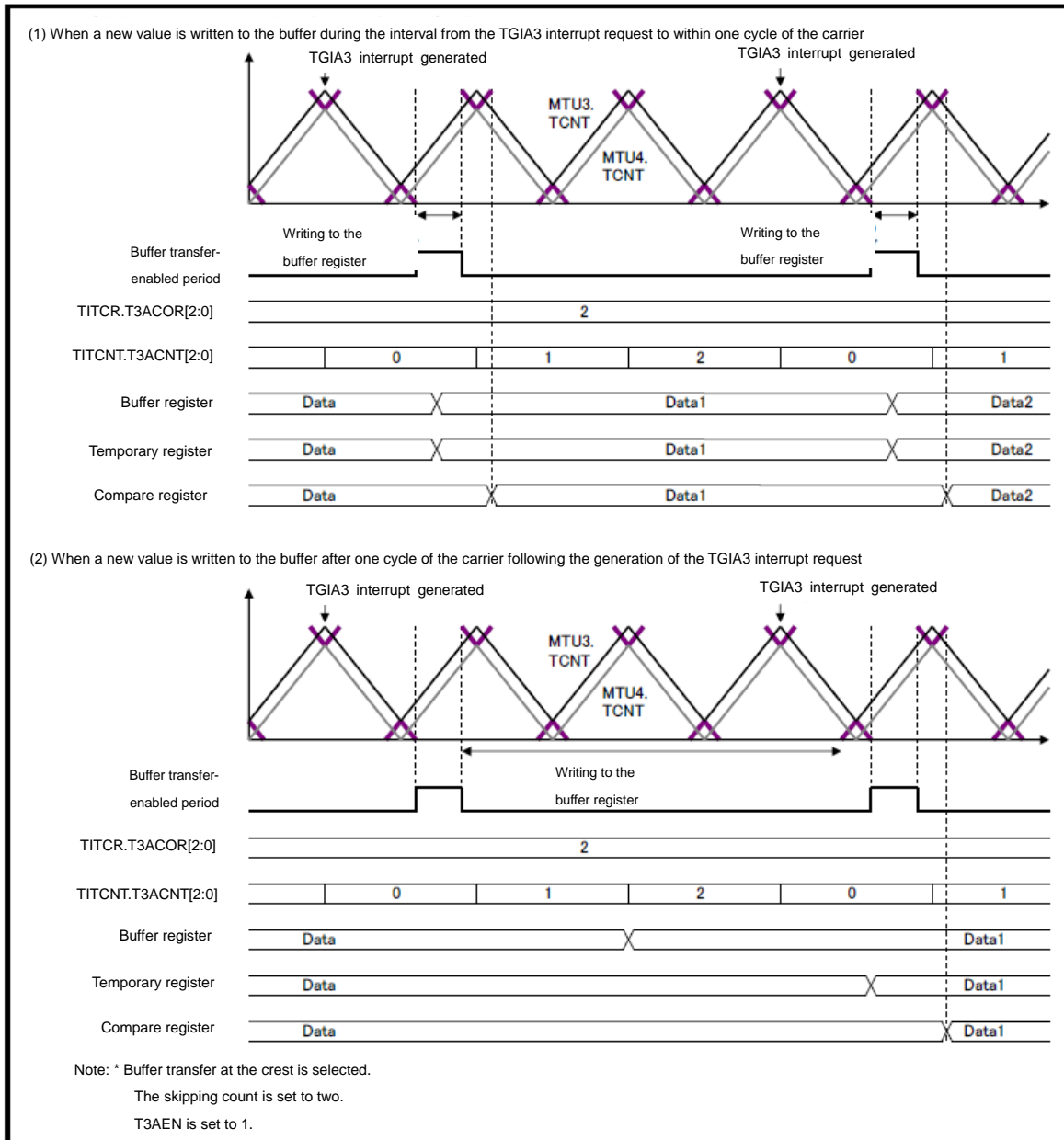


Figure 17.71 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE1 = 1 and BTE0 = 0) (Unit 0)

6. Interrupt Timing

6.1 Usage Note

For channels 5 and 11, the compare match can be generated even while the TCNT is stopped.

6.2 Countermeasure

None

6.3 Correction in the Manual

A note has been added to Figure 17.100, TGI Interrupt Timing (Compare Match) (Channel 5 or 11).

[After correction]

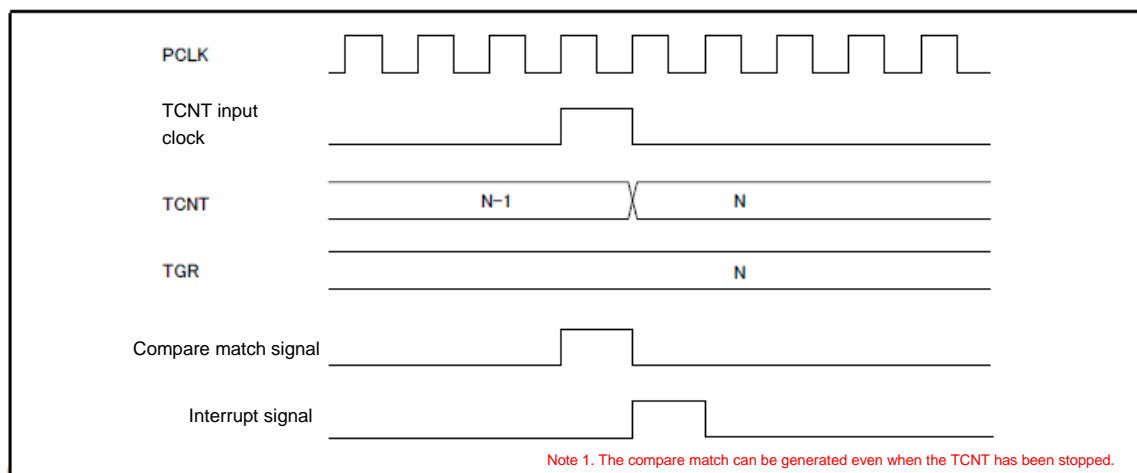


Figure 17.100 TGI Interrupt Timing (Compare Match) (Channel 5 or 11)

Table 1 Section Numbers for the MTU2 in Manuals

Group	Related Documents	Rev.	Control Code	Section No. for the MTU2
RX62N, RX621	RX62N Group, RX621 Group User's Manual: Hardware	1.20	R01UH0033EJ0120	17
RX630	RX630 Group User's Manual: Hardware	1.10	R01UH0040EJ0110	21
RX63N, RX631	RX63N Group, RX631 Group User's Manual: Hardware	0.90	R01UH0041EJ0090	22