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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A119A/E	Rev.	1.00
Title	Usage Notes on A/D Conversion Delaying Function of MTU3		Information Category	Technical Notification		
Applicable Product	RX62T, RX62G Group RX63T Group RX64M Group	Lot No. All lots	Reference Document	See below.		

Usage notes on the multi-function timer pulse unit 3 (MTU3, MTU3a) for the products listed below are as follows.

According to this update, relevant manuals are revised. The details of the corrections are described as follows based on the user's manual: hardware of the RX62T group and RX62G group.

See the section of Applicable Products and Relevant Documents in the last section for the corrections of the manuals in other groups.

[Notes]

1. A/D Converter Start Request Enabled Interval in A/D Conversion Delaying Function

- If the UTnAE or UTnBE bit in MTUn.TADCR is set to 1 in complementary PWM mode, A/D converter start requests are enabled during the MTUn.TCNT up-counting period. The A/D converter start request enabled interval is: 0 ≤ MTUn.TCNT ≤ TCDR - 1.
- If the DTnAE or DTnBE bit in MTUn.TADCR is set to 1 in complementary PWM mode, A/D converter start requests are enabled during the MTUn.TCNT down-counting period. The A/D converter start request enabled interval is: TCDR ≥ MTUn.TCNT ≥ 1.
- Clear the DTnAE and DTnBE bits in MTUn.TADCR to 0 when not in complementary PWM mode. Setting the UTnAE or UTnBE bit in MTUn.TADCR to 1 causes an A/D converter start request to be generated at a compare match between MTUn.TCNT and MTUn.TADCORA/MTUn.TADCORB, regardless of whether MTUn.TCNT is counting up or down (n = 4, 7).

2. Notes on A/D Converter Start Request Delaying Function in Complementary PWM Mode

- When MTUn.TADCOBRA/MTUn.TADCOBRB is set to 0 and the UTnAE or UTnBE bit in MTUn.TADCR is set to 1, and the result is transferred to the buffer when counting by MTUn.TCNT reaches its trough, an A/D converter start request is not generated during the up-counting period immediately following the transfer (Figure 2.1).
- When the same value as that of TCDR is set to MTUn.TADCOBRA or MTUn.TADCOBRB and the DTnAE or DTnBE bit in MTUn.TADCR is set to 1, and the result is transferred to the buffer when counting by MTUn.TCNT reaches its crest, an A/D converter start request is not generated during the down-counting period immediately following the transfer (Figure 2.2).

- When A/D converter start requests are linked to the interrupt skipping function, set MTUn.TADCORA or MTUn.TADCORB to meet the condition 2 ≤ MTUn.TADCORA or MTUn.TADCORB ≤ TCDR - 2 (n = 4, 7).

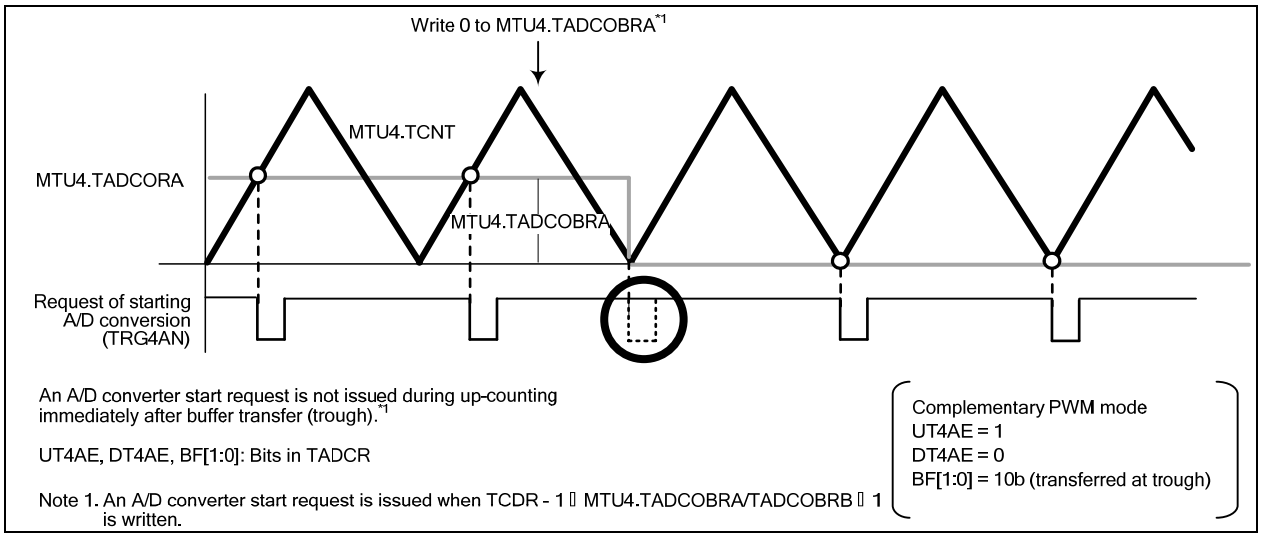

Figure 2.1 A/D Converter Start Request When 0 is Written to MTU4.TADCOBRA

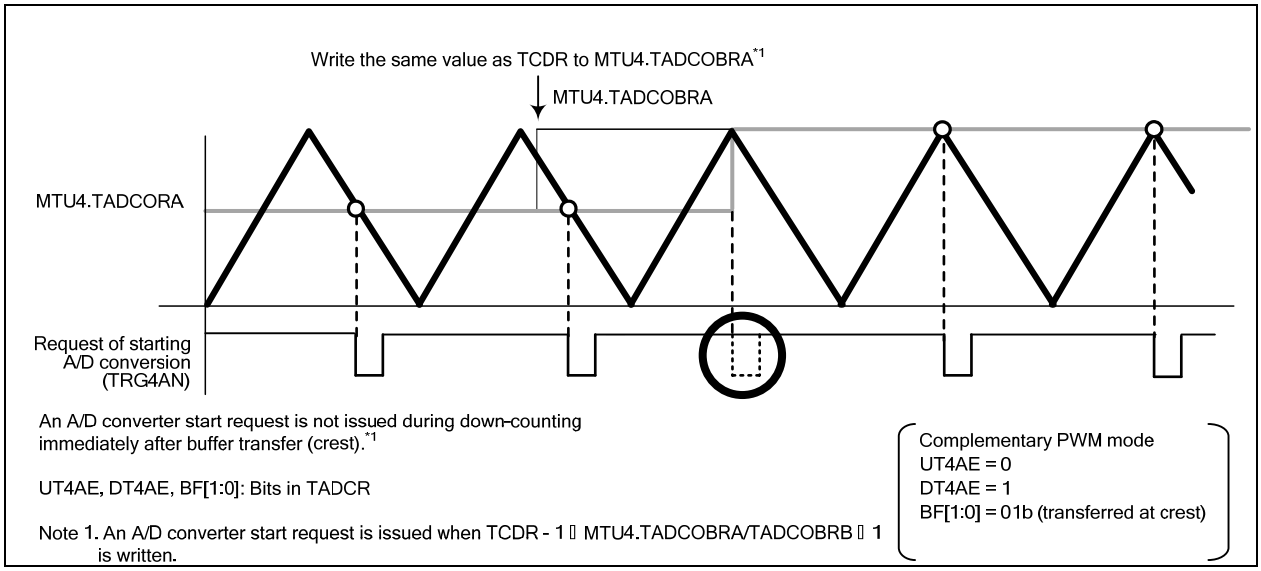

Figure 2.2 A/D Converter Start Request When the Same Value as TCDR is Written to MTU4.TADCOBRA

16.2.29 Timer A/D Converter Start Request Control Register (TADCR)

<Before correction (p. 538)>

TADCR (MTU4)

Address: 000C 1240h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
Value after reset	0	0	0	0	0	0	0	0	0	0*4	0	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	Bit Name	Description	R/W
b0	ITB4VE*4	TCIV4 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are linked	R/W
b1	ITB3AE*4	TGIA3 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are linked	R/W
b2	ITA4VE*4	TCIV4 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are linked	R/W
b3	ITA3AE*4	TGIA3 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are linked	R/W
b4	DT4BE*4	Down-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT down-count operation	R/W
b5	UT4BE	Up-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT up-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT up-count operation	R/W
b6	DT4AE*4	Down-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b7	UT4AE	Up-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT up-count operation 1: A/D converter up requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU4.TADCOBRA/B Transfer Timing Select	See Table 16.49 for details. These bits specify the transfer timing from MTU4.TADCOBRA and MTU4.TADCOBRB to MTU4.TADCORA and MTU4.TADCORB.	R/W

Note 1. MTU4.TADCR must not be accessed in eight bits; it should always be accessed in 16 bits.

Note 2. When interrupt skipping is disabled (the T3AEN and T4VEN bits in TITCR1A are cleared to 0 or the T3ACOR and T4VCOR bits in TITCR1A are cleared to 0), do not link A/D converter start requests with interrupt skipping function 1 (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in MUT3_4.TADCR to 0).

Note 3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.

Note 4. Do not set to 1 in other than complementary PWM mode.

<After correction>

TADCR (MTU4)

Address: 000C 1240h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
Value after reset	0	0	0	0	0	0	0	0	0	0*4	0	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	Bit Name	Description	R/W
b0	ITB4VE*4, *2, *3	TCIV4 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are linked	R/W
b1	ITB3AE*4 *2, *3	TGIA3 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are linked	R/W
b2	ITA4VE*4 *2, *3	TCIV4 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are linked	R/W
b3	ITA3AE*4 *2, *3	TGIA3 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are linked	R/W
b4	DT4BE*4	Down-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT down-count operation	R/W
b5	UT4BE	Up-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT up-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT up-count operation	R/W
b6	DT4AE*4	Down-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b7	UT4AE	Up-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT up-count operation 1: A/D converter up requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are always read as 0. The write value should be 0	R/W
b15, b14	BF[1:0]	MTU4.TADCOBRA/B Transfer Timing Select	See Table 16.49 for details. These bits specify the transfer timing from MTU4.TADCOBRA and MTU4.TADCOBRB to MTU4.TADCORA and MTU4.TADCORB.	R/W

Note 1. MTU4.TADCR must not be accessed in 8 bits; it should be accessed in 16 bits.

Note 2. Set to 0 when interrupt skipping is disabled (the T3AEN and T4VEN bits in TITCR1A are cleared to 0 or the T3ACOR and T4VCOR bits in TITCR1A are cleared to 0).

Note 3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.

Note 4. Set to 0 when complementary PWM mode is not selected.

<Before correction (p. 539)>

Table 16.49 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU4)

Bit 15	Bit 14	
BF[1]	**BF[0]**	**Description**
0	0	Does not transfer data from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB).
0	1	Transfers data from the cycle set buffer register to the cycle set register at the crest of the MTU4.TCNT count.*1
1	0	Transfers data from the cycle set buffer register to the cycle set register at the trough of the MTU4.TCNT count.*2
1	1	Transfers data from the cycle set buffer register to the cycle set register at the crest and trough of the MTU4.TCNT count.*2

Note 1. Data is transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB) when the crest of the MTU4.TCNT count is reached or the MTU4.TGRD is written to in complementary PWM mode, when a compare match occurs between MTU3.TCNT and MTU3.TGRA in reset-synchronized PWM mode, or when a compare match occurs between MTU4.TCNT and MTU4.TGRA in PWM mode 1 or normal operation mode.

Note 2. These settings are prohibited when complementary PWM mode is not selected.

<After correction>

Table 16.49 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU4)

Bit 15	Bit 14	Description	
BF1	BF0	Complementary PWM Mode	Reset Synchronous PWM Mode
0	0	Does not transfer data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB)	Does not transfer data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB)
0	1	Transfers data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB) at the crest of MTU4.TCNT	Transfers data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB) at a compare match between MTU3.TCNT and MTU3.TGRA
1	0	Transfers data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB) at the trough of MTU4.TCNT	Setting prohibited
1	1	Transfers data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB) at the crest and trough of MTU4.TCNT	Setting prohibited

Bit 15	Bit 14	Description	
BF1	BF0	PWM Mode 1	Normal Mode
0	0	Does not transfer data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB)	Does not transfer data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB)
0	1	Transfers data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB) at a compare match between MTU4.TCNT and MTU4.TGRA	Transfers data from the cycle set buffer register (MTU4.TADCOBRA/MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA/MTU4.TADCORB) at a compare match between MTU4.TCNT and MTU4.TGRA
1	0	Setting prohibited	Setting prohibited
1	1	Setting prohibited	Setting prohibited

<Before correction (p. 540)>

TADCR (MTU7)

Address: 000C 1A40h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT7AE	DT7AE	UT7BE	DT7BE	ITA6AE	ITA7VE	ITB6AE	ITB7VE
Value after reset	0	0	0	0	0	0	0	0	0	0*4	0	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	Bit Name	Description	R/W
b0	ITB7VE*4	TCIV7 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are linked	R/W
b1	ITB6AE*4	TGIA6 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are linked	R/W
b2	ITA7VE*4	TCIV7 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are linked	R/W
b3	ITA6AE*4	TGIA6 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are linked	R/W
b4	DT7BE*4	Down-Count TRG7BN Enable	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT down-count operation	R/W
b5	DT7AE	Up-Count TRG7BN Enable	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT up-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT up-count operation	R/W
b6	DT7AE*4	Down-Count TRG7AN Enable	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b7	UT7AE	Up-Count TRG7AN Enable	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT up-count operation 1: A/D converter up requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU7.TADCOBRA/B Transfer Timing Select	See Table 16.50 for details. These bits specify the transfer timing from MTU7.TADCOBRA and MTU7.TADCOBRB to MTU7.TADCORA and MTU7.TADCORB.	R/W

Note 1. MTU7.TADCR must not be accessed in eight bits; it should always be accessed in 16 bits.

Note 2. When interrupt skipping is disabled (the T6AEN and T7VEN bits in TITCR1B are cleared to 0 or the T6ACOR and T7VCOR bits in TITCR1B are cleared to 0), do not link A/D converter start requests with interrupt skipping function 1 (clear the ITA6AE, ITA7VE, ITB6AE, and ITB7VE bits in MUT3_7.TADCR to 0).

Note 3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.

Note 4. Do not set to 1 in other than complementary PWM mode.

<After correction>

TADCR (MTU7)

Address: 000C 1A40h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT7AE	DT7AE	UT7BE	DT7BE	ITA6AE	ITA7VE	ITB6AE	ITB7VE
Value after reset	0	0	0	0	0	0	0	0	0	0*4	0	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	Bit Name	Description	R/W
b0	ITB7VE*4 *2, *3	TCIV7 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are linked	R/W
b1	ITB6AE*4 *2, *3	TGIA6 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are linked	R/W
b2	ITA7VE*4 *2, *3	TCIV7 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are linked	R/W
b3	ITA6AE*4 *2, *3	TGIA6 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are linked	R/W
b4	DT7BE*4	Down-Count TRG7BN Enable	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT down-count operation	R/W
b5	DT7BE	Up-Count TRG7BN Enable	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT up-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT up-count operation	R/W
b6	DT7AE*4	Down-Count TRG7AN Enable	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b7	UT7AE	Up-Count TRG7AN Enable	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT up-count operation 1: A/D converter up requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU7.TADCOBRA/B Transfer Timing Select	See Table 16.50 for details. These bits specify the transfer timing from MTU7.TADCOBRA and MTU7.TADCOBRB to MTU7.TADCORA and MTU7.TADCORB.	R/W

Note 1. MTU7.TADCR must not be accessed in 8 bits; it should be accessed in 16 bits.

Note 2. Set to 0 when interrupt skipping is disabled (the T6AEN and T7VEN bits in TITCR1B are cleared to 0 or the T6ACOR and T7VCOR bits in TITCR1B are cleared to 0)..

Note 3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.

Note 4. Set to 0 when complementary PWM mode is not selected.

<Before correction (p. 541)>

Table 16.50 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU7)

Bit 15	Bit 14	
BF[1]	**BF[0]**	**Description**
0	0	Does not transfer data from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB).
0	1	Transfers data from the cycle set buffer register to the cycle set register at the crest of the MTU7.TCNT count.*1
1	0	Transfers data from the cycle set buffer register to the cycle set register at the trough of the MTU7.TCNT count.*2
1	1	Transfers data from the cycle set buffer register to the cycle set register at the crest and trough of the MTU7.TCNT count.*2

Note 1. Data is transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB) when the crest of the MTU7.TCNT count is reached or the MTU7.TGRD is written to in complementary PWM mode, when a compare match occurs between MTU6.TCNT and MTU6.TGRA in reset-synchronized PWM mode, or when a compare match occurs between MTU7.TCNT and MTU7.TGRA in PWM mode 1 or normal operation mode.

Note 2. These settings are prohibited when complementary PWM mode is not selected.

<After correction>

Table 16.50 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU7)

Bit 15	Bit 14	Description	
BF1	BF0	Complementary PWM Mode	Reset Synchronous PWM Mode
0	0	Does not transfer data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB)	Does not transfer data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB)
0	1	Transfers data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB) at the crest of MTU7.TCNT	Transfers data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB) at a compare match between MTU6.TCNT and MTU6.TGRA
1	0	Transfers data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB) at the trough of MTU7.TCNT	Setting prohibited
1	1	Transfers data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB) at the crest and trough of MTU7.TCNT	Setting prohibited

Bit 15	Bit 14	Description	
BF1	BF0	PWM Mode 1	Normal Mode
0	0	Does not transfer data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB)	Does not transfer data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB)
0	1	Transfers data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB) at a compare match between MTU7.TCNT and MTU7.TGRA	Transfers data from the cycle set buffer register (MTU7.TADCOBRA/MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA/MTU7.TADCORB) at a compare match between MTU7.TCNT and MTU7.TGRA
1	0	Setting prohibited	Setting prohibited
1	1	Setting prohibited	Setting prohibited

16.3.9 A/D Converter Start Request Delaying Function

(1) Example of Procedure for Specifying A/D Converter Start Request Delaying Function

<Before correction (p.627)>

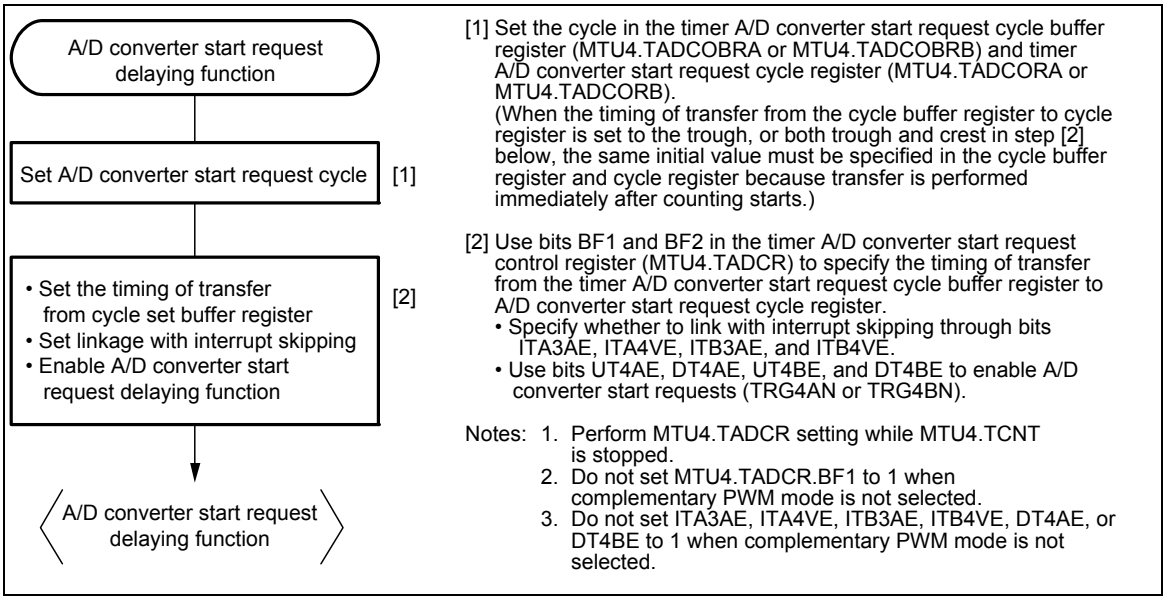

Figure 16.83 Example of Procedure for Specifying A/D Converter Start Request Delaying Function

<After correction>

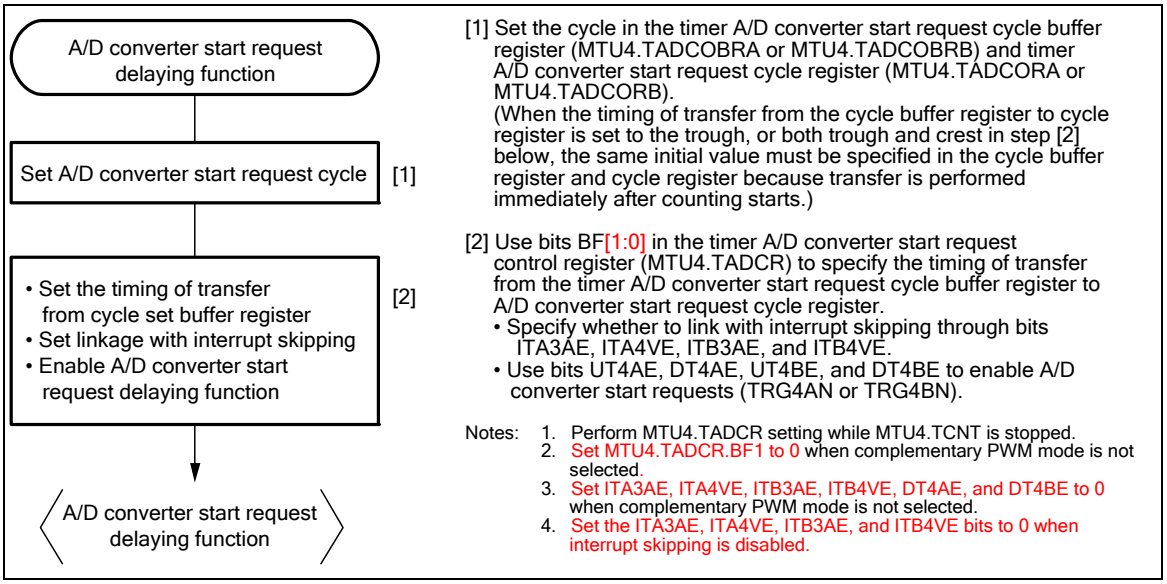

Figure 16.83 Example of Procedure for Specifying A/D Converter Start Request Delaying Function

(2) Basic Example of A/D Converter Start Request Delaying Function Operation

<Before correction (p.628)>

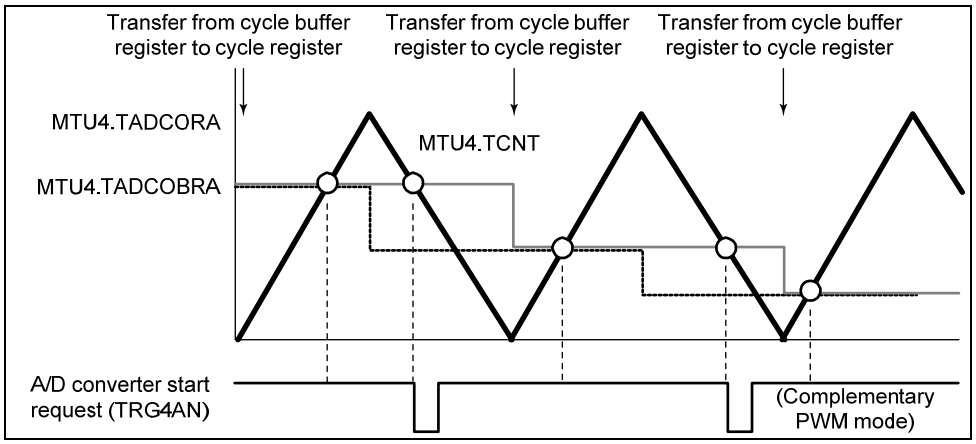

Figure 16.84 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation

<After correction>

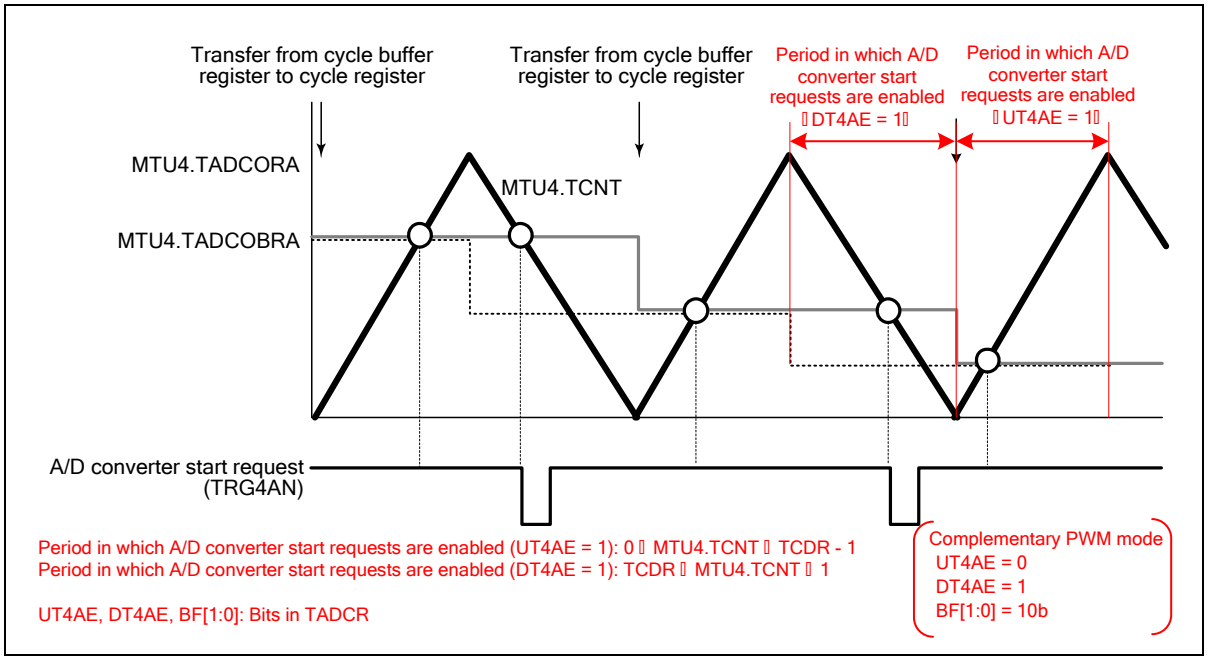

Figure 16.84 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation

<Addition>

(3) A/D converter Start Request Enabled Interval

When the MTU4.TCNT (MTU7.TCNT) counter and the MTU4.TADCORA or MTU4.TADCORB (MTU7.TADCORA or MTU7.TADCORB) register matches within the period enabled by the UT4AE and UT4BE (UT7AE and UT7BE) bits, the corresponding A/D converter start request (TRG4AN or TRG4BN) is issued.

When the UT4AE and UT4BE (UT7AE and UT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1 in complementary PWM mode, A/D converter start requests are enabled during the MTU4.TCNT (MTU7.TCNT) upcounting (0 □ MTU4.TCNT (MTU7.TCNT) □ TCDR - 1). When the DT4AE and DT4BE (DT7AE and DT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1, A/D converter start requests are enabled during MTU4.TCNT (MTU7.TCNT) down-counting (TCDR □ MTU4.TCNT (MTU7.TCNT) □ 1). See Figure 16.84.

(3) Buffer Transfer

The title is changed to “(4) Buffer Transfer”.

<Before correction (p.629)>

The data in the timer A/D converter start request cycle set registers (MTU4.TADCORA and MTU4.TADCORB, or MTU7.TADCORA and MTU7.TADCORB) is updated by writing data to the timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA and MTU4.TADCOBRB, or MTU7.TADCOBRA and MTU7.TADCOBRB). Data is transferred from the buffer registers to the respective cycle set registers at the timing selected with the BF[1:0] bits in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR).

In complementary PWM mode, data is also transferred from the timer A/D converter start request cycle set buffer registers to the timer A/D converter start request cycle set registers when timer general register D (MTU4.TGRD or MTU7.TGRD) is updated.

<After correction>

The data in the timer A/D converter start request cycle set registers (MTU4.TADCORA and MTU4.TADCORB, or MTU7.TADCORA and MTU7.TADCORB) is updated by writing data to the timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA and MTU4.TADCOBRB, or MTU7.TADCOBRA and MTU7.TADCOBRB). Data is transferred from the buffer registers to the respective cycle set registers at the timing selected with the BF[1:0] bits in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR).

In complementary PWM mode, data is also transferred from the timer A/D converter start request cycle set buffer registers to the timer A/D converter start request cycle set registers when timer general register D (MTU4.TGRD or MTU7.TGRD) is updated.

There are notes on the timing for transferring data when using buffer transfer in complementary PWM mode.

For details, section 16.6.26, Usage Notes on A/D Converter Delaying Function in Complementary PWM Mode.

In modes other than complementary PWM mode, set the BF1 bit in the MTU4.TADCR (MTU7.TADCR) register to 0.

(4) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 1

The title is changed to (5) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping.

<Before correction (p.630)>

A/D converter start requests (TRG4AN and TRG4BN (TRG7AN and TRG7BN)) can be issued in coordination with interrupt skipping 1 by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR).

Figure 16.86 shows an example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and down-counting and A/D converter start requests are linked with interrupt skipping 1.

Figure 16.87 shows another example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and A/D converter start requests are linked with interrupt skipping 1.

<After correction>

In complementary PWM mode, A/D converter start requests (TRG4AN and TRG4BN (TRG7AN and TRG7BN)) can be issued in coordination with interrupt skipping 1 by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR).

Figure 16.86 shows an example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and down-counting and A/D converter start requests are linked with interrupt skipping 1.

Figure 16.87 shows another example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and A/D converter start requests are linked with interrupt skipping 1.

In modes other than complementary PWM mode, do not use the A/D converter start request delaying function linked with the interrupt skipping function.

Set the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the MTU4.TADCR (MTU7.TADCR) register to 0.

<Addition>

16.6.26 Usage Notes on A/D Converter Delaying Function in Complementary PWM Mode

- When data is transferred from a buffer register at the trough of the MTU4.TCNT (MTU7.TCNT) counter while the MTU4.TADCOBRA and MTU4.TADCOBRB (MTU7.TADCOBRA and MTU7.TADCOBRB) registers are set to 0 and the UT4AE and UT4BE (UT7AE and UT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1, no A/D converter start request is issued during up-counting immediately after transfer. See Figure 16.143.
- When data is transferred from a buffer register at the crest of the MTU4.TCNT (MTU7.TCNT) counter while the MTU4.TADCOBRA and MTU4.TADCOBRB (MTU7.TADCOBRA and MTU7.TADCOBRB) registers are set to the same value as the TRCR and the UT4AE and UT4BE (UT7AE and UT7BE) bits in the MTU4.TADCR (MTU7.TADCR) register are set to 1, no A/D converter start request is issued during down-counting immediately after transfer. See Figure 16.144.

- To issue an A/D converter start request linked with the interrupt skipping function, set the MTU4.TADCORA and MTU4.TADCORB (MTU7.TADCORA and MTU7.TADCORB) registers so that 2 ≤ MTUn.TADCORA/TADCORB ≤ TCDR - 2 is satisfied (n = 4, 7).

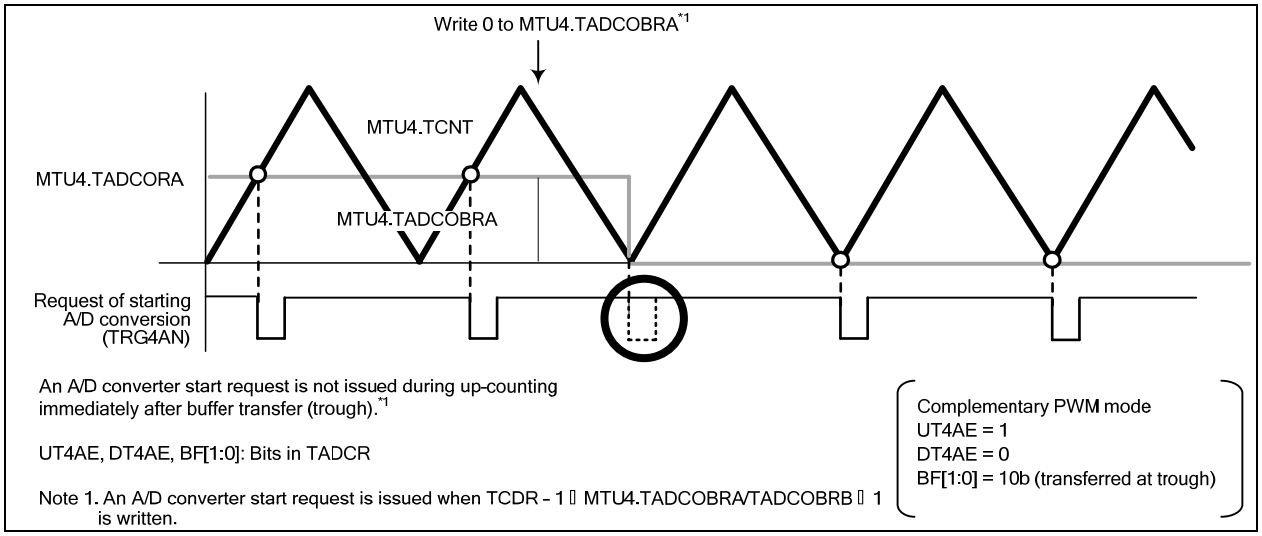

Figure 16.143 A/D Converter Start Request When 0 is Written to MTU4.TADCOBRA

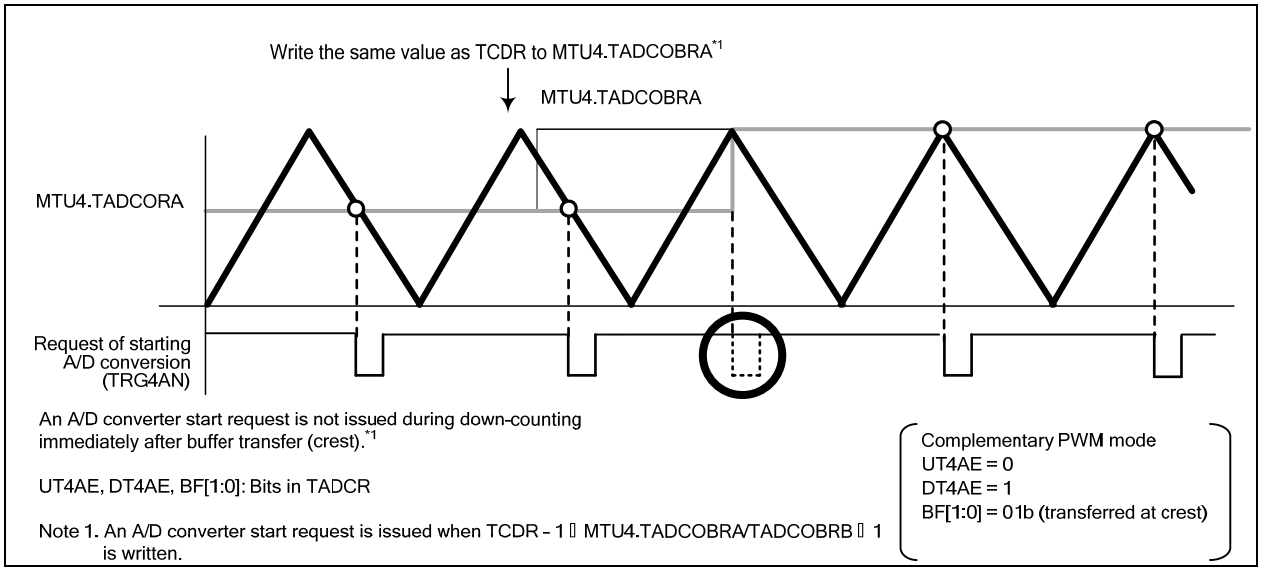

Figure 18.126 A/D Converter Start Request When the Same Value as TCDR is Written to MTU4.TADCOBRA

[Applicable Products and Reference Documents]

Series	Group	Reference Document	Rev.	Ref. No.	Section No. of MTU3
RX600	RX63T/63G	RX63T Group User's Manual: Hardware	2.10	R01UH0238EJ0210	22
	RX62T/62G	RX62T/RX62G Group User's Manual: Hardware	2.00	R01UH0034EJ0200	16
	RX64M	RX64M Group User's Manual: Hardware	1.00	R01UH0377EJ100	24