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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-H8*-A438A/E	Rev.	1.00
Title	Usage Notes on Activation of DTC and DMAC by RSPI's Interrupt		Information Category	Technical Notification		
Applicable Product	H8SX 1720 Group, H8SX 1720S Group	Lot No. All lots	Reference Document	Refer to the "Reference Documents" section below		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of usage notes in the description about the activation of DTC or DMAC by RSPI's interrupt in the H8SX 1720/1720S Group Hardware Manual.

Please read these notes carefully before using the H8SX Group products.

[Notice]

(1)Section 8 Data Transfer Controller (DTC)

RSPI is deleted from **Table 8.1 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs**.

Origin of Activation Source	Activation Source	Vector Number	DTC Vector Address Offset	DTCE*1	Priority
TPU_6	TGI6A	164	H'690	DTCEE11	High
	TGI6B	165	H'694	DTCEE10	▲
	TCI10V*2	186	H'6E8	DTCEF11	
TPU_11	TGI11A	188	H'6F0	DTCEF10	
	TGI11B	189	H'6F4	DTCEF9	
RSPI_0	SPRI_0	197	H'714	DTCEF5	
	SPTI_0	198	H'718	DTCEF4	
RSPI_1	SPRI_1	200	H'720	DTCEF3	
	SPTI_1	201	H'724	DTCEF2	
RSPI_2	SPRI_2	203	H'72C	DTCEF1	
	SPTI_2	204	H'730	DTCEF0	
RSPI_3	SPRI_3	206	H'738	DTCEG15	
	SPTI_3	207	H'73C	DTCEG14	Low ▼

Delete

Notes: 1. The DTCE bits with no corresponding interrupt are reserved, and the write value should always be 0. To leave software standby mode or all-module-clock-stop mode with an interrupt, write 0 to the corresponding DTCE bit.
2. TCI10V does not activate the DTC.

(2) Section 5 Interrupt Controller

RSPI's DTC Activations are changed from '○'(valid) to '—'(invalid) in **Table 5.2 Interrupt Sources, Vector Address Offsets, and Interrupt Priority.**

Change From

Classification	Interrupt Source	Vector Number	Vector Table Address Offset* Advanced Mode	IPR	Priority	DTC Activation	DMAC Activation
—	Reserved for system use	192	H'0300	—	High	—	—
		193	H'0304			—	—
RSPI_0	SPEI_0	196	H'0310	IPRP14 to IPRP12		—	—
	SPRI_0	197	H'0314			○	○
	SPTI_0	198	H'0318			○	○
RSPI_1	SPEI_1	199	H'031C	IPRP10 to IPRP8		—	—
	SPRI_1	200	H'0320			○	○
	SPTI_1	201	H'0324			○	○
RSPI_2	SPEI_2	202	H'0328	IPRP6 to IPRP4		—	—
	SPRI_2	203	H'032C			○	○
	SPTI_2	204	H'0330			○	○
RSPI_3	SPEI_3	205	H'0334	IPRP2 to IPRP0		—	—
	SPRI_3	206	H'0338			○	○
	SPTI_3	207	H'033C			○	○

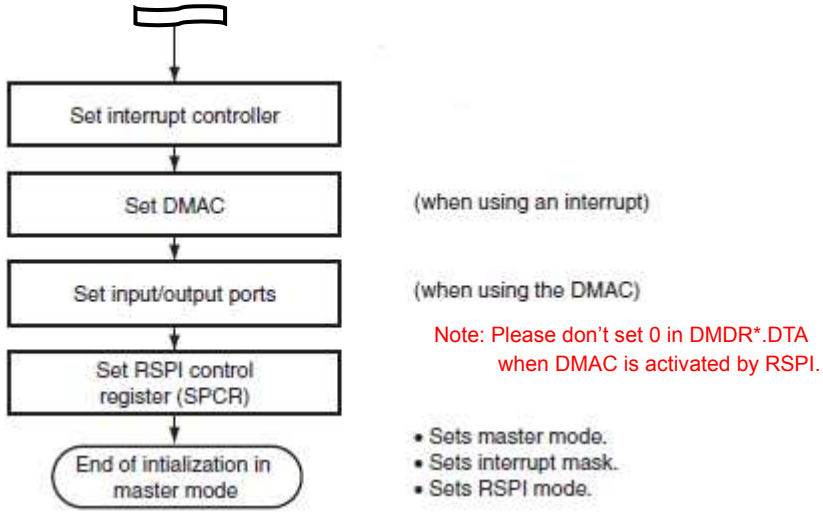
Change To

Classification	Interrupt Source	Vector Number	Vector Table Address Offset* Advanced Mode	IPR	Priority	DTC Activation	DMAC Activation
—	Reserved for system use	192	H'0300	—	High	—	—
		193	H'0304			—	—
RSPI_0	SPEI_0	196	H'0310	IPRP14 to IPRP12		—	—
	SPRI_0	197	H'0314			—	○
	SPTI_0	198	H'0318			—	○
RSPI_1	SPEI_1	199	H'031C	IPRP10 to IPRP8		—	—
	SPRI_1	200	H'0320			—	○
	SPTI_1	201	H'0324			—	○
RSPI_2	SPEI_2	202	H'0328	IPRP6 to IPRP4		—	—
	SPRI_2	203	H'032C			—	○
	SPTI_2	204	H'0330			—	○
RSPI_3	SPEI_3	205	H'0334	IPRP2 to IPRP0		—	—
	SPRI_3	206	H'0338			—	○
	SPTI_3	207	H'033C			—	○

(3) Section 15 Renesas Serial Peripheral Interface (RSPI)

In **Figure 15.28 Example of Initialization Flowchart in Master Mode**, Note is added.

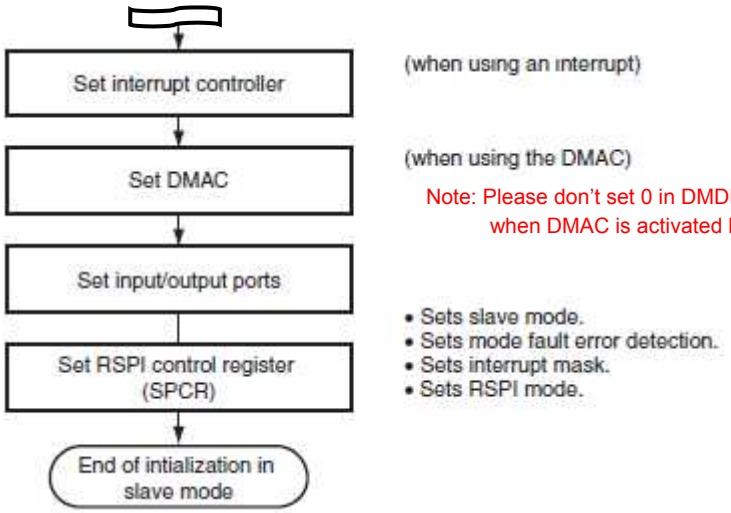
(The Figure number is H8SX/1720S's.)



(4) Section 15 Renesas Serial Peripheral Interface (RSPI)

In **Figure 15.30 Example of Initialization Flowchart in Slave Mode**, Note is added.

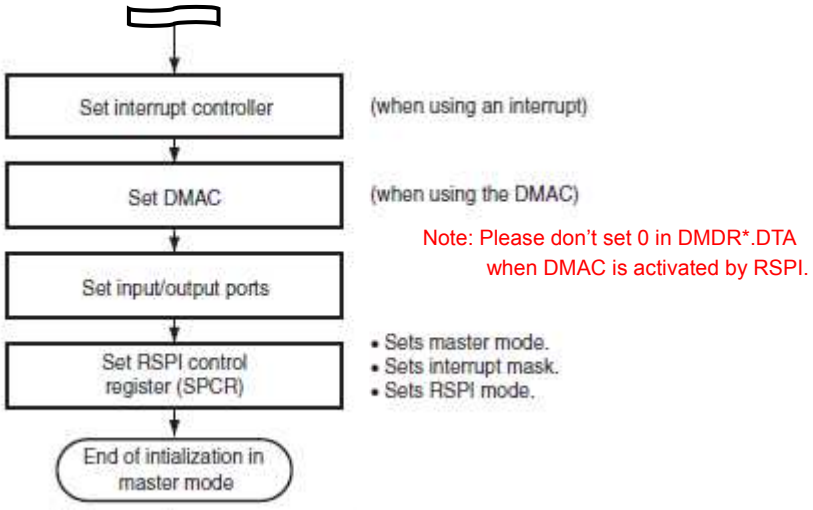
(The Figure number is H8SX/1720S's.)



(5) Section 15 Renesas Serial Peripheral Interface (RSPI)

In **Figure 15.34 Example of Initialization Flowchart in Master Mode**, Note is added.

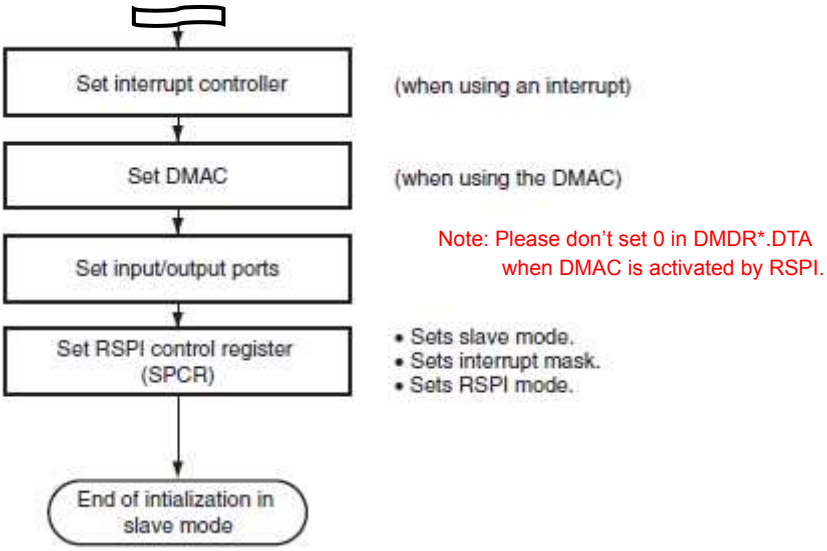
(The Figure number is H8SX/1720S's.)



(6) Section 15 Renesas Serial Peripheral Interface (RSPI)

In **Figure 15.36 Example of Initialization Flowchart in Slave Mode**, Note is added.

(The Figure number is H8SX/1720S's.)



(7) Section 15 Renesas Serial Peripheral Interface (RSPI)

Section 15.5 Usage Notes is added as below.

15.5 Usage Notes

15.5.1 Interrupt Generation after DMAC activation by RSPI

DMDR*.DTA bit enables or disables the clearing of the interrupt source which is selected by DMRSR.

In the case DMAC is activated by RSPI, the RSPI's interrupt source can be cleared by DMA transfer (SPTEF clear by writing the SPDR or SPRF clear by reading the SPDR etc.), and when the interrupt source is cleared after it activated DMAC, unintentional interrupt exception handling may be executed.

Therefore please don't use the RSPI's interrupt exception handler when DMA is activated by RSPI.

DMAC has DMA transfer end interrupt vector (DMTEND*) apart from interrupt source which activates DMAC. So, the above-mentioned unintentional interruption would not be occurred when DMTEND* is used even though RSPI interrupt source is cleared by DMA transfer.

Based on the above, as for DMA activation by RSPI, usage of DMDR*.DTA will be restricted like below.

> Please don't set 0 in DMDR*.DTA when DMAC is activated by RSPI.
> DMADR*.DTA = 0 : RSPI interrupt request to CPU is generated
> (Setting prohibited at DMAC activation by RSPI)
> =1 : RSPI interrupt request to CPU is not generated

Reference Documents:

H8SX/1720 Group Hardware Manual （R01UH0369EJ0300）Rev.3.00

H8SX/1720S Group Hardware Manual （R01UH0370EJ0200）Rev.2.00