# **RENESAS TECHNICAL UPDATE**

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Product Category	MPU/MCU		Document No.	TN-RX*-A116A/E	1.00		
Title	Temperature Sensor / Flash Memory Errata to using Temperature Sensor Calibrati Registers and Unique ID Registers n.	Information Category	Technical Notification				
		Lot No.					
Applicable Product	RX630 group RX63N, RX631 group	Reference Document	RX630 group RX63N, RX631 group User's Manual, Hardware section				

This document describes corrections to using Temperature Sensor Calibration Data Registers in Temperature Sensor section and Unique ID Registers n in Flash Memory section.

Page and section numbers are based on the RX630 Group. Refer to the table on the last page for the corresponding pages and chapters in other groups.

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Table 5.1 is corrected as follows:

# Before correction

## Table 5.1 List of I/O Registers (Address Order)

Module			Register	Number	Access	Number of Ac	cess States	Related	Reference
Address Symbol	Register Name	Symbol	of Bits	Size	ICLK ≧ PCLK	ICLK < PCLK	Function	Page	
FEFF FAC0h	FLASH	Unique ID register 0 *9	UIDR0	8	8	1ICLK	1ICLK	Flash	1515
FEFF FAC1h	FLASH	Unique ID register 1 *9	UIDR1	8	8	1ICLK	1ICLK	Memory	1515
FEFF FAC2h	FLASH	Unique ID register 2 *9	UIDR2	8	8	1ICLK	1ICLK		1515
FEFF FAC3h	FLASH	Unique ID register 3 *9	UIDR3	8	8	1ICLK	1ICLK		1515
FEFF FAC4h	FLASH	Unique ID register 4 *9	UIDR4	8	8	1ICLK	1ICLK	-	1515
FEFF FAC5h	FLASH	Unique ID register 5 *9	UIDR5	8	8	1ICLK	1ICLK	-	1515
FEFF FAC6h	FLASH	Unique ID register 6 *9	UIDR6	8	8	1ICLK	1ICLK		1515
FEFF FAC7h	FLASH	Unique ID register 7 *9	UIDR7	8	8	1ICLK	1ICLK	-	1515
FEFF FAC8h	FLASH	Unique ID register 8 *9	UIDR8	8	8	1ICLK	1ICLK		1515
FEFF FAC9h	FLASH	Unique ID register 9 *9	UIDR9	8	8	1ICLK	1ICLK		1515
FEFF FACAh	FLASH	Unique ID register 10 <sup>*9</sup>	UIDR10	8	8	1ICLK	1ICLK	-	1515
FEFF FACBh	FLASH	Unique ID register 11 <sup>*9</sup>	UIDR11	8	8	1ICLK	1ICLK		1515
FEFF FACCh	FLASH	Unique ID register 12 *9	UIDR12	8	8	1ICLK	1ICLK	-	1515
FEFF FACDh	FLASH	Unique ID register 13 <sup>*9</sup>	UIDR13	8	8	1ICLK	1ICLK		1515
FEFF FACEh	FLASH	Unique ID register 14 <sup>*9</sup>	UIDR14	8	8	1ICLK	1ICLK		1515
FEFF FACFh	FLASH	Unique ID register 15 <sup>*9</sup>	UIDR15	8	8	1ICLK	1ICLK	-	1515
FEFF FAD2h	TEMPS	Temperature sensor calibration data register *9	TSCDRL	8	8	1ICLK	1ICLK	Temperature Sensor	1480
FEFF FAD3h	TEMPS	Temperature sensor calibration data register *9	TSCDRH	8	8	1ICLK	1ICLK	]	1480



## **Corrections**

#### Table 5.1 List of I/O Registers (Address Order)

	Module		Register	Number	Access	Number of Ac	mber of Access States		Reference
Address	Symbol	Register Name	Symbol	of Bits	Size	ICLK ≧ PCLK	ICLK < PCLK	Function	Page
FEFF FAC0h	FLASH	Unique ID register 0 *9	UIDR0	32	32	1ICLK	1ICLK	Flash	1515
FEFF FAC4h	FLASH	Unique ID register 1 *9	UIDR1	32	32	1ICLK	1ICLK	Memory	1515
FEFF FAC8h	FLASH	Unique ID register 2 *9	UIDR2	32	32	1ICLK	1ICLK		1515
FEFF FACCh	FLASH	Unique ID register 3 *9	UIDR3	32	32	1ICLK	1ICLK		1515
FEFF FAD0h	TEMPS	Temperature sensor calibration data register *9	TSCDR	32	32	1ICLK	1ICLK	Temperature Sensor	1480

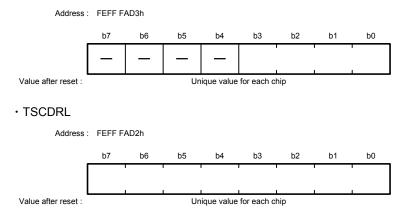
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The description of Temperature Sensor Calibration Data Registers in 41.2.2 is corrected as follows:

#### Before correction

41.2.2 Temperature Sensor Calibration Data Registers (TSCDRH, TSCDRL)

#### • TSCDRH



The TSCDRH and TSCDRL registers hold the temperature sensor calibration data measured for each chip at the time of shipment.

The temperature sensor calibration data is a digital value converted by the 12-bit A/D converter from the voltage output by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V. The TSCDRH and TSCDRL registers respectively hold the higher-order four bits and the lower-order eight bits of the result of conversion. If the endian setting for the CPU is little endian, read FEFF FAD2h as a 16-bit unit to obtain 12 bits of data at a time.

These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM.

These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case.



# **Corrections**

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41.2.2 Temperature Sensor Calibration Data Register (TSCDR)

0 0 0 0   TSCD[11:0]   Value after reset :	Address																
value after rest:						b27	b26	b25	b24	b23	1	1	b20	b19 1	b18	b17	b16
115  014  013  012  011  010  00  02  02  02		0	0	0	0		1	1	1	1		D[11:0]	1	1	1	1	
Value after read:   Unque value for each chip     Bit   Symbol   Bit Name   Description   RW     D15 to b0   —   Reserved   Unique value for each chip   R     D27 to b16   TSCD[11:0]   Temperature Sensor   The 12-bit A/D conversion results of the temperature R	Value after reset :									Ur	nique value	e for each c	hip				
Value after root:   Unque value for each chip     Bit   Symbol   Bit Name   Description   RW     b15 to b0   —   Reserved   Unique value for each chip   R     b27 to b16   TSCD[11:0]   Temperature Sensor   The 12-bit A/D conversion results of the temperature R     calibration Data   _sensor output measured at the time of shipment.   R     b31 to b28   —   Reserved   These bits are read as 0.   R     The TSCDR register hold the temperature sensor calibration data measured for each chip at the time of shipment.   R     The temperature sensor calibration data is a digital value converted by the 12-bit A/D converter from the voltage outp by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V.     These registers are neserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case.     Page 1515 of 1681     The description of Unique ID Registers n in 43.2.22 is corrected as follows:     Orrectorion     3.2.22 Unique ID Registers n (UIDRn) (n = 0 to 15)     UDBM FEFF FACE,																	
Bit     Symbol     Bit Name     Description     RW       b15 to b0     —     Reserved     Unique value for each chip     R       b27 to b16     TSCD[11:0]     Temperature Sensor     The 12-bit A/D conversion results of the temperature R       b21 to b28     —     Reserved     The 12-bit A/D conversion results of the temperature R       b21 to b28     —     Reserved     The SCDR register hold the temperature sensor calibration data measured for each chip at the time of shipment.       The TSCDR register hold the temperature sensor calibration data is a digital value converted by the 12-bit A/D converter from the voltage output by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V.       These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM.       These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case.       Page 1515 of 1681       The description of Unique ID Registers n in 43.2.22 is corrected as follows:       fore correction       32.22 Unique ID Registers n (UDRn) (n = 0 to 15)       volted FEFF FACH, UDRT F		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bit     Symbol     Bit Name     Description     RW       b15 to b0     —     Reserved     Unique value for each chip     R       b27 to b16     TSCD[11:0]     Temperature Sensor     The 12-bit A/D conversion results of the temperature R       b21 to b28     —     Reserved     The 12-bit A/D conversion results of the temperature R       b21 to b28     —     Reserved     The SCDR register hold the temperature sensor calibration data measured for each chip at the time of shipment.       The TSCDR register hold the temperature sensor calibration data is a digital value converted by the 12-bit A/D converter from the voltage output by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V.       These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM.       These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case.       Page 1515 of 1681       The description of Unique ID Registers n in 43.2.22 is corrected as follows:       fore correction       32.22 Unique ID Registers n (UDRn) (n = 0 to 15)       volted FEFF FACH, UDRT F		-	—	—		_	-	_	—	—	_	-	_		—	-	-
b15 to b0   -   Reserved   Unique value for each chip   R     b27 to b16   TSCD[11:0]   Temperature Sensor   The 12-bit A/D conversion results of the temperature   R     b31 to b28   -   Reserved   These bits are read as 0.   R     b31 to b28   -   Reserved   These bits are read as 0.   R     The TSCDR register hold the temperature sensor calibration data is a digital value converted by the 12-bit A/D converter from the voltage outp by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V.   These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM.     These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case.   Page 1515 of 1681     Page 1515 of 1681   The description of Unique ID Registers n in 43.2.22 is corrected as follows:     Ore correction   3.2.22 Unique ID Registers n (UIDRn) (n = 0 to 15)     UDR0 FEFF FACID, UDR1 FEFF FACID, UDR3 FEFF FACID, UDR3 FEFF FACID, UDR1	Value after reset :							Ur	nique value	for each c	hip						
b15 to b0   -   Reserved   Unique value for each chip   R     b27 to b16   TSCD[11:0]   Temperature Sensor   The 12-bit A/D conversion results of the temperature   R     b31 to b28   -   Reserved   These bits are read as 0.   R     b31 to b28   -   Reserved   These bits are read as 0.   R     The TSCDR register hold the temperature sensor calibration data measured for each chip at the time of shipment.   R     The temperature sensor alibration data is a digital value converted by the 12-bit A/D converter from the voltage outp by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V.   These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM.     These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case.   Page 1515 of 1681     The description of Unique ID Registers n in 43.2.22 is corrected as follows:   Integes registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case.     Matressep:   Integes registers are integes registers are integes registers are integes registers are only present in the for each chip.     Matressep:   Integes registers are integes registers are only present in the for each chip.     Matressep:   Integes registers are only present in the G-version products. These registers cannot be modified by the user sinc																	
b15 to b0	Rit	Symb	ol	Bit	Name			Desc	rintion								R/M
Calibration Data sensor output measured at the time of shipment. bit to b28 — Reserved These bits are read as 0. R The TSCDR register hold the temperature sensor calibration data measured for each chip at the time of shipment. The temperature sensor calibration data is a digital value converted by the 12-bit A/D converter from the voltage output by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case. Page 1515 of 1681 The description of Unique ID Registers n in 43.2.22 is corrected as follows: and correction 3.2.22 Unique ID Registers n (UIDRn) (n = 0 to 15) uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN TEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, UIDBN FEFF FACH, uiDBN FEFF FACH, UIDBN FEFF FA		_	01							e for ea	ach chi	р					
b31 to b28   —   Reserved   These bits are read as 0.   R     The TSCDR register hold the temperature sensor calibration data is a digital value converted by the 12-bit A/D converter from the voltage outp   by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V.     These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM.   These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case.     Page 1515 of 1681   The description of Unique ID Registers n in 43.2.22 is corrected as follows:     fore correction   IDBN FEFF FACH, UDBR FEFF	b27 to b16	TSCE	[11:0]				isor								•	ature	R
The TSCDR register hold the temperature sensor calibration data measured for each chip at the time of shipment. The temperature sensor calibration data is a digital value converted by the 12-bit A/D converter from the voltage outp by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case. Page 1515 of 1681 The description of Unique ID Registers n in 43.2.22 is corrected as follows: fore correction I3.2.22 Unique ID Registers n (UIDRn) (n = 0 to 15) UDBR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UDBR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UDBR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UDBR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UDBR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN UIDR FEFF FACEN, UIDR FEFF FACEN UIDR FEFF FACEN UIDR FEFF FACEN UIDR FEFF FACEN UIDR FEFF FACEN UIDR FEFF FACEN UIDR FEFF FAC	b31 to b28					n Data						at the ti	me of s	snipme	nt.		R
The temperature sensor calibration data is a digital value converted by the 12-bit A/D converter from the voltage output by the temperature sensor at Ta = Tj = 128°C and AVCC0 = VREFH0 = 3.3V. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case. Page 1515 of 1681 The description of Unique ID Registers n in 43.2.22 is corrected as follows: <u>ore correction</u> 3.2.22 Unique ID Registers n (UIDRn) (n = 0 to 15) UIDRO FEFF FACCH, UIDR1 FEFF FACCH, UIDR2 FEFF FACCH, UIDR3 FEFF FACCH UIDR2 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH UIDR2 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH UIDR2 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH UIDR3 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH UIDR3 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH UIDR3 FEFF FACCH, UIDR3 FEFF FACCH, UIDR3 FEFF FACCH The UIDRA registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in th G-version products. These registers cannot be modified by the user since they are in the FCU firmwa																	
ore correction     3.2.22 Unique ID Registers n (UIDRn) (n = 0 to 15)     UDR0 FEFF FACOh, UIDR1 FEFF FAC1h, UIDR2 FEFF FAC2h, UIDR3 FEFF FAC3h     Address(es):     UIDR0 FEFF FAC0h, UIDR1 FEFF FAC3h, UIDR3 FEFF FAC3h, UIDR3 FEFF FAC3h, UIDR4 FEFF FAC3h, UIDR6 FEFF FAC3h, UIDR10 FEFF FAC3h, UIDR11 FEFF FAC3h, UIDR12 FEFF FAC3h, UIDR13 FEFF FAC3h, UIDR10 FEFF FAC3h, UIDR13 FEFF FAC3h, UIDR13 FEFF FAC3h, UIDR13 FEFF FAC3h, UIDR14 FEFF FAC3h, UIDR15 FEFF FAC3h, UIDR12 FEFF FAC3h, UIDR13 FEFF FAC3h, UIDR14 FEFF FAC4h, UIDR15 FEFF FAC5h     Value after reset:     Value after reset:     Unique value for each chip     The UIDRn registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in to G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of to pn-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited					n-enip	ROM C	lisabled	d exten	ded mo	ode, so	acces	s to the	em is pi	ohibite	d in thi	s case	
H3.2.22 Unique ID Registers n (UIDRn) (n = 0 to 15)     Address(es):   UIDR0 FEFF FAC0h, UIDR1 FEFF FAC3h, UIDR3 FEFF FAC3h, UIDR1 FEFF	-											s to the	em is pi	ohibite	d in thi	s case	·.
Address(es): UIDR0 FEFF FAC0h, UIDR1 FEFF FAC1h, UIDR2 FEFF FAC2h, UIDR3 FEFF FAC3h UIDR4 FEFF FAC3h, UIDR5 FEFF FAC3h, UIDR5 FEFF FAC3h, UIDR10 FEFF FAC3h, UIDR11 FEFF FAC3h UIDR12 FEFF FAC2h, UIDR13 FEFF FAC3h, UIDR14 FEFF FAC2h, UIDR15 FEFF FAC3h UIDR12 FEFF FAC2h, UIDR13 FEFF FAC3h, UIDR14 FEFF FAC2h, UIDR15 FEFF FAC3h Value after reset : Unique value for each chip The UIDRn registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in th G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of th on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	-											s to the	em is pr	ohibite	d in thi	s case	
Address(es) : UIDR4 FEFF FAC4h, UIDR5 FEFF FAC5h, UIDR6 FEFF FAC6h, UIDR7 FEFF FAC3h UIDR8 FEFF FAC3h, UIDR9 FEFF FAC3h, UIDR10 FEFF FAC3h, UIDR11 FEFF FAC3h UIDR12 FEFF FAC3h, UIDR13 FEFF FAC3h, UIDR14 FEFF FAC3h, UIDR15 FEFF FAC3h UIDR12 FEFF FAC3h, UIDR13 FEFF FAC3h, UIDR14 FEFF FAC3h, UIDR15 FEFF FAC3h Value after reset : Unique value for each chip The UIDRn registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in th G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	The descript	ion of L										s to the	ım is pi	rohibite	d in thi	s case	<u>.</u>
Address(es) · UIDR8 FEFF FAC8h, UIDR9 FEFF FAC9h, UIDR10 FEFF FAC9h, UIDR11 FEFF FAC8h UIDR12 FEFF FAC6h, UIDR13 FEFF FAC9h, UIDR14 FEFF FACEh, UIDR15 FEFF FACFh b7 b6 b5 b4 b3 b2 b1 b0 value after reset : Unique value for each chip The UIDRn registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in th G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	The descript	ion of L <u>on</u>	Jnique	ID Reg	isters r	ו in 43.	2.22 is					s to the	ım is pi	ohibite	d in thi	s case	·.
Value after reset : Unique value for each chip The UIDRn registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in th G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	The descript	ion of L o <u>n</u> ue ID R <sup>UIDR0</sup>	Jnique egister	ID Reg s n (UI	isters r DRn) (I	n in 43. n = 0 ta FAC1h, U	2.22 is 0 15) 1dr2 FEF	<b>COFFEC</b>	ted as T	<b>follows</b> EFF FAC	: 3h	s to the	em is pi	rohibite	d in thi	s case	ι.
Value after reset : Unique value for each chip The UIDRn registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in th G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	The descript fore correctic	ion of L on ue ID R UIDR0 ): UIDR4	Jnique egister FEFF FAG FEFF FAG FEFF FAG	ID Reg s n (UI <sup>Coh,</sup> UIDI <sup>Coh,</sup> UIDI Sah, UIDI	isters r DRn) (ו או הברה ה ק הברה ה ק הברה ה	n in 43. n = 0 ta FAC5h, U FAC5h, U	2.22 is 0 15) IDR2 FEF IDR6 FEF IDR10 FE	F FAC2h, F FAC2h, F FAC6h, F FAC6h,	UIDR3 F UIDR3 F UIDR7 F 1, UIDR11	follows EFF FAC EFF FAC FEFF FA	: - 7h ACBh	s to the	ım is pi	rohibite	d in thi	s case	
The UIDRn registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in th G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of th on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	The descript	ion of L on ue ID R UIDR0 ): UIDR4	Jnique egister FEFF FAG FEFF FAG FEFF FAG	ID Reg s n (UI <sup>Coh,</sup> UIDI <sup>Coh,</sup> UIDI Sah, UIDI	isters r DRn) (ו או הברה ה ק הברה ה ק הברה ה	n in 43. n = 0 ta FAC5h, U FAC5h, U	2.22 is 0 15) IDR2 FEF IDR6 FEF IDR10 FE	F FAC2h, F FAC2h, F FAC6h, F FAC6h,	UIDR3 F UIDR3 F UIDR7 F 1, UIDR11	follows EFF FAC EFF FAC FEFF FA	: - 7h ACBh	s to the	em is pi	rohibite	d in thi	s case	
The UIDRn registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in the G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	The descript fore correctic	uion of L ue ID R uudro UUDR0 UUDR12	Jnique egister FEFF FAG FEFF FAG 2 FEFF FA	ID Reg s n (UI coh, UID coh, UID coh, UID acch, UIT	DRn) (I R1 FEFF I R5 FEFF I R5 FEFF I R5 FEFF I DR13 FEF	n <b>= 0 t</b> ơ FAC1h, U FAC5h, U FAC9h, U FF FACDh	2.22 is 0 15) IDR2 FEF IDR6 FEF IDR6 FEF JDR10 FE , UIDR14	F FAC2h, F FAC2h, FF FAC6h, FF FAC6h, FE FAC6h,	UIDR3 F UIDR3 F UIDR7 F 1, UIDR11 CEh, UIDF	Follows EFF FAC EFF FAC FEFF FA R15 FEFF	: - 7h ACBh	s to the	em is pi	rohibite	d in thi	s case	а.
G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	The descript fore correctic	uion of L ue ID R uudro UUDR0 UUDR12	Jnique egister FEFF FAG FEFF FAG 2 FEFF FA	ID Reg s n (UI coh, UID coh, UID coh, UID acch, UIT	DRn) (I R1 FEFF I R5 FEFF I R5 FEFF I R5 FEFF I DR13 FEF	n <b>= 0 t</b> ơ FAC1h, U FAC5h, U FAC9h, U FF FACDh	2.22 is 0 15) IDR2 FEF IDR6 FEF IDR6 FEF JDR10 FE , UIDR14	F FAC2h, F FAC2h, FF FAC6h, FF FAC6h, FE FAC6h,	UIDR3 F UIDR3 F UIDR7 F 1, UIDR11 CEh, UIDF	Follows EFF FAC EFF FAC FEFF FA R15 FEFF	: - 7h ACBh	s to the	em is pi	rohibite	d in thi	s case	A.
G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	The descript	ion of L on ue ID R UIDR0 UIDR12 UIDR12	Jnique egister FEFF FAG FEFF FAG 2 FEFF FA	ID Reg s n (UI coh, UIDf cah, UIDf cah, UIDf cah, UIDf cach, UIDf cach cach cach cach cach cach cach cach	DRn) (1 R1 FEFF 1 R9 FEFF 1 R9 FEFF 1 DR13 FEF b4	n in 43. n = 0 to FAC5h, U FAC9h, U FAC9h, U FAC9h, U FAC9h b3	2.22 is 0 15) IDR2 FEF IDR10 FEF IDR10 FE UIDR14 b2	F FAC2h, F FAC2h, FF FAC6h, FF FAC6h, FE FAC6h,	UIDR3 F UIDR3 F UIDR7 F 1, UIDR11 CEh, UIDF	Follows EFF FAC EFF FAC FEFF FA R15 FEFF	: - 7h ACBh	s to the	em is pi	rohibite	d in thi	s case	A.
on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited	The descript	ion of L 2n ue ID R UIDR0 UIDR4 UIDR12 b7	Jnique egister FEFF FAG FEFF FAG 2 FEFF FA b6	ID Reg s n (UI coh, UIDI cah, UIDI cah, UIDI cach, UIDI acch, UID	DRn) (I R1 FEFF I R3 FEFF I DR13 FEF b4	n = 0 tơ FAC1h, U FAC3h, U FAC3h, U FAC3h, U FAC3h, U FAC3h Ulue for ead	2.22 is 0 15) IDR2 FEF IDR6 FEF IDR10 FE UIDR14 b2 ch chip	F FAC2h, F FAC6h, F FAC6h, FF FACAI FEFF FA	UIDR3 F UIDR3 F UIDR7 F 1, UIDR11 CEh, UIDF	follows EFF FAC EFF FAC FEFF FA R15 FEFF	3h 7h NCBh FACFh						
	The descript	ion of L <u>on</u> ue ID R UIDR0 UIDR0 UIDR1 UIDR1 b7 register	Jnique egister FEFF FAG FEFF FAG 2 FEFF FA 2 FEFF FA b6 1 1 5 hold	ID Reg s n (UI coh, UIDf cah, UIDf cah, UIDf cah, UIDf cach, UIDf	DRn) (I R1 FEFF I R3 FEFF I R3 FEFF I DR13 FEF D4 Unique va	n in 43. n = 0 to FAC3h, U FAC9h, U FAC9h, U FAC9h Ulue for eao des (ur	2.22 is 0.15) IDR2 FEF IDR10 FEF IDR10 FE IDR10 FE DR10 FEF IDR10 FEF	Correc F FAC2h, F FAC6h, FF FACAI FEFF FAC DS) to in	UIDR3 F UIDR3 F UIDR7 F n, UIDR11 CEh, UIDF	follows EFF FAC EFF FAC FEFF FA 15 FEFF	3h 7h NCBh FACFh	nd these	e regis	ters are	e only p	presen	t in t
this case.	The descript	ion of L <u>on</u> ue ID R UIDR0 UIDR0 UIDR1 UIDR1 b7 register	Jnique egister FEFF FAG FEFF FAG 2 FEFF FA 2 FEFF FA b6 1 1 5 hold	ID Reg s n (UI coh, UIDf cah, UIDf cah, UIDf cah, UIDf cach, UIDf	DRn) (I R1 FEFF I R3 FEFF I R3 FEFF I DR13 FEF D4 Unique va	n in 43. n = 0 to FAC3h, U FAC9h, U FAC9h, U FAC9h Ulue for eao des (ur	2.22 is 0.15) IDR2 FEF IDR10 FEF IDR10 FE IDR10 FE DR10 FEF IDR10 FEF	Correc F FAC2h, F FAC6h, FF FACAI FEFF FAC DS) to in	UIDR3 F UIDR3 F UIDR7 F n, UIDR11 CEh, UIDF	follows EFF FAC EFF FAC FEFF FA 15 FEFF	3h 7h NCBh FACFh	nd these	e regis	ters are	e only p	presen	t in tr
	The descript	ion of L 20 Je ID R UIDRO UIDRO UIDRO UIDRO UIDRO UIDRO UIDRO CONTROL DO DO DO DO DO DO DO DO DO DO	Jnique egister FEFF FAG FEFF FA ≥ FEFF FA ≥ FEFF FA b6 - b6 - s hold . These	ID Reg s n (UI coh, UID 24h, UID 24h, UID ACCh, UID ACCh, UID 16-byte e regis	DRn) (I R1 FEFF F R9 FEFF F R9 FEFF F DR13 FEF b4 Unique va e ID coo ters ca	n in 43. n = 0 to FAC5h, U FAC5h, U FAC5h, U FAC5h, U i FAC5h u tag i u u tag i u u tag i u u u u u u u u u u u u u u u u u u	2.22 is 0.15) IDR2 FEF IDR6 FEF IDR10 FE , UIDR14 b2 ch chip hique I[ pe mod	correc F FAC2h, F FAC6h, FF FACA FEFF FA DS) to in ified by	UIDR3 F UIDR7 F JUDR7 F JUDR11 CEh, UIDF	follows EFF FAC FEFF FAC FEFF FAC Ser FFF	: Th ICBh FACFh ICU ar ICU ar ICU ar	nd these ay are i	e regis	ters are FCU fil	e only p	presen e area	t in th of th
	The descript	ion of L 20 Je ID R UIDRO UIDRO UIDRO UIDRO UIDRO UIDRO UIDRO CONTROL DO DO DO DO DO DO DO DO DO DO	Jnique egister FEFF FAG FEFF FA ≥ FEFF FA ≥ FEFF FA b6 - - - - - - - - - - - - - - - - - -	ID Reg s n (UI coh, UID 24h, UID 24h, UID ACCh, UID ACCh, UID 16-byte e regis	DRn) (I R1 FEFF F R9 FEFF F R9 FEFF F DR13 FEF b4 Unique va e ID coo ters ca	n in 43. n = 0 to FAC5h, U FAC5h, U FAC5h, U FAC5h, U i FAC5h u tag i u u tag i u u tag i u u u u u u u u u u u u u u u u u u	2.22 is 0.15) IDR2 FEF IDR6 FEF IDR10 FE , UIDR14 b2 ch chip hique I[ pe mod	correc F FAC2h, F FAC6h, FF FACA FEFF FA DS) to in ified by	UIDR3 F UIDR7 F JUDR7 F JUDR11 CEh, UIDF	follows EFF FAC FEFF FAC FEFF FAC Ser FFF	: Th ICBh FACFh ICU ar ICU ar ICU ar	nd these ay are i	e regis	ters are FCU fil	e only p	presen e area	t in th of th



# **Corrections**

#### 43.2.22 Unique ID Registers n (UIDRn) (n = 0 to 3)

Address(es): UIDR0 FEFF FAC0h, UIDR1 FEFF FAC4h, UIDR2 FEFF FAC8h, UIDR3 FEFF FACCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
			1					T		1			1	I	1	1
										1						1
Value after reset							U	nique value	for each c	hip						
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
								1		1			1	1	1	'
									L	ı		L		I		1
Value after reset :							Ur	nique value	for each c	hip						

The UIDRn registers hold 16-byte ID codes (unique IDs) to identify each MCU and these registers are only present in the G-version products. These registers cannot be modified by the user since they are in the FCU firmware area of the on-chip ROM. These registers are reserved in on-chip ROM disabled extended mode, so access to them is prohibited in this case.



# RENESAS TECHNICAL UPDATE TN-RX\*-A116A/E

< Reference	Documents >					
Applicable			Desument	Section Num	ber (Page Numbe	er)
Applicable Product	Manual Title	Rev.	Document Number	I/O	Temperature	Flash
Produci			Number	Registers	Sensor	Memory
RX630 Group	RX630 Group	1.60	R01UH0040EJ0160	5	41	43
RA030 Gloup	User's Manual Hardware	1.00	R010H0040E30100	(178)	(1480)	(1515)
RX63N, RX631	RX63N Group,			5	45	47
Group	RX631 Group	1.80	R01UH0041EJ0180	(213)	(1782)	(1817)
Gloup	User's Manual Hardware			(213)	(1702)	(1017)

