

To our customers,

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## Old Company Name in Catalogs and Other Documents

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# RENESAS TECHNICAL NEWS

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M66291 \*TC1 Pin Usage Limitations

## Classification

Corrections and supplementary  
explanation of document

√ Notes  
Knowhow  
Others

## Concerned Products

USB ASSP M66291GP/M66291HP

### 1. Phenomenon

When the data write completion process is executed to the IN buffer due to a \*TC1 pin assertion, a Zero-length packet (Null packet) may also be sent with the transfer packet on the USB bus to the endpoint assigned to D1\_FIFO.

### 2. Occurring Conditions

This limitation does not apply to systems that do not use the \*TC1 pin.

When all of the following conditions are present, the phenomenon described above may occur.

Condition 1: The system uses D1\_FIFO under the condition INTM = "1".

Condition 2: The system designates the endpoint that is set to [IN buffer and Epi\_DBLB = "1"] to D1\_FIFO for data transmission.

Condition 3: \*TC1 pin is asserted when the SIE-side buffer is empty.

### 3. Solutions

The occurrence of this phenomenon can be worked around with any of the following methods:

(1)Use D1\_FIFO with INTM = "0".

(2)Use the IN-direction endpoint with Epi\_DBLB = "0".

(3)Instead of asserting the \*TC1 pin, execute the data write completion process to the IN buffer by writing IVAL = "1".

### 4. Terms and Definitions

INTM: DMA interrupt mode (D1\_FIFO Select Register bit 9)

Epi\_DBLB:Double buffer mode (Epi Configuration Register 0 bit 7)

IVAL: IN buffer/OUT buffer status (D1\_FIFO Control Register bit 13)