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GRADE A

RENESAS TECHNICAL NEWS

No.ASSP-08-0309

M66291 Dreq Signal Assertion Limitation

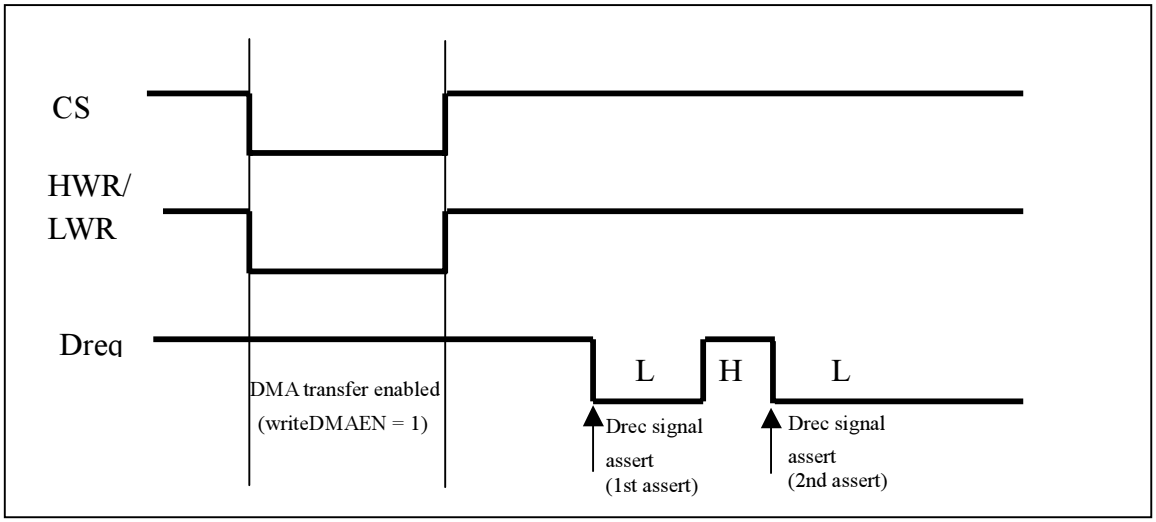
Classification	Concerned Products
Corrections and supplementary explanation of document √ Notes Knowhow Others	USB ASSP M66291GP/M66291HP

1. Phenomenon

In systems that send DMA transfers to the IN-direction endpoint using D0_FIFO or D1_FIFO (Dn_FIFO hereon) by the DMA controller, when DMA transfer is enabled (write DMAEN = "1"), the Dreq signal may be asserted twice consecutively (see Diagram 1).

[Supplement] If the system is set so that the DMA transfer is triggered by the M66291 Dreq signal, this phenomenon may cause the DMA controller to malfunction, and data will not be written successfully to the Dn_FIFO.

Figure 1. Incorrect Signal at Dreq Signal Assert



2. Occurring Conditions

This phenomenon does not apply to systems that do not perform DMA transfer to the IN endpoint or systems connected to an 8-bit data bus.

This phenomenon (Dreq signal assertion occurring twice consecutively) occurs if all of the following conditions are present when the DMA transfer enable process is written to the Dn_FIFO (write DMAEN = "1").

(1) The CPU writes to Dn_FIFO in word units (16-bit data bus).
(2) When the designated endpoint (DMA_EP) before the write is set to the IN direction and the FIFO buffer status is Ready (Dreq = "0").
(3) When the designated endpoint (DMA_EP) during the write is either IN-direction or OUT-direction.

3. Solutions

This phenomenon can be worked around with either of the following methods.

(1) Simultaneous Setup Method for DMA transfer enable and endpoint designation
To enable DMA transfer (write DMAEN = "1"), perform the following processes in the order indicated.
a. The CPU writes to the Dn_FIFO Select Register in word units when DMA transfer is disabled (write DMAEN = "0") and the endpoint is cleared (DMA_EP = "0000")
b. The CPU writes to the Dn_FIFO Select Register in word units when DMA transfer is enabled (write DMAEN = "1") and the endpoint is set (DMA_EP = corresponding EP)

(2) CPU Byte-Unit Write Method
When enabling DMA transfer (write DMAEN = "1"), perform a write in byte-units to the upper 8 bits of the Dn_FIFO Select Register.
* Do not write to the lower 8 bits of the Dn_FIFO.
* The designated endpoint (DMA_EP = corresponding EP) must be set before writing to the upper 8 bits.