To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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GRADE A

RENESAS TECHNICAL NEWS

No.ASSP-04-0309

M66291 D1_FIFO Access: Read Signal Timing Requirements

Classification	Concerned Products
Corrections and supplementary explanation of document √ Notes Knowhow Others	USB ASSP M66291GP/M66291HP

1. Phenomenon

When using D1_FIFO in a system in which the twr(CTRL) (control signal pulse width (read)) is less than 70ns, the data may not be read out properly from D1_FIFO.

2. Occurring Conditions

When all three of the following conditions are present, the D1_EP data read from the CPU bus will be incorrect.

Condition 1: DFORM ≠ "01" System - twr(CTRL (control signal pulse width(read)) is less than 70ns, or DFORM = "01 System - tw(Dack) (Dack pulse width) is less than 70ns

Condition 2: The application uses both D0_EP and D1_EP for OUT transfers.

Condition 3: [D0_EP receive complete on USB bus] and [read access from CPU bus to D1_EP] occur at the same time

3. Solutions

If the conditions described above are present in your system, please implement the following precautions:

DFORM ≠ "01" System: twr(CTRL) ≥ 70ns

DFORM = "01" System: tw(Dack) ≥ 70ns

4. Related Terminology

Dn_EP: The endpoint selected in the D0_FIFO or D1_FIFO Select Register.

OUT: OUT direction transfer

CPU Bus: External bus that accesses M66291 from the external CPU or DMAC.

DFORM: Bits 13 and 14 of Dn_FIFO Select Register.