To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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GRADE A

MESC TECHNICAL NEWS

No. M380-17-9910

Corrections and Supplementary Explanation for "3822 Group User's Manual"

This news includes all corrections and supplementary explanation for the 3822 Group User's Manual (1995.3 issued, document number: H-ED347-A) issued before.

Please refer to the corrected information as shown below.

- Corrections and supplementary explanation for the 3822 Group User's Manual issued before

  (A) M380-11-9507 Correction of "3822 Group User's Manual"
  (B) M380-14-9907 Corrections and Supplementary Explanation for "3820/3822/3825 Group User's Manuals

  Note: Alphabets in parentheses are corresponding to the alphabets in the parameter "REV." of the following corrections and supplementary explanation list. "Rev.C" is the new information added in this time.

Corrections and Supplementary Explanation for “3822 Group User’s Manuals” No.1

Rev.	Page	Contents
C	P1-20 (Left columun)	Error A key input interrupt request is generated by applying “L” level ... Correct A key input interrupt request is generated by detecting falling edge..
A	P1-22 line 7 (Right column)	Error (However, if the real time port control bit is changed from “0” to “1”, data are output without the timer X.) Correct (However, after rewriting a data storage bit for real time port, if the real time port control bit is changed from “0” to “1”, data is output without the timer X.)
A	P2-40 line 8	Error A data output from the real time port is started at setting the real time port control bit to “1”. Correct A data output from the real time port is started at setting the real time port control bit to “1” (when setting “1” to the real time port control bit of the timer X mode register, use the SEB instruction).
B	P2-65 (1) Timer X ■ Timer mode Fig. 2.3.22	Previous change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before setting ① below, clear the timer X interrupt enable bit and the timer X interrupt request bit to “0”. •After setting ④ below, set the timer X interrupt enable bit to “1” (interrupts enabled). After change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before timer X stops counting (before setting ① below), clear the timer X interrupt enable bit to “0”. •After setting ③ below, clear the timer X interrupt request bit to “0” and next set the timer X interrupt enable bit to “1” (interrupt enabled). •Set ④ last.
B	P2-66 (1) Timer X ■ Pulse output mode Fig. 2.3.23	Previous change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before setting ① below, clear the interrupt enable bits (timer X or $CNTR_0$) and the interrupt request bits (timer X or $CNTR_0$) to “0”. •After setting ⑤ below, set the interrupt enable bits (timer X or $CNTR_0$) to “1” (interrupts enabled). After change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before timer X stops counting (before setting ② below), clear the interrupt enable bit (timer X or $CNTR_0$) to “0”. •After setting ④ below, clear the interrupt request bit (timer X or $CNTR_0$) to “0” and next set the interrupt enable bit (timer X or $CNTR_0$) to “1” (interrupt enabled). •Set ⑤ last.

Corrections and Supplementary Explanation for “3822 Group User’s Manuals” No.2

Rev.	Page	Contents
B	P2-67 (1) Timer X ■ Event counter mode Fig. 2.3.24	Previous change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before setting ① below, clear the interrupt enable bits (timer X or CNTR0) and the interrupt request bits (timer X or CNTR0) to “0”. •After setting ⑤ below, set the interrupt enable bits (timer X or CNTR0) to “1” (interrupts enabled). After change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before timer X stops counting (before setting ② below), clear the interrupt enable bit (timer X or CNTR0) to “0”. •After setting ④ below, clear the interrupt request bit (timer X or CNTR0) to “0” and next set the interrupt enable bit (timer X or CNTR0) to “1” (interrupt enabled). •Set ⑤ last.
B	P2-68 (1) Timer X ■ Pulse width measurement mode Fig. 2.3.25	Previous change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before setting ① below, clear the interrupt enable bits (timer X or CNTR0) and the interrupt request bits (timer X or CNTR0) to “0”. •After setting ⑤ below, set the interrupt enable bits (timer X or CNTR0) to “1” (interrupts enabled). After change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before timer X stops counting (before setting ② below), clear the interrupt enable bit (timer X or CNTR0) to “0”. •After setting ④ below, clear the interrupt request bit (timer X or CNTR0) to “0” and next set the interrupt enable bit (timer X or CNTR0) to “1” (interrupt enabled). •Set ⑤ last.
B	P2-70 (2) Timer Y ■ Timer mode Fig. 2.3.27	Previous change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before setting ① below, clear the timer Y interrupt enable bit and the timer Y interrupt request bit to “0”. •After setting ④ below, set the timer Y interrupt enable bit to “1” (interrupts enabled). After change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before timer Y stops counting (before setting ① below), clear the timer Y interrupt enable bit to “0”. •After setting ③ below, clear the timer Y interrupt request bit to “0” and next set the timer Y interrupt enable bit to “1” (interrupt enabled). •Set ④ last.

Corrections and Supplementary Explanation for “3822 Group User’s Manuals” No.3

Rev.	Page	Contents
B	P2-71 (2) Timer Y ■ Period measurement mode Fig. 2.3.28	Previous change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before setting ① below, clear the interrupt enable bits (timer Y or CNTR1) and the interrupt request bits (timer Y or CNTR1) to “0”. •After setting ⑤ below, set the interrupt enable bits (timer Y or CNTR1) to “1” (interrupts enabled). After change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before timer Y stops counting (before setting ② below), clear the interrupt enable bit (timer Y or CNTR1) to “0”. •After setting ④ below, clear the interrupt request bit (timer Y or CNTR1) to “0” and next set the interrupt enable bit (timer Y or CNTR1) to “1” (interrupt enabled). •Set ⑤ last.
B	P2-72 (2) Timer Y ■ Event counter mode Fig. 2.3.29	Previous change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before setting ① below, clear the interrupt enable bits (timer Y or CNTR1) and the interrupt request bits (timer Y or CNTR1) to “0”. •After setting ⑤ below, set the interrupt enable bits (timer Y or CNTR1) to “1” (interrupts enabled). After change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before timer Y stops counting (before setting ② below), clear the interrupt enable bit (timer Y or CNTR1) to “0”. •After setting ④ below, clear the interrupt request bit (timer Y or CNTR1) to “0” and next set the interrupt enable bit (timer Y or CNTR1) to “1” (interrupt enabled). •Set ⑤ last.
B	P2-73 (2) Timer Y ■ Pulse width HL continuously measurement mode Fig. 2.3.30	Previous change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before setting ① below, clear the interrupt enable bits (timer Y or CNTR1) and the interrupt request bits (timer Y or CNTR1) to “0”. •After setting ⑤ below, set the interrupt enable bits (timer Y or CNTR1) to “1” (interrupts enabled). After change *[Notes on use]* **Notes 1:** For using interrupt processing, set the following: •Before timer Y stops counting (before setting ② below), clear the interrupt enable bit (timer Y or CNTR1) to “0”. •After setting ④ below, clear the interrupt request bit (timer Y or CNTR1) to “0” and next set the interrupt enable bit (timer Y or CNTR1) to “1” (interrupt enabled). •Set ⑤ last.

Corrections and Supplementary Explanation for “3822 Group User’s Manuals” No.4

Rev.	Page	Contents
A	P2-148 line 18	Error ■ Interrupt source selection bit ... **Note:** ... Correct (addition) **Note 2:** When an external trigger is selected, an ADT/A-D conversion interrupt may occur by switching the interrupt source selection bit from “1” to “0” or “0” to “1”. Before accepting an interrupt, set the interrupt request bit to “0” after disabling interrupts and setting the interrupt source selection bit.