Date: Feb. 10, 2012

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A830A/E	Rev.	1.00
Title	SH7786 Power-Down Mode User's Manual Correction		Information Category	Technical Notification		
Applicable Product	SH7786 Group	Lot No. All lots	Reference Document	SH7786 Group User's Manual: Hardware Rev.1.00 Nov 30, 2010 (REJ09B0501-0100)		

There are some corrections about the SH7786 Power-Down Mode user's manual.

Cancelation line parts (~~abc~~) are deleted and gray parts (abc) are newly added.

[Correction]

1. Section 20.1, Features

Reference document page 1239 2nd bullet item: Value of supply voltage

• Supports DDR3-SDRAM power supply backup mode that turns off the power supplies the ~~1.8~~1.5-V power supply

2. Section 20.1.1, Types of Power-Down Modes Table 20.1 States of Power-Down Modes

Reference document page 1240, DDR3-SDRAM power supply backup:

Conditions of Transition column and Pin column are corrected as follows.

Power-Down Mode	Conditions of Transition	State							
		CPG	CPU	On-Chip Memory	On-Chip Peripheral Module		Pin	DDR3-SDRAM	Releasing Methods
					DMAC	Others			
DDR3-SDRAM power supply backup	See section ~~12.7~~12.5.8	Stopped	Stopped	Un-defined	Stopped	Stopped	High-impedance state except for the ~~1.8~~1.5-V power supply interface	Self-refresh	Power-on reset

3. Section 20.3 Register Descriptions, Table 20.3 Register configuration

Reference document page 1241 CPU0 Ick frequency setting register line to CPU1 standby control register line: Sync clock

Register Name	Abbreviation	R/W	P4 Address	Area7 Address	Access Size	Sync clock
CPU0 Ick frequency setting register	C0IFC	R/W	H'FE40 0000	H'1E40 0000	32	~~Sck2~~ Dedicated clock
CPU1 Ick frequency setting register	C1IFC	R/W	H'FE40 1000	H'1E40 1000	32	~~Sck2~~ Dedicated clock
CPU0 standby control register	C0STBCR	R/W	H'FE40 0004	H'1E40 0004	32	~~Sck2~~ Dedicated clock
CPU1 standby control register	C1STBCR	R/W	H'FE40 1004	H'1E40 1004	32	~~Sck2~~ Dedicated clock

4. Section 20.3 Register Descriptions, Table 20.4 Register States of CPG in Each Processing Mode

1) Reference document page 1242: Table title

"Register States ~~of CPG~~ in Each Processing Mode"

2) Reference document page 1242 CPU1 standby control register: Power-on reset value is corrected as follows.

Register Name	Abbreviation	Power-on Reset	Manual Reset	Sleep/ Light Sleep
		By PRESET# Pin/WDT/H-UDI	WDT/Multiple Exceptions	By SLEEP Instruction
CPU1 standby control register	C1STBCR	~~H'0000 0001~~ H'0000 0003	Retained	Retained

5. Section 20.3.6, CPU0 Standby Control Register (C0STBCR) Table Description

Reference document page 1251, Bit 1(RESET0): Description is corrected as follows.

Bit	Bit Name	Initial Value	R/W	Description
1	RESET0	0	R/W	Reset Bit For details, see 20.5.3, CPU Core Module Stop Control. 0: ~~Don't operate a power-on reset when MSTP is cleared~~ A power-on reset is not executed to the CPU0 when MSTP0 is cleared 1: ~~Operate a power-on reset when MSTP is cleared~~ A power-on reset is executed to the CPU0 when MSTP0 is cleared Note: This bit can be set while MSTP0 is 1. When MSTP0 is cleared to 0, this bit is also cleared to 0. While MSTP0 is 0, it is prohibited to set 1 to this bit.

6. Section 20.3.7, CPU1 Standby Control Register (C1STBCR) Table Description

Reference document page 1253, Bit 1(RESET1): Description is corrected as follows.

Bit	Bit Name	Initial Value	R/W	Description
1	RESET1	1	R/W	Reset Bit For details, see 20.5.3, CPU Core Module Stop Control. 0: ~~Don't operate a power-on reset when MSTP is cleared~~ A power-on reset is not executed to the CPU1 when MSTP1 is cleared 1: ~~Operate a power-on reset when MSTP is cleared~~ A power-on reset is executed to the CPU1 when MSTP1 is cleared Note: This bit can be set while MSTP1 is 1. When MSTP1 is cleared to 0, this bit is also cleared to 0. While MSTP1 is 0, it is prohibited to set 1 to this bit.

7. Additional note for CPUn Standby Control Register (CnSTBCR; n=0, 1)

Note.

The setting value of CPUn Standby Control Register CnSTBCR (n=0, 1) bit 1 and bit 0 pair [Resetn, MSTPn] is as follows.

B'00: CPUn is operating (do not modify to B'10 from this state, C0STBCR initial value)

B'01: CPUn is in module stop and a power-on reset* is not executed to the CPU core n after release module stop

B'10: Setting prohibited (cleared to B'00)

B'11: CPUn is in module stop and a power-on reset* is executed to the CPU core n after release module stop

(C1STBCR initial value)

*: A power-on reset to the CPU core n is a similar operation with the manual reset by the WDT (CPUn).

8. Section 20.3.4, CPU0 Ick Frequency Setting Register (C0IFC)

Reference document page 1249, Bit 2 to 0 (IIFC0[2:0]): Description is corrected as follows.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	IIFC0[2:0]	000	R/W	These bits set the frequency ratio of the CPU clock that is set by FRQCR1 and the clock that is supplied internally to the CPU. 000: x1 001: x1/2 010: x1/4~~ or x1/3*~~ Other than above: Setting prohibited If the frequencies of the input Ick and SHck are equal, setting 010 is prohibited.

~~Note: * If the ratio of the input Ick and SHck is 1:3 or 1:6, the frequency ratio will be 1/3 or 1/6, respectively.~~

9. Section 20.3.5, CPU1 Ick Frequency Setting Register (C1IFC)

Reference document page 1250, Bit 2 to 0 (IIFC1[2:0]): Description is corrected as follows.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	IIFC1[2:0]	000	R/W	These bits set the frequency ratio of the CPU clock that is set by FRQCR1 and the clock that is supplied internally to the CPU. 000: x1 001: x1/2 010: x1/4~~ or x1/3*~~ Other than above: Setting prohibited If the frequencies of the input Ick and SHck are equal, setting 010 is prohibited.

~~Note: * If the ratio of the input Ick and SHck is 1:3 or 1:6, the frequency ratio will be 1/3 or 1/6, respectively.~~

- End of Correction -