Date: Jul. 27, 2010

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A777A/E	Rev.	1.00
Title	SH7780 CPG Manual Correction		Information Category	Technical Notification		
Applicable Product	SH7780 Group	Lot No. All lots	Reference Document	SH7780 Hardware Manual Rev.1.00, Dec.13.2005 (REJ09B0158-0100)		

There are corrections to the SH7780 hardware manual regarding the description of the CPG (Clock Pulse Generator).

Gray part is newly added (example: ABC) and cancellation line parts are removed (example: ~~ABC~~).

[Correction]

Reference document 15.4.1 Frequency Control Register (FRQCR) bits 24 to 16 of table (IFC0, CFC[3:0] and BFC[3:0]) and bit figure (Pages 619 and 620 of 1286) are corrected as follows.

15.4.1 Frequency Control Register (FRQCR)

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Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	IFC0~~*~~	CFC[3:0]~~*~~				BFC[3:0]~~*~~			
Initial Value	0	0	0	1	0	0	0	–	0	–	–	0	0	–	–	–
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	P1FC[3:0]~~*~~			
Initial Value	0	–	–	–	0	0	1	1	0	–	–	–	0	1	–	–
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: The initial values of these fields after power-on reset depend on the mode pins setting (see table 15.2).

Bit	Bit Name	Initial Value	R/W	Description
24	IFC0*	Undefined	R/W	CPU Clock (Ick) and SuperHyway Clock (SHck)
23	CFC3*	0	R/W	Frequency Division Ratio Setting
22	CFC2*	Undefined		00010: ×12 (Ick), ×6 (SHck) Clock operating mode 0, 1, 2 or 3 (after power-on reset)
21	CFC1*	Undefined		00100: ×12 (Ick), ×4 (SHck) Clock operating mode 12 (after power-on reset)
20	CFC0*	0		10000: ×6 (Ick), ×6 (SHck) Register setting in clock operating mode 0, 1, 2 or 3 (register setting after initialized)
				Other than above: Setting prohibited
				The initial value of this field after power-on reset depends on the mode pins setting (see table 15.2).

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19	BFC3	0	R	Bus Clock (Bck) Frequency Division Ratio ~~Setting~~
18	BFC2	Undefined	R	0011: x3
17	BFC1	Undefined	R	0100: x2
16	BFC0	Undefined	R	0101: x3/2
				0110: x1
				~~Other than above: Setting prohibited~~
				The initial value of this field after power-on reset depends on the mode pin setting (see table 15.2).
				Writing is ignored.

- End of Correction -