

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

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Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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## HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	MPU		No	TN-SH7-468A/E	Rev	1
THEME	SH7760 changes of the electrical characteristics and USB module and other modules functional explanation.		Classification of Information	1. Spec change ② Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line		
PRODUCT NAME	SH7760	Lot No.	Reference Documents	SH7760 Hardware Manual ADE-602-291 Rev. 1.0	Effective Date	
		All lots			Eternity	

This is to notify you of charges in the electrical characteristics of the SH7760, and USB as detailed below.

## 1. Absolute Maximum Ratings (Table 33.1)

Before change (rev 1.0)		After change	
Item	Symbol	Item	Symbol
I/O, CPG, ADC, USB power supply voltage	V <sub>DDQ</sub> V <sub>DD-CPG</sub> AV <sub>CC-ADC</sub>	I/O, CPG, ADC power supply voltage	V <sub>DDQ</sub> V <sub>DD-CPG</sub> AV <sub>CC-ADC</sub>

## 2. DC Characteristics (Table 33.2)

Item	Symbol	Before change (rev 1.0)			After change			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Input voltage	I2C1_SCL,I2C1_SDA, I2C0_SCL,I2C_SDA	V <sub>IH</sub>	V <sub>DDQ</sub> × 0.8	—	5.5	V <sub>DDQ</sub> × 0.7	—	5.5	V
			Other input pins	V <sub>DDQ</sub> × 0.8	—	V <sub>DDQ</sub> + 0.3	2.2	—	
	I2C1_SCL,I2C1_SDA, I2C0_SCL,I2C_SDA	V <sub>IL</sub>	-0.5	—	V <sub>DDQ</sub> × 0.1	-0.5	—	V <sub>DDQ</sub> × 0.3	

## Before change (rev 1.0)

Notes: 1. Regardless of whether or not the PLL is used, connect V<sub>DDQ</sub> and AV<sub>CC-ADC</sub> to V<sub>DD-CPG</sub>, V<sub>DD-PLL1/2/3</sub> to V<sub>DD</sub>, and V<sub>SS-CPG</sub> and V<sub>SS-PLL1/2/3</sub> to GND. The LSI may be damage when not filling this.

## After change

Notes: 1. Regardless of whether or not the PLL is used, please supply the same voltage to V<sub>DDQ</sub>, AV<sub>CC-ADC</sub> and V<sub>DD-CPG</sub>, supply the same voltage V<sub>DD-PLL1/2/3</sub> and V<sub>DD</sub>, connect V<sub>SS</sub>, V<sub>SS-CPG</sub> and V<sub>SS-PLL1/2/3</sub> to GND. The LSI may be damage when not filling this.

The continuation from 2. DC Characteristics (Table 33.2)

Before change (rev 1.0)			After change		
Item	Symbol		Item	Symbol	
Output voltage	all output pins	$V_{OH}$	Output voltage	all output pins <sup>6</sup>	$V_{OH}$

After change

Notes: 6. I2Cn\_SCL and I2Cn\_SDA pins are removed.

### 3. CMT Module Signal Timing (Table 33.13)

Item	Symbol	Before change (rev 1.0)		After change		Unit
		Min.	Max.	Min.	Max.	
CMT_CTR output delay time	$t_{TMD}$	—	36	—	8	ns
CMT_CTR input setup time	$t_{TMS}$	20	—	6	—	ns
CMT_CTR input hold time	$t_{TMH}$	20	—	2	—	ns

### 4. HCAN2 Module Signal Timing (Table 33.14)

Item	Symbol	Before change (rev 1.0)		After change		Unit
		Min.	Max.	Min.	Max.	
CAN_TX output delay time	$t_{CAND}$	—	100	—	6	ns
CAN_RX input setup time	$t_{CANS}$	100	—	4	—	ns
CAN_RX input hold time	$t_{CANH}$	100	—	2.5	—	ns

### 5. GPIO Signal Timing (Table 33.15)

Item	Symbol	Before change (rev 1.0)		After change		Unit
		Min.	Max.	Min.	Max.	
GPIO output delay time	$t_{IOPD}$	—	20	—	9	ns
GPIO input setup time	$t_{IOPS}$	20	—	7	—	ns
GPIO input hold time	$t_{IOPH}$	20	—	5	—	ns

### 6. I<sup>2</sup>C Electrical Characteristics (2. I<sup>2</sup>C DC characteristics) (Table 33.17)

Item	Symbol	Before change (rev 1.0)		After change		Unit
		Min.	Max.	Min.	Max.	
Input voltage	$t_{IH}$	$V_{DDQ} \times 0.8$	5.5	$V_{DDQ} \times 0.7$	5.5	V
	$t_{IL}$	-0.5	$V_{DDQ} \times 0.1$	-0.5	$V_{DDQ} \times 0.3$	V

### 7. I<sup>2</sup>C Electrical Characteristics (3. I<sup>2</sup>C AC characteristics) (Table 33.18)

Item	Symbol	Before change (rev 1.0)			After change			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I2Cn_SCL frequency	$t_{cyc}$	0	—	400	—	—	400	kHz
I2Cn_SCL/I2Cn_SDA rise time	$t_{Cr}$	—	—	300	$20 + 0.1Cb^*$	—	300	ns
I2Cn_SCL/I2Cn_SDA fall time	$t_{Cf}$	—	—	300	$20 + 0.1Cb^*$	—	300	ns

After change

Note: \* Cb is the total capacity of one bus line. (max. 400pF)

### 8. I<sup>2</sup>C Electrical Characteristics (4. I<sup>2</sup>C Schmitt characteristics) (Table 33.19)

Item	Symbol	Before change (rev 1.0)		After change		Unit
		Min.	Max.	Min.	Max.	
Threshold voltage	VTT+	—	$V_{DDQ} \times 0.8$	$V_{DDQ} \times 0.7$	—	V
	VTT-	$V_{DDQ} \times 0.1$	—	—	$V_{DDQ} \times 0.3$	V

9. SSI Interface Module Signal Timing (Table 33.29)

Item	Symbol	Before change (rev 1.0)		After change		Unit
		Min.	Max.	Min.	Max.	
Output cycle time	$t_{OSCK}$	T.B.D	T.B.D	40	710	ns
Input cycle time	$t_{ISCK}$	T.B.D	T.B.D	80	3300	ns
Input high level width / Output high level width	$t_{IH}/t_{OHC}$	T.B.D	—	65	—	ns
Input low level width / Output low level width	$t_{IL}/t_{OLC}$	T.B.D	—	65	—	ns

10. A/D Converter Characteristics (Table 33.30)

Before change (rev 1.0)

Notes: 2.  $AV_{CC-ADC} = GND$

After change

Notes: 2.  $AV_{SS-ADC} = GND$

11. Section 16 Timer/Counter (CMT)

Before change (rev 1.0)

16.4.4 16-Bit Timer: Input Capture 4 lines

The counters will retain their values or can be cleared to H'0000 by disabling the timer enable bits.

After change

The counters will be cleared to H'0000 by disabling the timer enable bits.

Before change (rev 1.0)

16.4.5 16-Bit Timer: Output Compare 6 lines

The counters will retain their values or can be cleared to H'0000 by disabling the timer enable bits.

After change

The counters will be cleared to H'0000 by disabling the timer enable bits.

Before change (rev 1.0)

16.4.7 Counter: Up-Counter with Capture 4 lines

The counters will retain their values or can be cleared to H'0000 by disabling the timer enable bits.

After change

The counters will be cleared to H'0000 by disabling the timer enable bits.

12. Section 21 USB Host Module (USB)

Before change (rev 1.0)

The USB Host Controller module supports Open Host Controller Interface (Open HCI) Specification for the Universal Serial Bus (USB) as well as the Universal Serial Bus specification Ver.1.1.

After change

The USB Host Controller module supports Open Host Controller Interface (Open HCI) Specification<sup>\*2</sup> for the Universal Serial Bus (USB) as well as the Universal Serial Bus specification Ver.1.1<sup>\*1</sup>.

[Note] \*1 : Moreover, refer to the USB Host Electrical Characteristics section for the electrical characteristics of USB Host.

\*2 : Part of registers is not supported. For details, see section 21.3, Register Descriptions and section 21.6, Restrictions on HcRhDescriptorA.