To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A550A/E	Rev.	1.00
Title	SH7727 Error Correction of Hardware Manual		Information Category	Technical Notification		
Applicable Product	SH3-DSP SH7700 Series SH7727 Group	Lot No. All	Reference Document	SH3-DSP SH7727 Hardware Manual (ADE-602-209C Rev. 4.0)		

SH3-DSP SH7727 Hardware Manual has following error of description.

1. page 169
Table 7.4 Interrupt Exception Handling Sources and Priority (IRQ Mode)
Error:

Interrupt Source		INTEVT Code (INTEVT2 Code)	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit	Default Priority
TMU2	TUNI2	H'440 (H'440)	0–15 (0)	IPRA (7–4)	High	
	TICPI2	H'460 (H'460)			Low	

Correction:

Interrupt Source		INTEVT Code (INTEVT2 Code)	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit	Default Priority
TMU2	TUNI2	H'440 (H'440)	0–15 (0)	IPRA (7–4)	—	

2. page 171
Table 7.5 Interrupt Exception Handling Sources and Priority (IRL Mode)
Error:

Interrupt Source		INTEVT Code (INTEVT2 Code)	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit	Default Priority
TMU2	TUNI2	H'440 (H'440)	0–15 (0)	IPRA (7–4)	High	
	TICPI2	H'460 (H'460)			Low	

Correction:

Interrupt Source		INTEVT Code (INTEVT2 Code)	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit	Default Priority
TMU2	TUNI2	H'440 (H'440)	0–15 (0)	IPRA (7–4)	—	

3. page 290
12.2.5 Individual Memory Control Register (MCR)
Error:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPC 1	TPC 0	RCD 1	RCD 0	TRW L1	TRW L0	TRA S1	TRA S0	RAS D	AMX 3	AMX 2	AMX 1	AMX 0	RFS H	RMO DE	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Correction:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPC 1	TPC 0	RCD 1	RCD 0	TRW L1	TRW L0	TRA S1	TRA S0	—	AMX 3	AMX 2	AMX 1	AMX 0	RFS H	RMO DE	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

4. page 291
12.2.5 Individual Memory Control Register (MCR)
Error:
Bit 7—SDRAM Bank Active (RASD): Specifies whether SDRAM is put into bank-active mode or auto-precharge mode. The auto-precharge mode should be used if both area 2 and area 3 are set in SDRAM space and the bus width is 16 bits.

Bit 7: RASD	Description	
0	Auto-precharge mode	(Initial value)
1	Bank-active mode	

Correction:
Bit 7—Reserved: This bit is always read as 0. The write value should always be 0.

5. page 296
Bits 8, 1, and 0—Area6 $\overline{OE}$/$\overline{WE}$ Negate Address Delay (A6TEH2, A6TEH1, and A6TEH0):
Error:

Bit 8: A6TEH2	Bit 1: A6TEH1	Bit 0: A6TEH0	Description	
0	0	0	0.5-cycle delay	(Initial value)
		1	1.5-cycle delay	
	1	0	2.5-cycle delay	
		1	3.5-cycle delay	
1	0	0	4.5-cycle delay	
		1	Reserved	
	1	0	Reserved	
		1	Reserved	

Correction:

Bit 8: A6TEH2	Bit 1: A6TEH1	Bit 0: A6TEH0	Description	
0	0	0	0.5-cycle delay	(Initial value)
		1	1.5-cycle delay	
	1	0	2.5-cycle delay	
		1	3.5-cycle delay	
1	0	0	4.5-cycle delay	
		1	5.5-cycle delay	
	1	0	6.5-cycle delay	
		1	7.5-cycle delay	

6. page 369
14.2.2 DMA Destination Address Registers 0 to 3 (DAR0 to DAR3)
Error:
To transfer data in 16 bits or in 32 bits, specify the address on the 16-bit or 32-bit boundary.
If any other address is specified, correct operation is not guaranteed.

Correction:
To transfer data in 16 bits or in 32 bits, specify the address on the 16-bit or 32-bit boundary.
To transfer data in 16 bytes, specify the address on the 16-byte boundary (16n address).
If any other address is specified, correct operation is not guaranteed.

7. page 447
16.2.15 RTC Control Register 1 (RCR1)
Error:
RCR1 is initialized to H'00 by a power-on reset. By a manual reset, bits except the CF flag are all initialized to 0, but the CF flag is undefined. When using the CF flag, it must be initialized beforehand. This register is not initialized in standby mode.

Bit:	7	6	5	4	3	2	1	0
	CF	—	—	CIE	AIE	—	—	AF
Initial Value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R	R	R/W

Correction:
CIE, AIE, and AF flag is initialized to 0 by a power-on reset and by a manual reset. But the CF flag is undefined by a power-on reset and by a manual reset. When using the CF flag, it must be initialized beforehand. This register is not initialized in standby mode.

Bit:	7	6	5	4	3	2	1	0
	CF	—	—	CIE	AIE	—	—	AF
Initial Value:	—	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R	R	R/W

8. page 462
Table 17.2 Registers
Error:

Name	Abbreviation	R/W	Initial Value	Address	Access size
Port SC control register	SCPCR	R/W	H'A888	H'04000116 (H'A4000116)*2	16

Correction:

Name	Abbreviation	R/W	Initial Value	Address	Access size
Port SC control register	SCPCR	R/W	H'8008	H'04000116 (H'A4000116)*2	16

9. page 719
Table 25.2 Register Configuration
Error:

Register Name	Abbreviation	Initial Value	Address	Access Size
LCDC power supply sequence period register	LDPSPR	H'F606	H'04000C26 (H'A4000C26)*	16

Correction:

Register Name	Abbreviation	Initial Value	Address	Access Size
LCDC power supply sequence period register	LDPSPR	H'F60F	H'04000C26 (H'A4000C26)*	16

10. page 928
Table A.1 Pin Functions
Error:

Type	Signal Name (Initial Status: Bold)	Pin No. (HQFP)	I/O	Power-On Reset	Manual Reset	Standby	Release/Open Bus Privileges
Serial related	**SCK_SIO**/SCPT[5], **SIOFSYNC**/SCPT[6]	196, 197	IO/IO	I	Z/P	Z/K	IO/P

Correction:

Type	Signal Name (Initial Status: Bold)	Pin No. (HQFP)	I/O	Power-On Reset	Manual Reset	Standby	Release/Open Bus Privileges
Serial related	**SCK_SIO**/SCPT[5],	196	IO/IO	I	Z/P	Z/K	IO/P
	SIOFSYNC/SCPT[6]	197	IO/IO	I	Z/P	K/K	IO/P