RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RZ*-A048A/E | Rev. | 1.00 |
|-----------------------|--|----------|-------------------------|--|------|------|
| Title | RZ/T1 Group User's Manual: Hardware Correction of CKIOSET register description a Electrical Characteristics description in Bus s controller | | Information Category | Technical Notification | | |
| | | Lot No. | | | | |
| Applicable Product | RZ/T1 Group | All lots | Reference Document | RZ/T1 User's Manual: Hardw R01UH0483EJ0130 R | | 1.30 |

Incorrect description of the CKIOSET register for bus state controller have been found.

This document describes correct description of CKIOSET register in User's manual.

And also, there are expressions in the electrical characteristics (bus timing) regarding CKIO pin, which may cause misunderstanding. We change expressions of electrical characteristics (bus timing) regarding CKIO pin (There is no change in specification itself).

1. CKIOSET register

1) Contents

Although it is written in the current user's manual that CKIO pin drive ability can be set by setting the CKIOSET register, in fact it does not affect the drive ability and it affects the timing of CKIO signal and the other output signals of Bus state controller. Because this register affects the timing of the output signals as address, there is a possibility that the electrical characteristics (bus timing) does not meet the specification when changing this register setting from initial value. CKIOSET register must be set "0h" (initial value).

CKIO pin drive ability can be set by setting the Driving Ability Control Register (DSCR).



3) Correction of User's Manual

[1] Correct descriptions of CKIOSET register.

| Page | Chapter | | | | Description | | |
|----------------|---------|--|--|-----------------|--|-------------------|--|
| 123 of 2609 | 14.3.10 | [Current description] 14.3.10 CKIO Control Register (CKIOSET) | | | | | |
| | | When CK (CKIOSET When the | IO is used at a fr = 0h). CKIO is to be used he CKIOSET | equency of or | bility of the CKIO clock. above 50 MHz, set the CKIO driving ability cy below 50 MHz, the CKIO can be set to 4m. | | |
| | | consecutiv Write 1 by Write 1 by | | o register CKIC | KEY. | peration | |
| | | Bit | Symbol | Bit Name | Description | R/W | |
| | | b3-b0 | CKIOSET[3:0] | | CKIO control 0x0: When CKIO driving ability is set at 8mA. 0xA: When CKIO driving ability is set at 4mA. | R/W | |
| | | bits to Ah. | | | | | |
| | | | o use this registe [3:0] bits to 0x0. | r with initial | value. When setting the register, be sure to | o set th | |
| | | consecutiv Write 1 by Write 1 by | | o register CKIC | KEY. | peration | |
| | | Bit | Symbol | Bit Name | Description | R/W | |
| | | b3-b0 | CKIOSET[3:0] | Dir Namo | CKIO control 0x0: When CKIO driving ability is set at 8mA. 0xA: When CKIO driving ability is set at 4mA. | R/W | |
| | | | | | Be sure to set CKIOSET[3:0] = 0b (value after reset). | | |
| | | 03-00 | | | 0x0: When CKIO driving abilit 0xA: When CKIO driving abilit Be sure to set CKIOSET | ty is set at 4mA. | |



[2] Correct "notes" for Bus state controller electrical characteristics (bus timing).

| Page | Chapter | Description |
|---------|---------|---|
| 2502 of | 47.4.3 | [Current description] |
| 2609 | | Table 47.17 |
| | | Note 1. Examine the fmax value of CKIO (external bus clock) together with the number of waits in accordance with system configuration. When CKIO is used at a frequency of or above 50 MHz, set the CKIO driving ability at 8 mA (CKIOSET = 0h). When the CKIO is to be used at a frequency below 50 MHz, the CKIO can be set to 4 mA. In this case, set the CKIOSET bits to Ah. Note 3. Values when SDRAM is used. Note 4. Values when CKIO driving ability is set at 8 mA/4 mA. |
| | | [Correct description] |
| | | Table 47.17 |
| | | Note 1. Examine the fmax value of CKIO (external bus clock) together with the number of waits in accordance with system configuration. When CKIO is used at a frequency of or above 50 MHz, set the B0 bit of Driving Ability Control Register (DSCR) to 1 (High-drive output). When CKIO is used at a frequency of below 50MHz, set the B0 bit of Driving Ability Control Register (DSCR) to 0(Normal output). |
| | | Note 3. Values when set the CSn Space Bus Control Register (CSnBCR) to "SDRAM (TYPE[2:0] bits = 100b)" and set Driving Ability Control Register (DSCR) to "High-drive output (B0 bit = 1)". |
| | | Note 4. Values when Driving Ability Control Register (DSCR) is set at High-drive output (B0 bit = 1) or Normal output (B0 bit = 0). |



- 2. Change expressions of electrical characteristics (bus timing) regarding CKIO pin
- 1) Contents

As current expression of electrical characteristic regarding CKIO pin may cause misunderstanding, we change the expressions as follows (There is no change in specification itself).

2) Correction to User's Manual

| B [Current description] Table 47.17 Item Address delay time 1 Address delay time 2 CS# delay time Read/write delay time 1 Read data setup time 1 Read data setup time 2 Read data setup time 3 Write enable delay time 1 WAIT# setup time WAIT# hold time AH# delay time Address setup time to AH# Note 1. Examine the fmax value of configuration. When CKIO (CKIOSET = 0h). When th In this case, set the CKIOS Note 3. Values when SDRAM is use Note 4. Values when CKIO driving at the construction of the configuration. [Correct description] Table 47.17 Item Address delay time 1 Address delay time 2 CS# delay time Read/write delay time 1 | is used at a freque e CKIO is to be us SET bits to Ah. ed. | Min. 0/2 '3 1/2t _{cyc} 0/2 '3 0/2 '3 1/2t _{cyc} <th></th> <th>ns ns ns ns ns ns ns ns ns swaits in accordanc O driving ability at CKIO can be set</th> <th>8 mA</th> | | ns ns ns ns ns ns ns ns ns swaits in accordanc O driving ability at CKIO can be set | 8 mA |
|---|---|--|--|---|--|
| Item Address delay time 1 Address delay time 2 CS# delay time 2 CS# delay time Read/write delay time Read data setup time 1 Read data setup time 2 Read data setup time 2 Read data setup time 3 Write enable delay time 1 WAIT# setup time WAIT# hold time Address setup time to AH# Note 1. Examine the fmax value of configuration. When CKIO (CKIOSET = 0h). When th In this case, set the CKIOS Note 3. Values when SDRAM is us Note 4. Values when CKIO driving a [Correct description] Table 47.17 Item Address delay time 1 Address delay time 2 CS# delay time | tad1 tad2 tad4 tave CKIO (external buist to be us SET bits to Ah. ed. ability is set at 8 m SDRAM '3 Other than SDRAM '3 Other than SDRAM | Min. 0/2 '3 1/2t _{cyc} 0/2 '3 0/2 '3 1/2t _{cyc} <td>Max. 10 1/2t_{cyc} +10 10 10 10 1/2t_{cyc} +10 7'4 - 7'4 - 1/2t_{cyc} +10 8'4 5 1/2t_{cyc} +10 2 - er with the number of v e 50 MHz, set the CKIC hcy below 50 MHz, the CKIO=1/tcx Min. 2 0 1/2tcxcyc 2</td> <td>Image: nstep in the image: nstep in</td> <td>8 mA to 4 mA.</td> | Max. 10 1/2t _{cyc} +10 10 10 10 1/2t _{cyc} +10 7'4 - 7'4 - 1/2t _{cyc} +10 8'4 5 1/2t _{cyc} +10 2 - er with the number of v e 50 MHz, set the CKIC hcy below 50 MHz, the CKIO=1/tcx Min. 2 0 1/2tcxcyc 2 | Image: nstep in the image: nstep in | 8 mA to 4 mA. |
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| Address delay time 2 CS# delay time Read/write delay time 1 Read strobe delay time 1 Read data setup time 2 Read data setup time 2 Read data setup time 3 Write enable delay time 1 WAIT# setup time WAIT# hold time AH# delay time to AH# Note 1. Examine the fmax value of configuration. When CKIO (CKIOSET = 0h). When th In this case, set the CKIOS Note 3. Values when SDRAM is using Note 4. Values when CKIO driving a [Correct description] Table 47.17 Item Address delay time 1 | tad2 tcSD1 tRVD1 tRSD tRD31 tRD32 tRD33 tRD31 tRD32 tRD31 tRD31 tRD32 tRD31 tRD31 tRD31 tRD31 tRD31 tRD31 tRD32 tRD31 tRD31 tRD32 tRD31 tRD31 tRD31 tRD31 tRD31 tRD31 tRD32 tRD31 tRD31 tRD32 tRD31 tRD31 tRD32 tRD333 tRD333 tRD334 tRD335 tRD335 tRD335 | 1/2t _{cyc} 0/2 '3 0/2 '3 1/2t _{cyc} 1/2t _{cyc} +4/7 1/2t _{cyc} +4/7 1/2t _{cyc} +4/7 1/2t _{cyc} +4.5/ 1/2t _{cyc} +4.5/ 1/2t _{cyc} +4.5/ 1/2t _{cyc} +3.3 1/2t _{cyc} -2 1s clock) togeth ency of or above sed at a frequent hA/4 mA. Symbol t _{AD1} t _{AD1} | 1/2t _{cyc} +10 10 10 10 1/2t _{cyc} +10 7'4 | ns | 8 mA to 4 mA. |
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| Note 1. Examine the fmax value of configuration. When CKIO (CKIOSET = 0h). When the In this case, set the CKIOS Note 3. Values when SDRAM is us. Note 4. Values when CKIO driving a local dri | CKIO (external build is used at a freque e CKIO is to be us SET bits to Ah. ed. ability is set at 8 n SDRAM ^{*3} Other than SDRAM ^{*3} Other than SDRAM | IS clock) togethered of or above sed at a frequent a frequent and/4 mA. | er with the number of v e 50 MHz, set the CKIC hcy below 50 MHz, the CKIO=1/tck Min. 2 0 1/2tckeyc 2 | waits in accordance O driving ability at CKIO can be set KIO can be set Max. 10 10 1/2tckeye +10 10 | 8 mA to 4 mA. |
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| Table 47.17 Item Address delay time 1 Address delay time 2 CS# delay time | Other than SDRAM SDRAM ^{*3} Other than SDRAM | t _{AD1} | Міп. 2 0 1/2t _{СКоус} 2 | Мах. 10 10 1/2t _{СКсус} +10 10 | ns ns ns ns |
| Item Address delay time 1 Address delay time 2 CS# delay time | Other than SDRAM SDRAM ^{*3} Other than SDRAM | t _{AD1} | Міп. 2 0 1/2t _{СКоус} 2 | Мах. 10 10 1/2t _{СКсус} +10 10 | ns ns ns ns |
| Address delay time 2 CS# delay time | Other than SDRAM SDRAM ^{*3} Other than SDRAM | t _{AD1} | Міп. 2 0 1/2t _{СКоус} 2 | Мах. 10 10 1/2t _{СКсус} +10 10 | ns ns ns |
| Address delay time 2 CS# delay time | Other than SDRAM SDRAM ^{*3} Other than SDRAM | t _{AD2} | 0 1/2 <u>tckcyc</u> 2 | 10 1/2t _{CKcyc} +10 10 | ns ns ns |
| CS# delay time | SDRAM SDRAM ^{*3} Other than SDRAM | t _{AD2} t _{CSD1} | <u>1/2tсксус</u> 2 | 1/2t _{CKcyc} +10 10 | ns ns |
| CS# delay time | Other than SDRAM | tcsD1 | 2 | 10 | ns |
| | Other than SDRAM | | | | |
| Read/write delay time 1 | SDRAM | | 0 | 10 | |
| Read/write delay time 1 | | t _{RWD1} | 2 | 10 | ns |
| | Other than | | 0 | 10 | ns |
| | SDRAM | | | | |
| Read strobe delay time | | t _{RSD} | 1/2 <mark>t_{CKcyc}</mark> | 1/2 <mark>t_{СКсус} +1</mark> 0 | ns |
| Read data setup time 1 *4 | High-drive output | t _{RDS1} | 1/2t _{CKcyc} +4 | - | ns |
| Decid data active time 0 *4 | Normal output | | 1/2t _{CKcyc} +7 | - | ns |
| Read data setup time 2 | output | TRDS2 | | - | ns |
| | output | | | | 115 |
| Read data setup time 3 *4 | | t _{RDS3} | 1/2t _{CKcyc} +4 | _ | ns |
| | Normal output | | 1/2t _{CKcyc} +7 | - | ns |
| Write enable delay time 1 WAIT# setup time ^{*4} | | twed1 twts | 1/2t _{CKcyc} 1/2t _{CKcyc} +4.5 | 1/2 <mark>t_{CKcyc} +10</mark> — | ns ns |
| | Normal | ┥ ┝ | 1/2t _{СКсус} +8 | - | ns |
| WAIT# hold time | Juliput | twrн | 1/2t _{CKcyc} +3.5 | - | ns |
| | | | | | ns |
| Address setup time to AH# | | t _{AVVH} | 1/2t _{CKcyc} – 2 | - | ns |
| configuration. When CKIO Register (DSCR) to 1 (High Driving Ability Control Regis Note 3. Values when set the CSn S | is used at a freque n-drive output). Wi ster (DSCR) to 0(I Space Bus Control | us clock) togethe ency of or above nen CKIO is use Normal output). Register (CSnE | e 50 MHz, set the B0 b ed at a frequency of be BCR) to "SDRAM (TYP | it of Driving Ability low 50MHz, set th | y Control ne B0 bit of |
| | Write enable delay time 1 WAIT# setup time ^{*4} WAIT# hold time AH# delay time Address setup time to AH# Note 1. Examine the fmax value of configuration. When CKIO Register (DSCR) to 1 (High Driving Ability Control Register (DS Ability Control Register (DS | Read data setup time 2 *4 High-drive output Normal output Normal output Read data setup time 3 *4 High-drive output Wormal output Normal output Write enable delay time 1 Normal output WAIT# setup time *4 High-drive output Normal output Normal output WAIT# hold time Address setup time to AH# Note 1. Examine the fmax value of CKIO (external bu configuration. When CKIO is used at a freque Register (DSCR) to 0 (High-drive output). Wh Driving Ability Control Register (DSCR) to 0 (I) Note 3. Values when set the CSn Space Bus Control Ability Control Register (DSCR) to "High-drive | Read data setup time 2 *4 High-drive output Items2 Normal output Normal output Items2 Read data setup time 3 *4 High-drive output Items3 Write enable delay time 1 Items3 WAIT# setup time *4 High-drive output Items1 WAIT# hold time Items1 AH# delay time to AH# Items1 Address setup time to AH# Items1 Note 1. Examine the fmax value of CKIO (external bus clock) togeth configuration. When CKIO is used at a frequency of or abov Register (DSCR) to 1 (High-drive output). When CKIO is use Driving Ability Control Register (DSCR) to 0(Normal output). Note 3. Values when set the CSn Space Bus Control Register (CSCR) Ability Control Register (DSCR) to "High-drive output (B0 bit | Read data setup time 2 ^{*4} High-drive output tRDS2 6.6 Normal output 10 10 Read data setup time 3 ^{*4} High-drive output 10 Read data setup time 3 ^{*4} High-drive output 1/2tckcyc +4 Write enable delay time 1 tweb1 1/2tckcyc WAIT# setup time ^{*4} High-drive output 1/2tckcyc +4.5 WAIT# hold time twrs 1/2tckcyc +4.5 WAIT# hold time twrth 1/2tckcyc +3.5 AH# delay time taHD 1/2tckcyc -2 Note 1. Examine the fmax value of CKIO (external bus clock) together with the number of v configuration. When CKIO is used at a frequency of or above 50 MHz, set the 80 t Register (DSCR) to 1 (High-drive output). When CKIO is used at a frequency of be Driving Ability Control Register (DSCR) to 0(Normal output). Note 3. Values when set the CSn Space Bus Control Register (CSnBCR) to "SDRAM (TYF Ability Control Register (DSCR) to "High-drive output, Bo bit = 1)". | Read data setup time 2 ¹⁴ High-drive output tRDs2 6.6 - Read data setup time 3 ¹⁴ High-drive output tRDs3 10 - Read data setup time 3 ¹⁴ High-drive output tRDs3 1/2tcKeyc +4 - Write enable delay time 1 twEb1 1/2tcKeyc +7 - Write enable delay time 1 twEb1 1/2tcKeyc +4.5 - WAIT# setup time ¹⁴ High-drive output twTs 1/2tcKeyc +4.5 - WAIT# hold time twTH 1/2tcKeyc +3.5 - - At# delay time taHD 1/2tcKeyc = 4.5 - - Note 1. Examine the fmax value of CKIO (external bus clock) together with the number of waits in accordance configuration. When CKIO is used at a frequency of or above 50 MHz, set the B0 bit of Driving Ability Register (DSCR) to 1 (High-drive output). When CKIO is used at a frequency of below 50MHz, set th Driving Ability Control Register (DSCR) to 0(SCR) to 0(SCRBCR) to "SDRAM (TYPE[2:0] bits = 100t |

