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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A012A/E	Rev.	1.00
Title	RZ/A1 Series: Notes about Sync Separator Circuit of Digital Video Decoder		Information Category	Technical Notification		
Applicable Product	See following	Lot No. All	Reference Document	See following		

In the following applicable products, description deficiency of specification about Sync Separator Circuit of Digital Video Decoder is found.

The detail of description deficiency is shown in bellow. According to this update, relevant manuals will be revised.

Applicable products and relevant documents

Applicable products		Relevant documents	Rev.	Document number
series	Group			
SH7260	SH7268, SH7269	SH7268 Group, SH7269 Group User's Manual: Hardware	Rev 2.00	R01UH0048EJ0200
RZ/A	RZ/A1H, RZ/A1M	RZ/A1H Group, RZ/A1M Group User's Manual: Hardware	Rev 2.00	R01UH0403EJ0200

1. The detail of description deficiency of specification

Notes about output timing adjustment of the horizontal and vertical sync signals of sync separator circuit of digital video decoder is not described in the User's Manual.

2. Additional specification details

As an example, additional specification for RZ/A1H Group and RZ/A1M Group is described in this technical update.

- Add notes in Page30-90 “30.5.3 (10) Timing Adjustment and Signal Detection Block”. (Additional portion is described in red)

The timing adjustment and signal detection block adjusts the output timing of the horizontal and vertical sync signals generated using (7) and (8) above. This block also detects the field; whether the interlaced or progressive system is used can be checked with VSYNCSR.INTERLACED. If the field detection function is unstable, setting SYNSCR5.VSYNCDELAY to 1 may improve the function.

The phases of the Hsync and Vsync signals are adjusted according to the result of detecting the field, and output of the Vsync signal from the sync separator circuit is delayed by one horizontal period. When having video display controller 5 capture the output signal from this module, take the above delay into consideration and set SC*_SCL*_DS2.SC*_RES_VS (vertical position setting for video signal capturing) as follows.

VSYNC + (V backporch - 2) lines

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