

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-RZ*-A0151A/E	Rev.	1.00
Title	RZ/A Series: Note about IRQ Interrupt request register erroneous clear of Interrupt Controller.	Information Category	Technical Notification		
Applicable Product	See following	Lot No.	Reference Document	See following	
		All			

In the following applicable products, if you want to clear the IRQ interrupt of Interrupt Controller, there are following precautions.

1 Applicable Products and Related Materials

Applicable products		Relevant documents	Rev.	Document number
series	Group			
RZ/A	RZ/A1H, RZ/A1M	RZ/A1H Group, RZ/A1M Group User's Manual: Hardware	Rev.7.00	R01UH0403EJ0700
	RZ/A1L, RZ/A1LU, RZ/A1LC	RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group User's Manual: Hardware	Rev.7.00	R01UH0437EJ0700
	RZ/A2M	RZ/A2M Group User's Manual: Hardware	Rev.5.00	R01UH0746EJ0500

2 Note

In the clearing process of multiple edge-detected IRQ interrupts, unintended IRQ interrupts may be cleared.

3 Conditions of occurrence

If you are using two or more IRQs that select the falling edge/rising edge/both edges for interrupt detection.

4 Phenomenon

In the process of clearing IRQ interrupt,

If the next IRQ interrupt occurs at the time when the IRQ Interrupt Request Register (hereinafter referred to as IRQRR) read is executed, Writing 0x0000 to IRQRR may clear not only the first interrupt but also the next interrupt.

5 Measures

If you want to clear the edge-detected IRQ interrupt, read IRQRR and check the status of IRQnF=1 that you want to clear, and then set 0 to the IRQnF you want to clear and set 1 to the other IRQmF.

Example : Clear IRQ0 interrupt

1 : Read IRQRR and check IRQ0F=1.

2 : Set 0x00FE to the IRQRR and clear IRQ0 interrupt.

Notes:

It is prohibited to write to IRQRR the value that result of the bitmasking process of writing 0 to the IRQnF you want to clear for the value that read from IRQRR.

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