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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A159A/E	Rev.	1.00
Title	RX64M, RX71M Group Modified electrical characteristics		Information Category	Technical Notification		
Applicable Product	RX71M Group、RX64M Group	Lot No. All	Reference Document	RX71M Group User's Manual: Hardware、(R01UH0493EJ0100) RX64M Group User's Manual: Hardware (R01UH0377EJ100)		

This document describes modifications in section 64 Electrical Characteristics.

No.	Chapter No.	Revised Point	Content
1	64.2 DC Characteristics	Table 64.2 (RX64M, RX71M)	Delete VIH and VIL of XCIN
2	64.2 DC Characteristics	Table 64.3 (RX64M, RX71M)	Modified ports of Input pull-up MOS current
3	64.3.7 Timing of On-Chip Peripheral Modules	Figure 64.48 (RX64M, RX71M)	Modified a parameter name
4	64.7 Temperature Sensor Characteristics	Table 64.49 (RX64M) Table 64.50 (RX71M)	Modified sampling time and added a note
5	64.10 Battery Backup Function Characteristics	Figure 64.84 (RX64M) Figure 64.88 (RX71M)	Figure update
6	64.11 Flash Memory Characteristics	Table 64.54 (RX64M) Table 64.55 (RX71M)	Specs added for blank check time of flash memory
7	64.1 Absolute Maximum Ratings	Table 64.1 (RX64M, RX71M)	Modified rated value for reference power supply voltage
8＊	64.11 Flash Memory Characteristics	Table 64.55 (RX71M)	Modified a spec for Forced stop command of flash memory

＊ No.8 is for RX71M only.

(1) 64.2 DC Characteristics

The VIH and VIL of XCIN are deleted in Table 64.2 DC Characteristics (1).

【Before】

Item		Symbol	min	typ	max	Unit	Test Conditions
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, TCK, SSI input pin, SDHI input pin, MMC input pin, PDC input pin, QSPI input pin		VCC × 0.8	—	VCC + 0.3		
	ETHERC input pin		2.3	—	VCC + 0.3		
	XCIN		—	—	VCC + 0.3		
	D0 to D31		VCC × 0.7	—	VCC + 0.3		
	RIIC(SMBus)		2.1	—	5.8		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	−0.3	—	VCC × 0.1	V	
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, TCK, SSI input pin, SDHI input pin, MMC input pin, PDC input pin, QSPI input pin		−0.3	—	VCC × 0.2		
	XCIN		−0.3	—	—		
	D0 to D31		−0.3	—	VCC × 0.3		
	RIIC(SMBus)		−0.3	—	0.8		

【After】

Item		Symbol	min	typ	max	Unit	Test Conditions
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, TCK, SSI input pin, SDHI input pin, MMC input pin, PDC input pin, QSPI input pin		VCC × 0.8	—	VCC + 0.3		
	ETHERC input pin		2.3	—	VCC + 0.3		
	D0 to D31		VCC × 0.7	—	VCC + 0.3		
	RIIC(SMBus)		2.1	—	5.8		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	−0.3	—	VCC × 0.1	V	
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, TCK, SSI input pin, SDHI input pin, MMC input pin, PDC input pin, QSPI input pin		−0.3	—	VCC × 0.2		
	D0 to D31		−0.3	—	VCC × 0.3		
	RIIC(SMBus)		−0.3	—	0.8		

(2) 64.2 DC Characteristics

The port 35 of input pull up MOS current is deleted in Table 64.3 DC Characteristics (2)。

【Before】

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input pull-up MOS current	Ports 0 to 2, 3, 4 to G, J3, J5	Ip	−300	—	−10	μA	VCC = 2.7 to 3.6V Vin = 0V

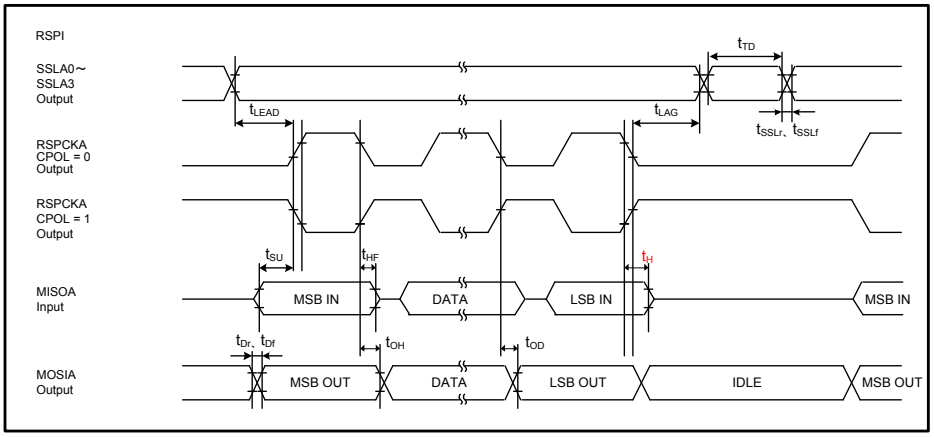
【After】

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input pull-up MOS current	port 0 to 2、 port 30 to 34、36、37、 port 4 to G、port J3, J5	Ip	−300	—	−10	μA	VCC = 2.7 to 3.6V Vin = 0V

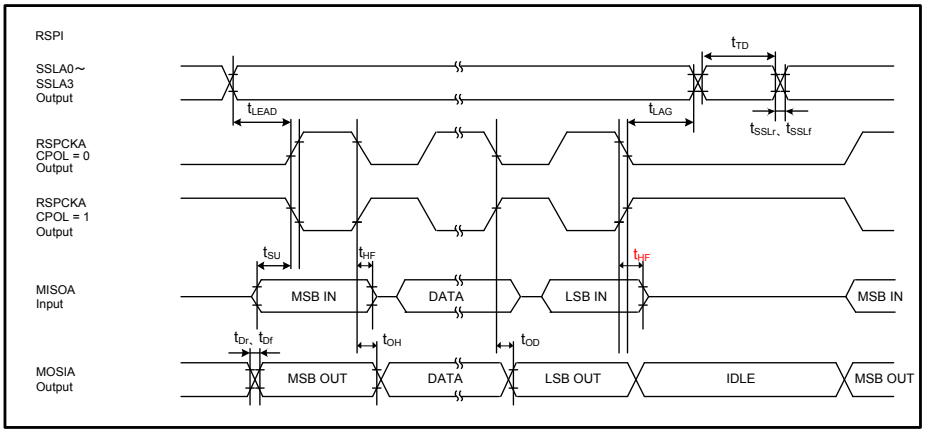
(3) 64.3.7 Timing of On-Chip Peripheral Modules

The parameter name “t_H” is revised to “t_{HF}” in Figure 64.48 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Division Ratio Set to 1/2).

【Before】



【After】



(4) 64.7 Temperature Sensor Characteristics

Test condition is removed and a note is added in Table 64.49 (RX64M) / Table 64.50 (RX71M) Temperature Sensor Characteristics.

■Table 64.49 (RX64M)

【Before】

Item	min.	typ.	max.	Unit	Test Conditions
Sampling time	—	—	4.15	μs	ADSSTRT.SST[7:0] = 250 states

【After】

Item	min.	typ.	max.	Unit	Test Conditions
Sampling time (Note.1)	4.15	—	—	μs	

Note1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

■Table 64.50 (RX71M)

【Before】

Item	min.	typ.	max.	Unit	Test Conditions
Sampling time	4.15	—	—	μs	

【After】

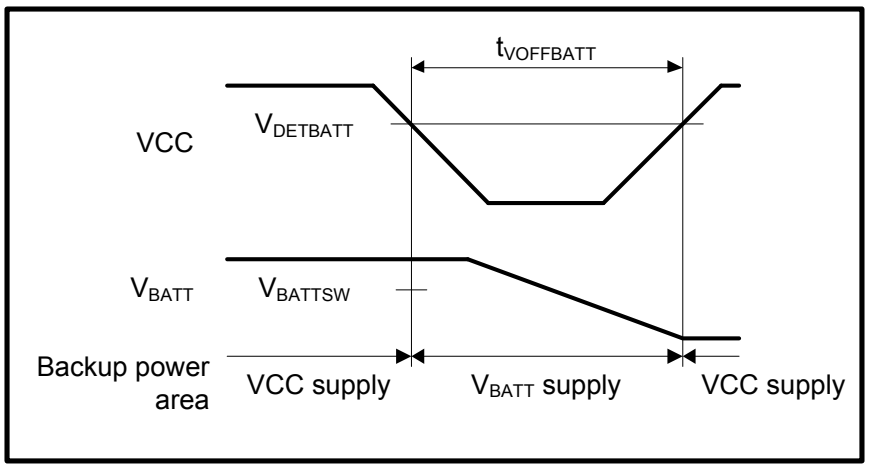
Item	min.	typ.	max.	Unit	Test Conditions
Sampling time (Note.1)	4.15	—	—	μs	

Note1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

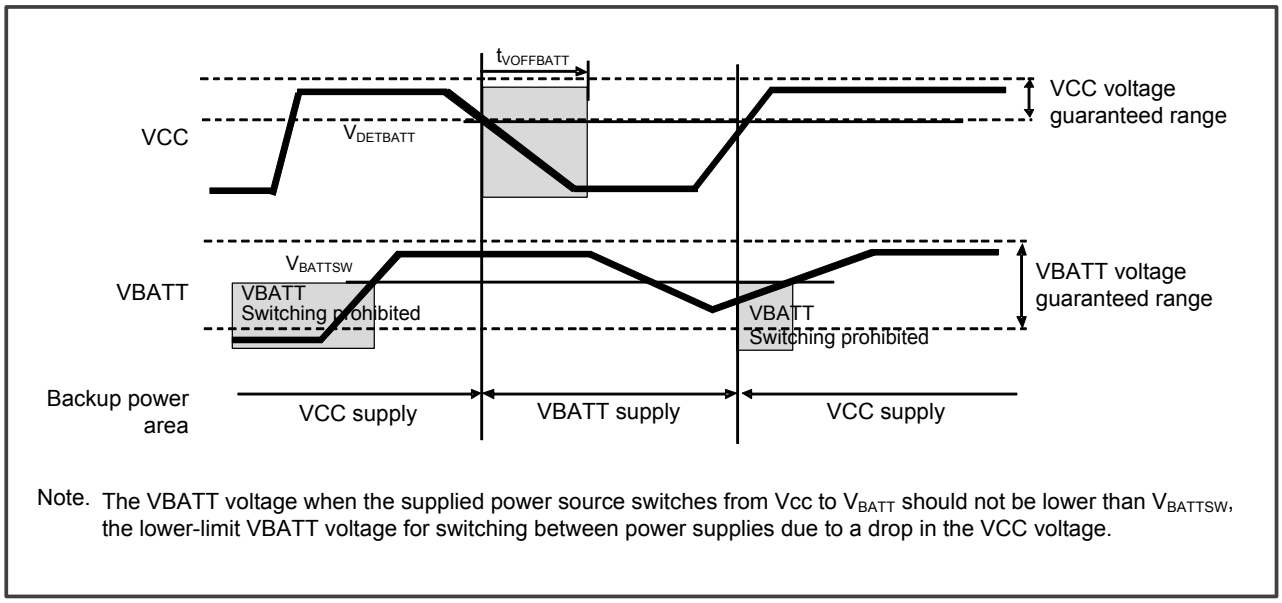
(5) 64.10 Battery Backup Function Characteristics

Figure 64.84(RX64M) / Figure 64.88(RX71M) Battery Backup Function Characteristics is revised.

【Before】



【After】



Note. The VBATT voltage when the supplied power source switches from Vcc to V_{BATT} should not be lower than V_{BATTSW}, the lower-limit VBATT voltage for switching between power supplies due to a drop in the VCC voltage.

(6) 64.11 Flash Memory Characteristics

Specs for blank check time are added in Table 64.54 (RX64M) / Table 64.55(RX71M) Data Flash Memory Characteristics.

■Table 64.54 (RX64M)

【Before】

Item		Symbol	FCLK = 4MHz			20MHz ≦ FCLK ≦ 60MHz			Unit
			min	typ	max	min	typ	max	
Blank check time	4bytes	t_{DBC4}	–	–	84*	–	–	30	μs

. "TBD" is changed to "84" as described in TU (TN-RX-A146A/E).

【After】

Item		Symbol	FCLK = 4MHz			20MHz ≦ FCLK ≦ 60MHz			Unit
			min	typ	max	min	typ	max	
Blank check time	4bytes	t_{DBC4}	–	–	84	–	–	30	μs
	64bytes	t_{DBC64}	–	–	280	–	–	100	μs
	2Kbytes	t_{DBC2k}	–	–	6169	–	–	2200	μs

■Table 64.55 (RX71M)

【Before】

Item		Symbol	FCLK = 4MHz			20MHz ≦ FCLK ≦ 60MHz			Unit
			min	typ	max	min	typ	max	
Blank check time	4bytes	t_{DBC4}	–	–	84	–	–	30	μs

【After】

Item		Symbol	FCLK = 4MHz			20MHz ≦ FCLK ≦ 60MHz			Unit
			min	typ	max	min	typ	max	
Blank check time	4bytes	t_{DBC4}	–	–	84	–	–	30	μs
	64bytes	t_{DBC64}	–	–	280	–	–	100	μs
	2Kbytes	t_{DBC2k}	–	–	6169	–	–	2200	μs

(7) 64.1 Absolute Maximum Ratings

Rated value for reference power supply voltage is modified in Table 64.1.

【Before】

Item	Symbol	Value	Unit
Reference power supply voltage	VREFH0	−0.3 to VCC + 0.3	V

【After】

Item	Symbol	Value	Unit
Reference power supply voltage	VREFH0	−0.3 to AVCC0 + 0.3	V

(8) 64.11 Flash Memory Characteristics

A spec of Forced stop time is modified in Table 64.55 (RX71M)

【Before】

Item	Symbol	FCLK = 4MHz			20MHz ≦ FCLK ≦ 60MHz			Unit
		min	typ	max	min	typ	max	
Forced stop command	t_{FD}	–	TBD	32	–	–	20	μs

【After】

Item	Symbol	FCLK = 4MHz			20MHz ≦ FCLK ≦ 60MHz			Unit
		min	typ	max	min	typ	max	
Forced stop command	t_{FD}	–	–	32	–	–	20	μs

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