RENESAS TECHNICAL UPDATE

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Title	RX610 Group Notes while using multiple units of A/D converter and while using D/A converter		Information Category	Technical Notification		
Applicable Product	RX610 Group	Lot No. All lots	Reference Document	RX610 Group Hardware Manual		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of notes when using multiple units of A/D converter, and when using the A/D converter and D/A converter simultaneously in the RX610 group.

1. Notes when using multiple units of A/D Converter

Since the same power supply is used between the units of the A/D converter contained in the RX610 group, when multiple units are used and conversion start timing between each unit is different, conversion accuracy may get affected. When the conversion accuracy is affected, adopt the following methods and perform an adequate evaluation.

(1) Example of recommended operation of simultaneous conversion of each unit at the time of multiple unit operation When multiple units of A/D converter are used, select the activation method of the trigger select bit as either activation by compare match from TPU or activation by compare match from TMR, and match the conversion start timing and end timing of each unit.

Figure 1 shows timing example 1 when the conversion timings of four units are simultaneous. Figure 2 shows timing example 2 when the conversion timings of four units are simultaneous.

-	Timer activation	
ADCLK		
Unit 0	Input sampling time	Successive approximation time
Unit 1	Input sampling time	Successive approximation time
Unit 2	Input sampling time	Successive approximation time
Unit 3	Input sampling time Identical state	Successive approximation time

Figure 1: Example of simultaneous conversion timings of four units - Case 1

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1 Conversion period

Figure 2: Example of simultaneous conversion timings of four units - Case 2

(2) Register settings of recommended operation

The following registers and bits should be set to the same value between all of the units.

- · A/D sampling state register (ADSSTR)
- · Clock select bits (ADCR.CKS[1:0])
- Trigger select bits (ADCR.TRGS[2:0])
- (3) Trigger selection corresponding to number of units

The number of units that can be activated depends on the selected trigger. See the following table.

No.	Trigger selection	ADCR.TRGS[2:0]	Number of multiple units		
			4	3	2
1	Activation by compare match A to D*1 from TPU0	100b	Possible	Possible	Possible
2	Activation by compare match A from TPU0 to TPU5*2	001b	Possible	Possible	Possible
3	Activation by compare match A of TPU6 to TPU11*2	101b	Possible	Possible	Possible
4	Activation by compare match A of TMR0*3	010b	Impossible	Impossible	Possible
5	Activation by compare match A of TMR2*3	010b	Impossible	Impossible	Possible

*1 Set the same value to TGRA to TGRD.

*2 The compare match A that is to be input to each unit of A/D converter should be set for the same TPU channel.

*3 Units 0 and 1 of A/D converter become compare match A of TMR0, and units 2 and 3 of become compare match A of TMR2.

For details on activation method of each unit, see sections 23.3.5 Activation on Compare-Match/Input-Capture A to D Signals of TPU0, 23.3.6 Activation on Compare-Match/Input-Capture A Signals of TPU0 to TPU5, and 23.3.7 Activation on Compare-Match of TMR Units of the RX610 Group Hardware Manual.

(4) Other procedures

• Perform an averaging procedure using a program.

Averaging procedure example: Perform A/D conversion of the analog input to identical pins successively for four times. Calculate an average of two values of the A/D conversion result excluding the maximum value and the minimum value.

• When the A/D converter is operated asynchronously, ensure that the conversion of one unit is complete and then operation of another single unit is started.



2. Notes when using the A/D converter and D/A converter simultaneously

Because the A/D converter and the D/A converter of the RX610 group use the same power supply, conversion accuracy of A/D conversion result may get affected depending on the usage. The conversion accuracy is likely to be affected in the following cases.

- · If the D/A data register (DADR) of D/A converter is rewritten while the A/D converter is being operated
- · If the D/A control register (DACR) is rewritten by setting a value other than 000h to the DADR

When conversion accuracy is affected, implement the following measures.

2.1 Method of rewriting DADR with AD converter operated

When rewriting the DADR while the AD converter is being operated, implement any one of the following methods.

- (1) When the DADR register is rewritten, discard the result of the A/D converter that is undergoing conversion.
- (2) When the DADR register is written, perform an averaging procedure for the A/D conversion result using a program. Averaging procedure example: Perform A/D conversion of the analog input to identical pins successively for four times. Calculate an average of two values of the A/D conversion result excluding the

maximum and minimum values.

(3) Set the rewriting procedure for DADR register as follows.

When the DADR register is written, keep the difference before changing and after changing at less than 100h, and when the next data is written, keep an interval of more than one conversion period of A/D converter. However, when rewriting is performed by maintaining the difference before and after changing at less than 080h, it is not necessary to maintain an interval of more than one conversion period of A/D converter.

Further, when multiple units of A/D converter are operated, implement "1. Notes when using multiple units of A/D Converter" and match one conversion period between each of the units.

Figure 3 shows an example of procedure of rewriting the DADR register from 000h to 3FFh.

- Before changing 000h (00 0000 0000b)
 First period of rewriting 100h (01 0000 0000b) =>Difference before and after rewriting 100h
 Second period of rewriting 200h (10 0000 0000b) => Difference before and after rewriting 100h
 Third period of rewriting 300h (11 0000 0000b) => Difference before and after rewriting 100h
- Fourth period of rewriting 3FFh (11 1111 1111b) => Difference before and after rewriting 0FFh
- After changing 3FFh (11 1111 1111b)







2.2 Rewriting DACR with AD converter operated

When the value of DACR is changed, rewrite the DACR with the DADR register value set to 000h. If the DACR register

is rewritten under other conditions, the accuracy of the AD converter may not be guaranteed.

