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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU	Document No.	TN-RL*-A012B/E	Rev.	2.00
Title	RL78/G12 Direction of use		Information Category	Technical Notification	
Applicable Product	RL78/G12 R5F102xx R5F103xx	Lot No. All	Reference Document	RL78/G12 User's Manual: Hardware Rev.2.00 R01UH0200EJ0200 (Aug 2013)	

A new direction of use on the products below has been added.

Direction added in Rev. 2.00

Subsection	Description	Applicable Products	Page
1.1	Restriction on LS (low-speed main) mode	20-pin and 24-pin products of the RL78/G12 group. Refer to "1.4 Applicable Products by restriction" for details.	2

Direction previously notified

Subsection	Description	Applicable Products	Page
2.1	Operating Precaution for Data Flash read access	RL78/G12 group products with Data Flash. Refer to "2.4 Target products' name list" for details.	3

Revision history

Revision history of "RL78/G12 Direction of use":

Document No.	Date	Description
TN-RL*-A012A/E	Aug 19, 2013	Rev. 1.00. "2 Restriction notified in Rev. 1.00"
TN-RL*-A012B/E	Apr. 10, 2015	Rev. 2.00. "1 Restriction notified in Rev. 2.00"

1 Direction added in Rev. 2.00

1.1 Restriction on LS (low-speed main) mode

<Use affected by this restriction>

As shown in Table 1.1, this restriction is applied to the cases in which the operating ambient temperature is low, and the flash operation mode and the frequency of the high-speed on-chip oscillator are set to the LS (low-speed main) mode and 3 to 8 MHz, respectively.

Table 1.1 applicable option byte value and operating ambient temperature affected

Option byte setting (Address: 000C2H)			Operating ambient temperature (T_A)	Affected by the restriction
	Flash operation mode	High-speed on-chip oscillator frequency		
AAH	LS (low-speed main) mode	8 MHz	$T_A \leq -20$ °C	Yes
A2H	LS (low-speed main) mode	6 MHz	$T_A \leq -15$ °C	Yes
ABH	LS (low-speed main) mode	4 MHz	$T_A \leq -35$ °C	Yes
A3H	LS (low-speed main) mode	3 MHz	$T_A \leq -30$ °C	Yes
Other				No

<Details of the restriction>

Repetitive resets by either the watchdog timer (WDT), illegal instruction (TRAP) or invalid memory access (IAW) may occur when a reset Note by an illegal instruction execution or the low voltage detection occurs under a condition shown in Table 1.1. This abnormal reset operation is resolved by an external reset input via the $\overline{\text{RESET}}$ pin or an increase of T_A (to temperature not subject to the restriction).

Do not operate an affected product under a condition that may cause the problem.

Note: A reset by the watchdog timer (WDT), illegal instruction (TRAP), invalid memory access (IAW), low voltage detection (LVD) or RAM parity error may cause the abnormal reset operation. A reset by power-on-reset (POR) or a reset input via the $\overline{\text{RESET}}$ pin does not cause the abnormal reset operation.

1.2 Workaround

<Software workaround>

Switch to the HS (high-speed main) mode in case that VDD is 2.4 V or greater.

ELECTRICAL SPECIFICATIONS is HS mode. Please check the User's Manual: Hardware.

1.3 Modification schedule

Revision of products is planned. Only revised products will be shipped after the changes are made. Part numbers of the revised products and the revision schedule will be announced in April, 2015.

1.4 Applicable products

20-pin and 24-pin products of the RL78/G12 group as shown in the following table.

20-pin LSSOP 4.4x6.5mm	R5F10266ASP, R5F10267ASP, R5F10268ASP, R5F10269ASP, R5F1026AASP R5F10366ASP, R5F10367ASP, R5F10368ASP, R5F10369ASP, R5F1036AASP R5F10266DSP, R5F10267DSP, R5F10268DSP, R5F10269DSP, R5F1026ADSP R5F10366DSP, R5F10367DSP, R5F10368DSP, R5F10369DSP, R5F1036ADSP R5F10266GSP, R5F10267GSP, R5F10268GSP, R5F10269GSP, R5F1026AGSP
24-pin HWQFN 4x4mm	R5F10277ANA, R5F10278ANA, R5F10279ANA, R5F1027AANA R5F10377ANA, R5F10378ANA, R5F10379ANA, R5F1037AANA R5F10277DNA, R5F10278DNA, R5F10279DNA, R5F1027ADNA R5F10377DNA, R5F10378DNA, R5F10379DNA, R5F1037ADNA R5F10277GNA, R5F10278GNA, R5F10279GNA, R5F1027AGNA

2 Direction notified in Rev. 1.00

2.1 Operating Precaution for Data Flash read access

Applicable Usage:

The usage which meets to all of (1), (2), and (3) is applicable to the restriction.

(1) Using both DMA and Data Flash.

(2) DMA is operating when Data Flash read occurs.

(3) Data Flash is read using flash-related libraries Renesas Electronics is offering, which are listed below.
Otherwise instead of using those libraries, the combination of CPU Related instructions Note1 are used for reading related memory Note2 and Data Flash.

- The FDL (Data Flash library) Type01 V1.11 or earlier version.
- The FDL Type02 V1.00 or earlier version.
- The FDL Type04 V1.04 or earlier version.

Note1. See 2.5. about the combination of the related instructions1 and 2.

Note2. Related memory is RAM (Include general purpose register area), SFR, 2nd SFR, ES, CS, PSW, SP

Detail of Restriction:

In the case that DMA transfer is operated and it is immediately followed by read access to the target memory (Related instructions 1) which access is also immediately followed in sequence, by read access to Data Flash (Related instructions 2), because of the conflict on the internal bus between read access to the target memory and to the Data Flash, the read out result from the target memory may be wrongly changed.

Example for an instruction sequence causing this issue:

```
    DMA transfer trigger
    DMA transer
MOVW    HL,!addr16      ; read data from RAM (Related instruction 1)
MOV     A,[DE]          ; read data from Data Flash (Related instructions 2)
```

When DMA transfer occurs as mentioned above timing, a wrong data is loaded into HL register.

2.2 Workaround

If you have any possibility that read access to the Data Flash and the DMA transfer could operate in the same time, please apply the following procedures according to the way to read out the Data Flash.

Case 1:

Data Flash Read access via the 'Data Flash Access Library' (FDL). This library is developed under the responsibility of Renesas.

Workaround for Case 1:

There are currently three type of FDL supported and all of them will be updated to cover the aforementioned workaround.

Library version (Not installer version)

FDL (Type01) version V1.12 Note or later

FDL (Type02) version V1.01 Note or later

FDL (Type04) version V1.05 Note or later

Case 2:

Data Flash Read access directly executed in the user software without library.

Workaround for Case 2:

Please apply either of the following procedures.

(A) Holding DMA or forcing termination DMA

In case, the user software has to perform a direct Data Flash Read access without using the FDL read command, any possible DMA transfer must be stopped before the Data Flash read access is executed. To stop any DMA transfer, please follow the procedure given in the User Manual.
Furthermore, please make sure to wait at least 3 clocks (f_{CLK}) after setting DWAITn bit to "1" before the Data Flash read instruction is executed. Restart any DMA transfer (by clearing DWAITn bit to "0") after the Data Flash read access have been finished.

(B) Reading Data Flash by using library

When access Data Flash, please use latest Data Flash library of case 1.

(C) Inserting a NOP instruction

Such kind of conflict can be avoided by inserting a NOP instruction immediately prior to any Data Flash Read access.

Example to avoid this issue: operand

```
MOVW   HL, !addr16      ; Read data from RAM
NOP                     ; Insert a NOP prior to the DF read access
MOV    A, [DE]          ; Read data from Data Flash
```

In case the application software will use the DMA feature, Renesas strongly recommend not to perform a direct Data Flash Read access in the user software, because in case of a high level language (e.g. C-Language) it cannot be avoided that the C-compiler may generate a code sequence as described before. Therefore, Renesas strongly recommend to perform the Data Flash Read access ONLY via the corresponding FDL read command.

Note. The modified version of FDL (Data Flash library) will be released in sequence after July 2013.
Remark. f_{CLK}: CPU/peripheral hardware clock frequency

2.3 Modification schedule

This matter is added to “Procedure for accessing data flash memory” of CHAPTER 24 FLASH MEMORY in the user’s manual by the next revision.

2.4 Target products’ name list

RL78/G12 with Data Flash (R5F102)

20-pin LSSOP 4.4x6.5mm	R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP
24-pin HWQFN 4x4mm	R5F1027AANA, R5F10279ANA, R5F10278ANA, R5F10277ANA R5F1027ADNA, R5F10279DNA, R5F10278DNA, R5F10277DNA R5F1027AGNA, R5F10279GNA, R5F10278GNA, R5F10277GNA
30-pin LSSOP 7.62mm(300)	R5F102AAASP, R5F102A9ASP, R5F102A8ASP, R5F102A7ASP R5F102AADSP, R5F102A9DSP, R5F102A8DSP, R5F102A7DSP R5F102AAGSP, R5F102A9GSP, R5F102A8GSP, R5F102A7GSP

2.5 Related instructions list

In case that the Data Flash is read out by "Related instructions 2" immediately after the target memory is read out by "Related instructions 1", this is within the restriction; however, particular combinations of related instructions shown in 2.6. are excepted.

Related instructions 1: Read instructions of RAM(Include general purpose register area), SFR,2nd SFR,ES,CS, PSW,SP

Note: Read instructions of 2nd SFR with wait, mirror area and Data Flash is not related

	Operand
MOV	A, saddr
	A, sfr
	A, !addr16
	A, PSW
	A, ES
	A, CS
	A, [DE]
	A, [DE+byte]
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
	A, word[B]
	A, word[C]
	A, word[BC]
	A, [SP+byte]
MOVW	AX, saddrp
	AX, sfrp
	AX, !addr16
	AX, [DE]
	AX, [DE+byte]
	AX, [HL]
	AX, [HL+byte]
	AX, word[B]
	AX, word[C]
	AX, word[BC]
	AX, [SP+byte]
ADD	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]

	Operand
ADDC	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
SUB	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
SUBC	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
AND	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
OR	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]

	Operand
XOR	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
CMP	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
ADDW	AX, saddrp
	AX, !addr16
	AX, [HL+byte]
SUBW	AX, saddrp
	AX, !addr16
	AX, [HL+byte]
CMPW	AX, saddrp
	AX, !addr16
	AX, [HL+byte]
MOVW	AX, SP

	Operand
MOV	ES, saddr
	B, saddr
	B, !addr16
	C, saddr
	C, !addr16
	X, saddr
	X, !addr16
MOVW	BC, saddrp
	BC, !addr16
	DE, saddrp
	DE, !addr16
	HL, saddrp
	HL, !addr16
	BC, SP
	DE, SP
	HL, SP
CMP	saddr, #byte
	!addr16, #byte
CMP0	saddr
	!addr16
CMPS	X, [HL+byte]

	Operand
MOV1	CY, saddr.bit
	CY, sfr.bit
	CY, PSW.bit
	CY, [HL].bit
AND1	CY, saddr.bit
	CY, sfr.bit
	CY, PSW.bit
	CY, [HL].bit
OR1	CY, saddr.bit
	CY, sfr.bit
	CY, PSW.bit
	CY, [HL].bit
XOR1	CY, saddr.bit
	CY, sfr.bit
	CY, PSW.bit
	CY, [HL].bit
POP	rp

Related instructions 2: Read instructions of Data Flash

	Operand
MOV	A, !addr16
	A, [DE]
	A, [DE+byte]
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
	A, word[B]
	A, word[C]
	A, word[BC]

	Operand
ADD	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
ADDC	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
SUB	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
SUBC	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]

	Operand
AND	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
OR	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
XOR	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
CMP	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]

	Operand
MOV	B, !addr16
	C, !addr16
	X, !addr16
CMP	!addr16, #byte
CMP0	!addr16
CMPS	X, [HL+byte]

2.6 Safe combinations of related instructions

Safe combinations of related instructions1 and 2 <1>

Related instruction 1		Related instruction 2	
	Operand		**Operand**
MOVW	DE, saddrp	MOV	A, [DE]
	DE, !addr16		A, [DE+byte]
	DE, SP		
POP	DE		

Safe combinations of related instructions1 and 2 <2>

Related instruction 1		Related instruction 2					
	Operand		**Operand**		**Operand**		**Operand**
MOVW	HL, saddrp	MOV	A, [HL]	ADD	A, [HL]	AND	A, [HL]
	HL, !addr16		A, [HL+byte]		A, [HL+byte]		A, [HL+byte]
	HL, SP		A, [HL+B]		A, [HL+B]		A, [HL+B]
POP	HL		A, [HL+C]		A, [HL+C]		A, [HL+C]
				ADDC	A, [HL]	OR	A, [HL]
			Operand		A, [HL+byte]		A, [HL+byte]
		CMPS	X, [HL+byte]		A, [HL+B]		A, [HL+B]
					A, [HL+C]		A, [HL+C]
				SUB	A, [HL]	XOR	A, [HL]
					A, [HL+byte]		A, [HL+byte]
					A, [HL+B]		A, [HL+B]
					A, [HL+C]		A, [HL+C]
				SUBC	A, [HL]	CMP	A, [HL]
					A, [HL+byte]		A, [HL+byte]
					A, [HL+B]		A, [HL+B]
					A, [HL+C]		A, [HL+C]

Safe combinations of related instructions1 and 2 <3>

Related instruction 1		Related instruction 2					
	Operand		**Operand**		**Operand**		**Operand**
MOV	B, saddr	MOV	A, [HL+B]	ADD	A, [HL+B]	AND	A, [HL+B]
	B, !addr16		A, word[B]	ADDC	A, [HL+B]	OR	A, [HL+B]
MOVW	BC, saddrp			SUB	A, [HL+B]	XOR	A, [HL+B]
	BC, !addr16			SUBC	A, [HL+B]	CMP	A, [HL+B]
	BC, SP						
POP	BC						

Safe combinations of related instructions1 and 2 <4>

Related instruction 1		Related instruction 2					
	Operand		**Operand**		**Operand**		**Operand**
MOV	C, saddr	MOV	A, [HL+C]	ADD	A, [HL+C]	AND	A, [HL+C]
	C, !addr16		A, word[C]	ADDC	A, [HL+C]	OR	A, [HL+C]
MOVW	BC, saddrp			SUB	A, [HL+C]	XOR	A, [HL+C]
	BC, !addr16			SUBC	A, [HL+C]	CMP	A, [HL+C]
	BC, SP						
POP	BC						

Safe combinations of related instructions1 and 2 <5>

Related instruction 1		Related instruction 2	
	Operand		**Operand**
MOV	B, saddr	MOV	A, word[BC]
	B, !addr16		
	C, saddr		
	C, !addr16		
MOVW	BC, saddrp		
	BC, !addr16		
	BC, SP		
POP	BC		