Date: Jan. 16, 2019

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	System LSI		Document No.	TN-RIN-A028A/E	Rev.	1.00
Title	Revision of Documents Associated with R-IN32M4 Series User's Manual		Information Category	Technical Notification		
Applicable Product	R-IN32M4-CL2 Series (See below for details)	Lot No. All lots	Reference Document	R-IN32M4-CL2 Series Documents (See below for details)		

This is to report revisions of the R-IN32M4-CL2 Series documents listed in the "Reference Documents" below.

Please use the products covered in this report in consideration with the revised contents.

The item marked with "♦" is strongly related to device specifications and constraints.

1. Applicable Products

Product Type	Model Marking	Product Code
R-IN32M4-CL2	R9J03G019GBG	R9J03G019GBG

2. Reference Documents

Doc. No. in this TU	Document Title	Renesas Document Number	Previous Edition	Revised Edition
1	R-IN32M4-CL2 User's Manual	R18UZ0033EJ****	V1.02	V2.00
2	R-IN32M4-CL2 User's Manual: Peripheral Modules	R18UZ0035EJ****	V2.00	V3.00
3	R-IN32M4-CL2 User's Manual: Board design edition	R18UZ0046EJ****	V1.00	V2.00
4	R-IN32M4-CL2 Programming Manual: Driver	R18UZ0038EJ****	V2.01	V3.00
5	R-IN32 Series User's Manual (CC-Link Remote device station)	R18UZ0056EJ****	V1.01	V1.02

3. Revision Contents

Doc. No. in this TU	Item No.	Revisions (Section Number)	Previous Edition's Page Number	Revision Type
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1	1-2	1.5 Base Addresses of the System Registers Area	-	Complement
1	1-3	2.1.11 CC-Link Pins (intelligent device station)	25	Error correction
1	1-4	3. Memory Maps: Figure 3.1	50	Error correction
1	1-5	3. Memory Maps: Figure 3.1 and Figure 3.5	50, 53	Note addition
1	1-6	3. Memory Maps: Figure 3.5	53	Error correction
1	1-7	7.2 Port Configuration	65	Expression alignment
1	1-8	7.2 Port Configuration	65	Note alignment
1	1-9	8.8.4 External MCU Interface Pins ♦ (1) Synchronous mode	131	Error correction
1	1-10	8.8.4 External MCU Interface Pins ♦ (4) Synchronous SRAM type transfer mode	142	Error correction
1	1-11	8.8.4 External MCU Interface Pins Figure 8.17, Figure 8.18, Figure 8.19 and Figure 8.20	143, 144	Complement
1	1-12	8.8.5 Serial Flash ROM Interface ♦	145	Error correction
2	2-1	2.3.4 Operations for Reset	2-11	Complement
2	2-2	5.1 Selecting the Boot Mode	5-1	Expression alignment
2	2-3	8.3.4.1 MIIM Register (GMAC_MIIM)	8-9	Expression alignment
2	2-4	8.3.4.5 RX Mode Register (GMAC_RXMODE)	8-12	Error correction
2	2-5	8.3.4.6 TX Mode Register (GMAC_TXMODE)	8-14	Error correction
2	2-6	8.3.4.6 TX Mode Register (GMAC_TXMODE)	8-14	Error correction
2	2-7	8.4.1.2 Flow of Processing for Issuing the Hardware Function Call ♦	8-33	Complement
2	2-8	8.4.1.3 Buffer Allocator	8-33	Error correction
2	2-9	8.4.1.3 Buffer Allocator	8-36	Error correction
2	2-10	8.4.1.3 Buffer Allocator	8-37	Error correction
2	2-11	8.4.1.4 MAC DMA Controller	8-44	Error correction
2	2-12	8.4.1.4 MAC DMA Controller	8-45	Error correction
2	2-13	8.4.1.4 MAC DMA Controller	8-50	Error correction
2	2-14	8.4.1.4 MAC DMA Controller	8-50	Complement
2	2-15	8.4.1.5 Buffer RAM DMA Controller	8-52	Error correction

Doc. No. in this TU	Item No.	Revisions (Section Number)	Previous Edition's Page Number	Revision Type
2	2-16	8.4.1.5 Buffer RAM DMA Controller	8 -52	Error correction
2	2-17	8.4.2 Interrupts	8-56	Error correction
2	2-18	8.4.2 Interrupts	8-58	Complement
2	2-19	8.5 Notes	-	Note addition
2	2-20	9.3.1 List of Registers, (5) Timer Module Registers	9-4	Error correction
2	2-21	9.3.1 List of Registers, (6) DLR Module Registers	9-5	Error correction
2	2-22	10.7 Memory Access Timing Examples	10-20	Error correction
2	2-23	10.7 Memory Access Timing Examples	10-17 to 10-24	Expression alignment
2	2-24	12.1 Memory Map	12-3	Note addition
2	2-25	12.1 Memory Map	12-3	Error correction
2	2-26	12.2.5 Control Registers (2) HOSTIF bus control register (HIFBCC)	12-17, 12-18	Error correction
2	2-27	12.2.5 Control Registers (2) HOSTIF bus control register (HIFBCC)	12-18	Note addition
2	2-28	12.2.5 Control Registers (4) HOSTIF page ROM control register (HIFPRC)	12-20	Error correction
2	2-29	14.1.1 Overview	14-2	Expression alignment
2	2-30	14.4.6 DMA Trigger Source Registers (DTFRn, RTDTFR)	14-86	Note addition
2	2-31	14.6 Interrupt Output	14-91	Expression alignment
2	2-32	20.4.2 Master/Slave Connections	20-38, 20-39	Expression alignment
2	2-33	21.3 (6) IICBn high-level width setting register (IICBnWH)	21-14	Error correction
2	2-34	21.6.1 Single Transfer Mode (3) Example of communications in single transfer mode (slave reception)	21-42	Error correction
2	2-35	25.7 System Protect Command Register (SYSPCMD)	25-7	Complement
2	2-36	25.11.1 Noise Filter Configuration Registers (NFC0 to NFC4)	25-18	Error correction
2	2-37	25.11.2 Noise Filter Operation	25-23	Error correction
2	2-38	26. Debugging	26-1	Expression alignment
3	3-1	7. Guide to Thermal Design	22	Expression alignment
3	3-2	7.3 Notes	-	Newly added
3	3-3	15. CSIH Pins	-	Newly added
3	3-4	24. Countermeasure for Noise	-	Newly added
4	4-1	3.2.1 Memory Maps	12, 15	Note addition
4	4-2	3.2.1 Memory Maps	12	Error correction
4	4-3	3.2.1 Memory Maps	15	Error correction
4	4-4	6.4.1 Initialization of IIC Controller ♦	34	Error correction
4	4-5	6.5.5 Confirmation of Received Data (for Slave)	45	Error correction
5	5-1	3. Specified Parts and Recommended Parts	4	Complement
5	5-2	5. CC-Link Remote Device Station Pins	6, 8	Complement
5	5-3	6.1 Setting the Number of Occupied Stations	9	Complement
5	5-4	14.1 Circuit Design in General, (3) Questions and Answers Related to Switches, Connectors, and Terminal Blocks	72	Complement

No.1-1 1.2 Functional Overview, 2. Pin Functions and 6. CC-Link IE Field [1/2]

A feature "remote device station" was added to CC-Link IE Field and the notation of the feature "intelligent device station" alone was deleted.

<table>
<tr><th colspan="2">V1.02</th><th colspan="2">V2.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>3</td><td>[Table 1.1 Overview of R-IN32M4-CL2 (2/2)]

<table><tr><th>Product / Item</th><th>R-IN32M4-CL2</th></tr><tr><td>CC-Link IE</td><td>CC-Link IE Field (intelligent device station)</td></tr></table></td><td>3</td><td>[Table 1.1 Overview of R-IN32M4-CL2 (2/2)]

<table><tr><th>Product / Item</th><th>R-IN32M4-CL2</th></tr><tr><td>CC-Link IE</td><td>CC-Link IE Field (intelligent device station and remote device station)</td></tr></table></td></tr>
<tr><td>24</td><td>[2.1 List of Pins]

2.1.10 CC-Link IE Field Pins (Intelligent Device Station)</td><td>24</td><td>[2.1 List of Pins]

2.1.10 CC-Link IE Field Pins</td></tr>
<tr><td>27</td><td>[2.1.14 Trace Pins]

Note: This pin function is multiplexed with a pin function of the CC-Link IE Field.
For information on the multiplexed functions of the port pins, see section 2.1.10, CC-Link IE Field Pins (Intelligent Device Station).
The initial setting is for input and the pin is switched from input to output in 20 BUSCLK cycles after the RSTOUTZ pin has been de-asserted in response to release from the reset state.</td><td>27</td><td>[2.1.14 Trace Pins]

Note: This pin function is multiplexed with a pin function of the CC-Link IE Field.
For information on the multiplexed functions of the port pins, see section 2.1.10, CC-Link IE Field Pins.
The initial setting is for input and the pin is switched from input to output in 20 BUSCLK cycles after the RSTOUTZ pin has been de-asserted in response to release from the reset state.</td></tr>
<tr><td>47</td><td>[2.5 Buffer Type of Pins and Handling of Unused Pins]

2.5.5 CC-Link IE Field (Intelligent Device Station) Pin</td><td>47</td><td>[2.5 Buffer Type of Pins and Handling of Unused Pins]

2.5.5 CC-Link IE Field Pin</td></tr>
<tr><td>61</td><td>[6. CC-Link IE Field (Intelligent Device Station)]

6. CC-Link IE Field (Intelligent Device Station)

[6. CC-Link IE Field (Intelligent Device Station)]

6.1 CC-Link IE Field (Intelligent Device Station) Control Registers

[Table 6.2 Overview of the Bus Control Registers]

<table><tr><th>Register Name</th><th>Symbol</th><th>Address</th></tr><tr><td>CC-Link IE Field (intelligent device station) bus size control register</td><td>CIEBSC</td><td>400A 4004H</td></tr><tr><td>CC-Link IE Field (intelligent device station) bus bridge control register</td><td>CIESMC</td><td>400A 4008H</td></tr><tr><td>CC-Link IE Field (intelligent device station) clock gate register</td><td>CIECLKGTD</td><td>BASE + 0938H</td></tr></table></td><td>61</td><td>[6 CC-Link IE Field]

6 CC-Link IE Field

[6 CC-Link IE Field]
6.1 CC-Link IE Field Control Registers

[Table 6.2 Overview of the Bus Control Registers]

<table><tr><th>Register Name</th><th>Symbol</th><th>Address</th></tr><tr><td>CC-Link IE Field bus size control register</td><td>CIEBSC</td><td>400A 4004H</td></tr><tr><td>CC-Link IE Field bus bridge control register</td><td>CIESMC</td><td>400A 4008H</td></tr><tr><td>CC-Link IE Field clock gate register</td><td>CIECLKGTD</td><td>BASE + 0938H</td></tr></table></td></tr>
</table>

No.1-1 1.2 Functional Overview, 2. Pin Functions and 6. CC-Link IE Field [2/2]

A feature "remote device station" was added to CC-Link IE Field and the notation of the feature "intelligent device station" alone was deleted.

V1.02		V2.00	
Page	Description	Page	Revised Description
62	**[6. CC-Link IE Field (Intelligent Device Station)]** 6.1.1 CC-Link IE Field (Intelligent Device Station) Bus Size Control Register (CIEBSC) The CIEBSC register is for setting the data bus width for access to the CC-Link IE Field (intelligent device station). When using the CC-Link IE Field (intelligent device station), set the bits of this register to 0000 FFFFH.	62	**[6 CC-Link IE Field]** 6.1.1 CC-Link IE Field Bus Size Control Register (CIEBSC) The CIEBSC register is for setting the data bus width for access to the CC-Link IE Field. When using the CC-Link IE Field, set the bits of this register to 0000 FFFFH.
	[6. CC-Link IE Field (Intelligent Device Station)] 6.1.2 CC-Link IE Field (Intelligent Device Station) Bus Bridge Control Register (CIESMC) The CIESMC register is used for access control. When using the CC-Link IE Field (intelligent device station), be sure to set the bits of this register to 0000 0050H.		**[6 CC-Link IE Field]** 6.1.2 CC-Link IE Field Bus Bridge Control Register (CIESMC) The CIESMC register is used for access control. When using the CC-Link IE Field, be sure to set the bits of this register to 0000 0050H.
63	**[6. CC-Link IE Field (Intelligent Device Station)]** 6.1.3 CC-Link IE Field (Intelligent Device Station) Clock Gate Register (CIECLKGTD)	63	**[6 CC-Link IE Field]** 6.1.3 CC-Link IE Field Clock Gate Register (CIECLKGTD)

No.1-2 1.5 Base Addresses of the System Registers Area

The description on the base addresses of the system registers area was added.

V1.02		V2.00	
Page	Description	Page	Revised Description
-	**[1.5 Base Addresses of the System Registers Area]** N/A	6	**[1.5 Base Addresses of the System Registers Area** The addresses of registers given in the subsequent sections are relative to the base addresses. In access to the registers via the external MCU interface, the base address is D_0000H. In access by the internal CPU or DMA controller, the base address is 4001_0000H. • In access by the CPU or DMA controller BASE = 4001_0000H • In access via the external microcontroller interface BASE = D_0000H

No.1-3 2.1.11 CC-Link Pins (Intelligent Device Station)

Functional description for the CC-Link (intelligent device station) pins were modified.

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[2.1.11 CC-Link Pins (Intelligent Device Station)]

Function Name	Pin Name	I/O	Description	Active	Level during Reset
CCM_LINKERRZ	P20	O	Link error LED control output	Low	Hi-Z (high)
CCM_ERRZ	P21	O	Error LED control output		
CCM_RUNZ	P26	O	RUN LED control output		
CCM_MDIN0-CCM_MDIN3	P62-P65	I	Transfer rate and mode setting switch input	-	
CCM_SNIN0-CCM_SNIN7	P70-P77	I	Station no. setting switch input		
CCM_LNKRUNZ	P32	O	Link Run LED control output	Low	
CCM_RDLEDZ	P33	O	Receive data LED control output		
CCM_SDLEDZ	RP00	O	Transmit data LED control output		
CCM_IRLZ	P43	O	Interrupt output port		
CCM_WDTENZ	P12	I	Watchdog timer error input		
CCM_MSTZ	P66	O	Operation check LED		
CCM_SMSTZ	RP01	O	Standby master LED control output		
CCM_RD	P54	I	Communications circuit data reception pin	-	
CCM_SD	P56	O	Communications circuit data transmission pin		
CCM_SDGCZ	P57	O	Communications circuit transmit data & gate control pin	Low	
CCM_STMON3	EXTP7	O	Status output	-	
CCM_CLK80M	-	I	CC-Link clock input (80 MHz)		-

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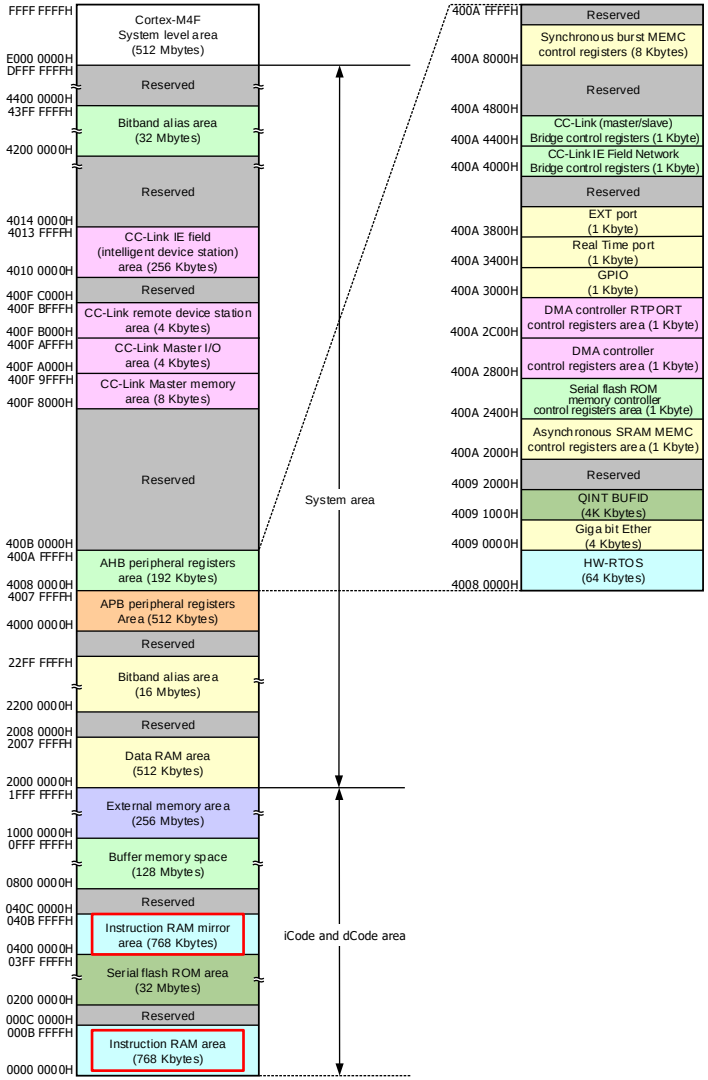
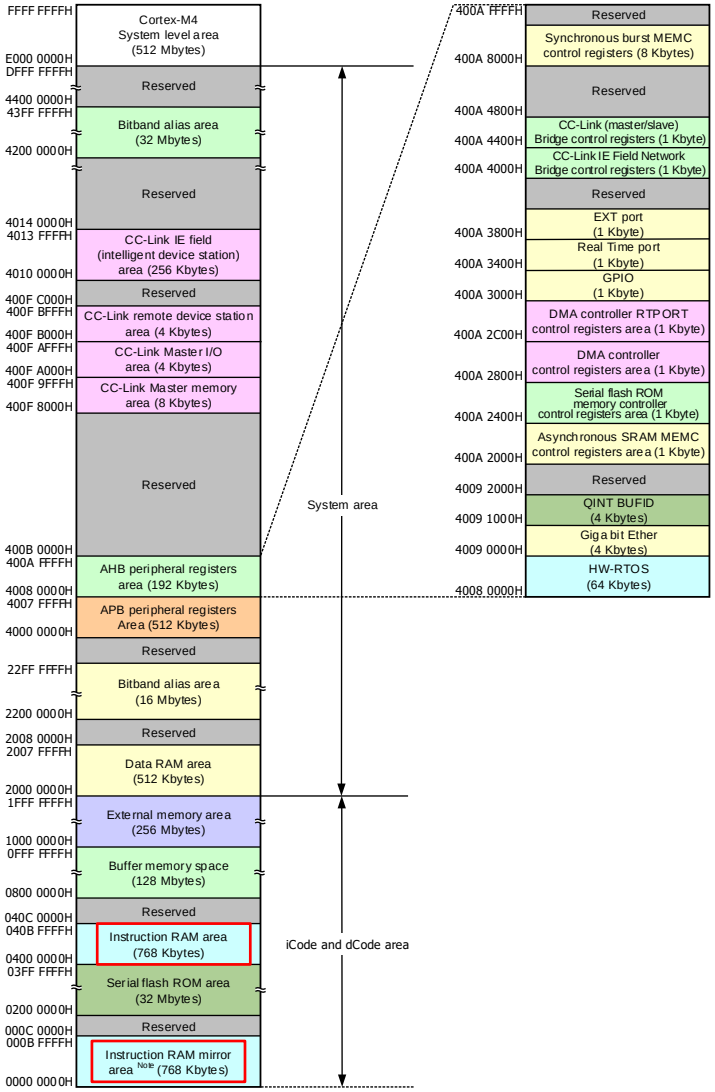
[2.1.11 CC-Link Pins (Intelligent Device Station)]

Function Name	Pin Name	I/O	Description	Active	Level during Reset
CCM_LINKERRZ	P20	O	Link error LED control output	Low	Hi-Z (high)
CCM_ERRZ	P21	O	Not used		
CCM_RUNZ	P26	O	RUN LED control output		
CCM_MDIN0-CCM_MDIN3	P62-P65	I	Transfer rate setting input	-	
CCM_SNIN0-CCM_SNIN7	P70-P77	I	Station no. setting switch input		
CCM_LNKRUNZ	P32	O	Link Run LED control output	Low	
CCM_RDLEDZ	P33	O	Receive data LED control output		
CCM_SDLEDZ	RP00	O	Transmit data LED control output		
CCM_IRLZ	P43	O	Interrupt signal output from communications circuit		
CCM_WDTENZ	P12	I	Watchdog timer error input		
CCM_MSTZ	P66	O	Not used		
CCM_SMSTZ	RP01	O	Not used		
CCM_RD	P54	I	Communications circuit data reception pin	-	
CCM_SD	P56	O	Communications circuit data transmission pin		
CCM_SDGCZ	P57	O	Communications circuit transmit data & gate control pin	Low	
CCM_STMON3	EXTP7	O	Status output	-	
CCM_CLK80M	-	I	CC-Link clock input (80 MHz)		-

No.1-4 3. Memory Maps

Locations of instruction RAM area and instruction RAM mirror area were corrected.

<table>
<tr><th colspan="2">V1.02</th><th colspan="2">V2.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>50</td><td>[Figure 3.1 Entire Memory Map]
 
</td><td>51</td><td>[Figure 3.1 Entire Memory Map]
 
</td></tr>
</table>

No.1-5 3. Memory Maps

Note regarding instruction RAM mirror area was added.

<table>
<tr><th colspan="2">V1.02</th><th colspan="2">V2.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>50</td><td>[Figure 3.1 Entire Memory Map]

N/A</td><td>51</td><td>[Figure 3.1 Entire Memory Map]

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.</td></tr>
<tr><td>53</td><td>[Figure 3.5 External MCU Interface Space]

Note. The upper 52 Kbytes of the AHB peripheral registers area covers the range from the GPIO area to the synchronous burst memory controller control registers. For details, see Figure 3.1 Entire Memory Map.</td><td>54</td><td>[Figure 3.5 External MCU Interface Space]

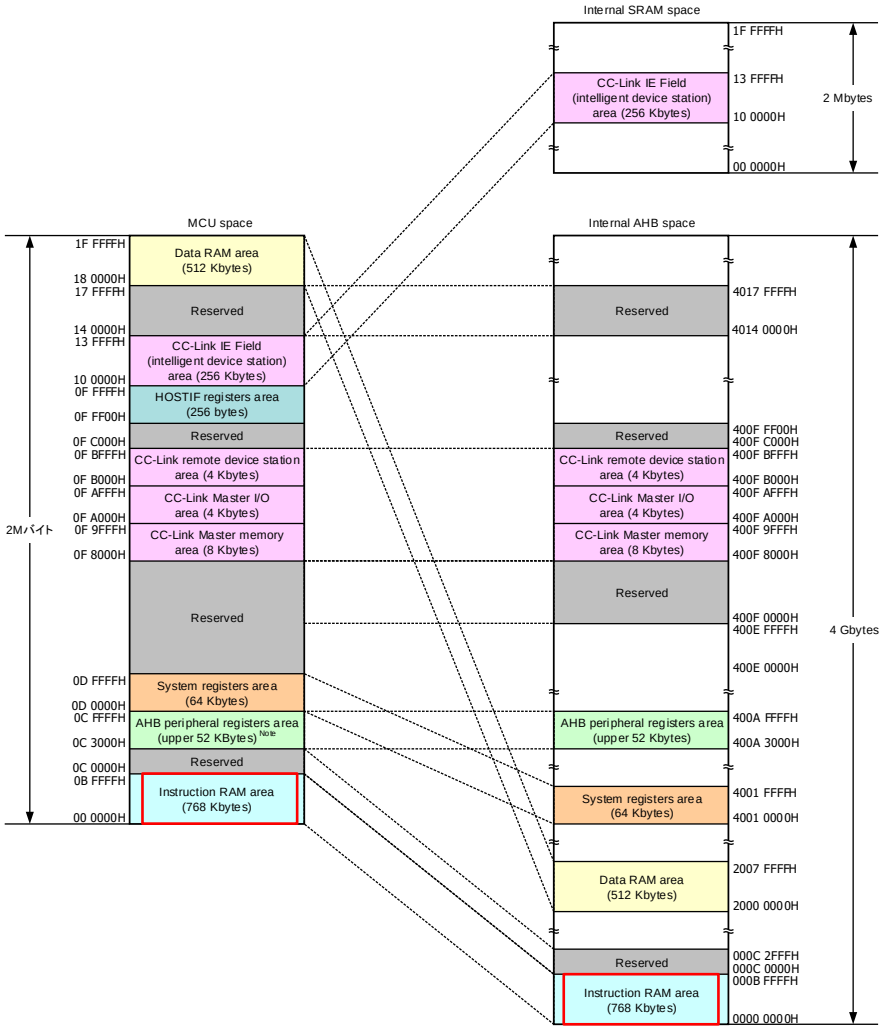
Notes 1. The upper 52 Kbytes of the AHB peripheral registers area covers the range from the GPIO area to the synchronous burst memory controller control registers. For details, see Figure 3.1, Entire Memory Map.
2. The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory Map in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.

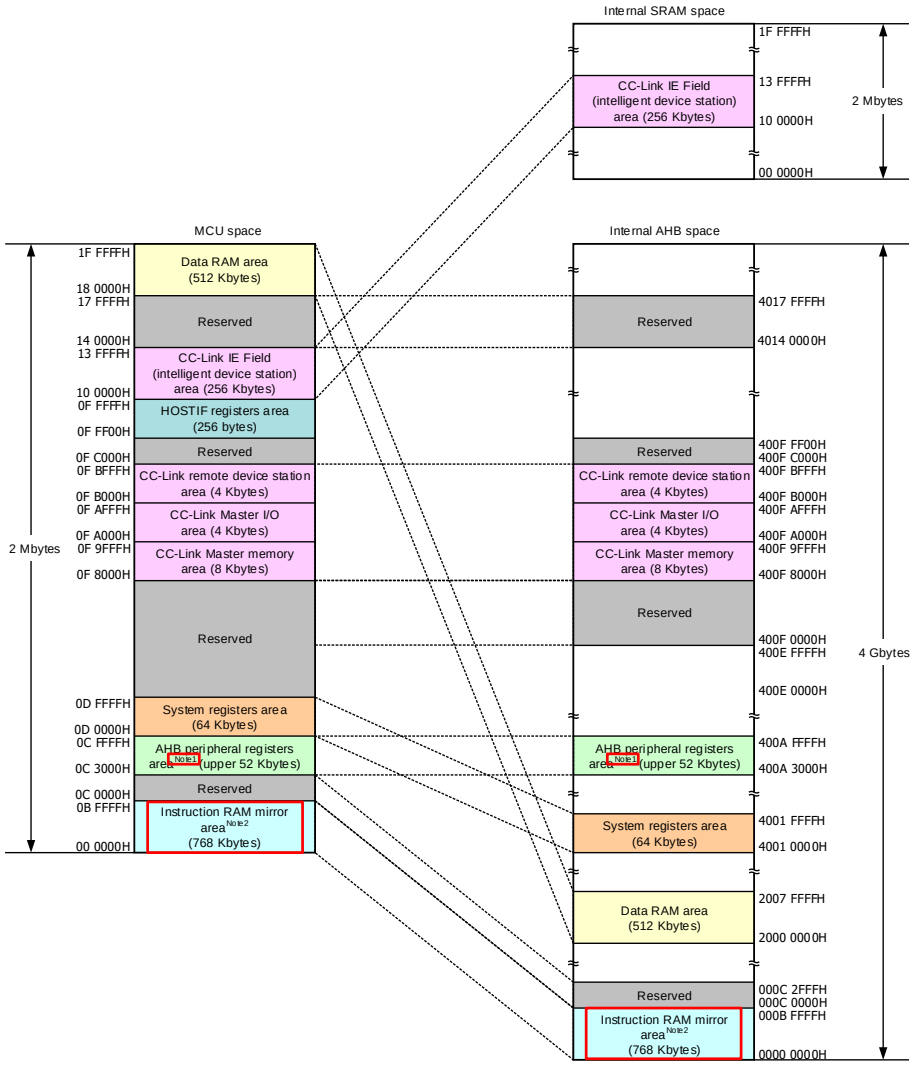
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr>
</table>
</td></tr>
</table>

No.1-6 3. Memory Maps

Locations of Instruction RAM area and instruction RAM mirror area were corrected. A note regarding instruction RAM mirror area was added.

V1.02		V2.00	
Page	Description	Page	Revised Description
53	**[Figure 3.5 External MCU Interface Space]**	54	**[Figure 3.5 External MCU Interface Space]**





No.1-7 7.2 Port Configuration

"Application and Operation" for the port function control registers and the port function control expansion registers was modified.

<table>
<tr><th colspan="2">V1.02</th><th colspan="2">V2.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>65</td><td>[7.2 Port Configuration]
<table>
<tr><th rowspan="2">Register Name</th><th colspan="2">Application and Operation</th></tr>
<tr><th>Read</th><th>Write</th></tr>
<tr><td>Port function control registers (PFCn, RPFCm, EXTPFCp)</td><td>If more than two pin functions are multiplexed on port pins, the corresponding register is used to read which functions are selected.</td><td>If more than two pin functions are multiplexed on port pins, the corresponding register is used to select which functions are to be used.</td></tr>
<tr><td>Port function control expansion registers (PFCEn, RPFCEm, EXTPFCEp)</td><td>If more than three pin functions are multiplexed on port pins, the corresponding register is used to read which functions are selected.</td><td>If more than three pin functions are multiplexed on port pins, the corresponding register is used to select which functions are to be used in combination with the PFCn register.</td></tr>
</table></td><td>66</td><td>[7.2 Port Configuration]
<table>
<tr><th rowspan="2">Register Name</th><th colspan="2">Application and Operation</th></tr>
<tr><th>Read</th><th>Write</th></tr>
<tr><td>Port function control registers (PFCn, RPFCm, EXTPFCp)</td><td rowspan="2">Used to read which function is selected for the multiplexed pin.</td><td rowspan="2">Used to select the function of the multiplexed pin.</td></tr>
<tr><td>Port function control expansion registers (PFCEn, RPFCEm, EXTPFCEp)</td></tr>
</table></td></tr>
</table>

No.1-8 7.2 Port Configuration

Maximum value for HWAITZ valid data output delay time (tDKHWTV) was modified.

V1.02		V2.00	
Page	Description	Page	Revised Description
65	**[7.2 Port Configuration]** **Cautions 1. If a port pin having multiple multiplexed functions which include an external interrupt input is set to control mode by using the PMCn or RPMCm register, and the multiplexed function is an input, the external interrupt input is also multiplexed.** **2. Operation is not guaranteed if the setting has been made not to allocate a multiplexed pin. For example, if multiplexed functions 2 and 4 are not allocated in the same way as the P14 pin, operation does not proceed correctly even if the bits of the PFC and PFCE registers for the given function are set to 1.** **For the allocation of multiplexed pins, see section 7.4, List of Selectable Multiplexed Functions.**	66	**[7.2 Port Configuration]** **Caution: Operation is not guaranteed if an unsupported function is allocated to the multiplexed pin. For example, if multiplexed function 2 is allocated to the P00 pin, which does not support multiplexed function 2, operation does not proceed correctly. For the allocation of multiplexed pins, see section 7.4, List of Selectable Multiplexed Functions.**

No.1-9 8.8.4 External MCU Interface Pins, (1) Synchronous mode

Maximum value for HWAITZ valid data output delay time (tDKHWTV) was modified.

V1.02		V2.00	
Page	Description	Page	Revised Description
131	**[(1) Synchronous mode]** No. | Parameter | Symbol | MIN | MAX | Unit 13 | HWAITZ valid data output delay time (for HBUSCLK↑) | tDKHWTV | 2.0 | 10.0 | ns	133	**[(1) Synchronous mode]** No. | Parameter | Symbol | MIN | MAX | Unit 13 | HWAITZ valid data output delay time (for HBUSCLK↑) | tDKHWTV | 2.0 | 11.0 | ns

No.1-10 8.8.4 External MCU Interface Pins, (4) Synchronous SRAM type transfer mode

Maximum values for HWAITZ output delay time (tDKPHWT and tDKNHWT) were modified.

V1.02		V2.00	
Page	Description	Page	Revised Description
142	**[(4) Synchronous SRAM type transfer mode]** No. | Parameter | Symbol | MIN | MAX | Unit 28 | HWAITZ output delay time (for HBUSCLK↑) | tDKPHWT | 2.0 | 10.0 | ns 29 | HWAITZ output delay time (for HBUSCLK↓) | tDKNHWT | 2.0 | 10.0 | ns	144	**[(4) Synchronous SRAM type transfer mode]** No. | Parameter | Symbol | MIN | MAX | Unit 28 | HWAITZ output delay time (for HBUSCLK↑) | tDKPHWT | 2.0 | 11.0 | ns 29 | HWAITZ output delay time (for HBUSCLK↓) | tDKNHWT | 2.0 | 11.0 | ns

No.1-11 8.8.4 External MCU Interface Pins, (4) Synchronous SRAM type transfer mode

Timing waves were partially modified and remarks were added.

V1.02		V2.00	
Page	Description	Page	Revised Description
—	N/A	145	**[Figure 8.17 External MCU Interface Write Timing (MEMCSEL = H, ADMUXMODE = L)]** A timing wave was added.
—	N/A	146	**[Figure 8.18 External MCU Interface Read Timing (MEMCSEL = H, ADMUXMODE = L)]** A timing wave was added.
143	**[Figure 8.17External MCU Interface Write Timing (MEMCSEL = H, ADMUXMODE = H)]**	147	**[Figure 8.19 External MCU Interface Write Timing (MEMCSEL = H, ADMUXMODE = H)]** The specification which applies when ADMUXMODE = L was removed from the given timing wave. A remark was added stating that the source address depends on data bus width.
144	**[Figure 8.18External MCU Interface Read Timing (MEMCSEL = H, ADMUXMODE = H)]**	148	**[Figure 8.20 External MCU Interface Read Timing (MEMCSEL = H, ADMUXMODE = H)]** The specification which apples when ADMUXMODE = L was removed from the given timing wave. A remark was added stating that the source address depends on data bus width.

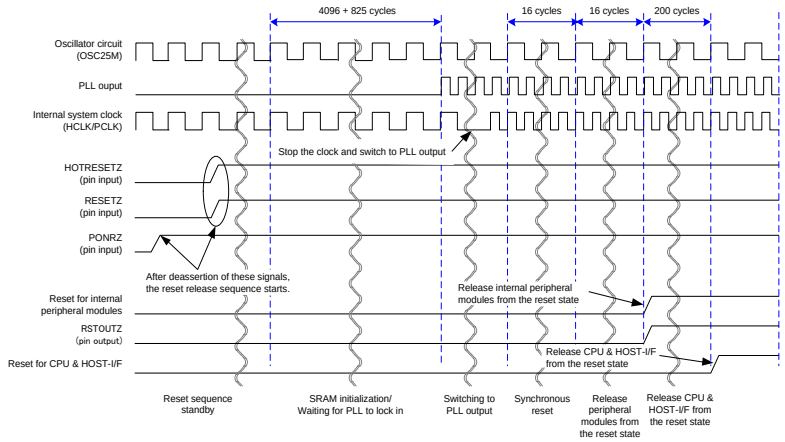
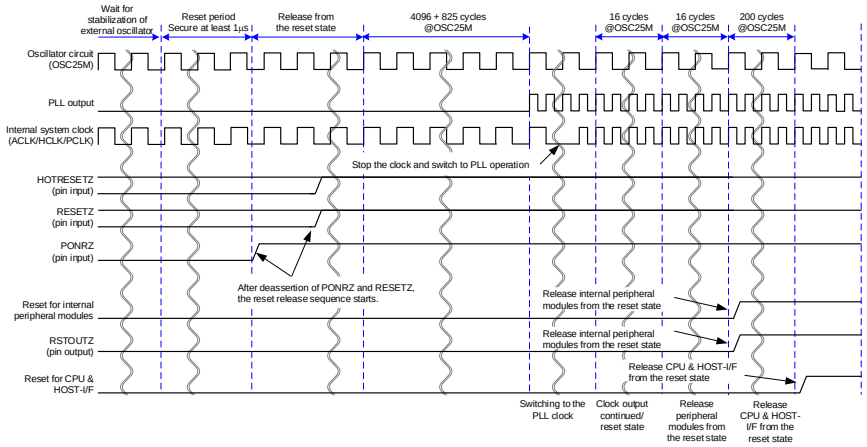
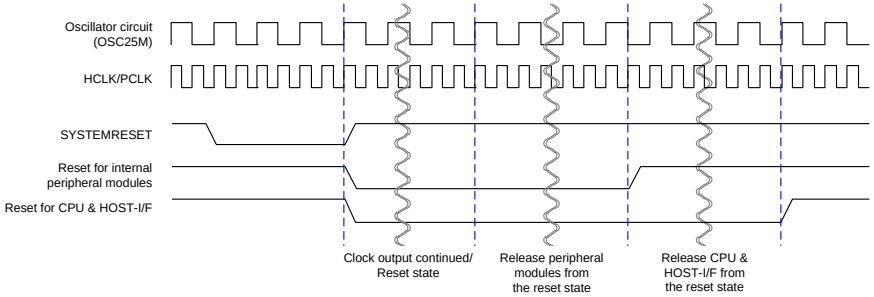
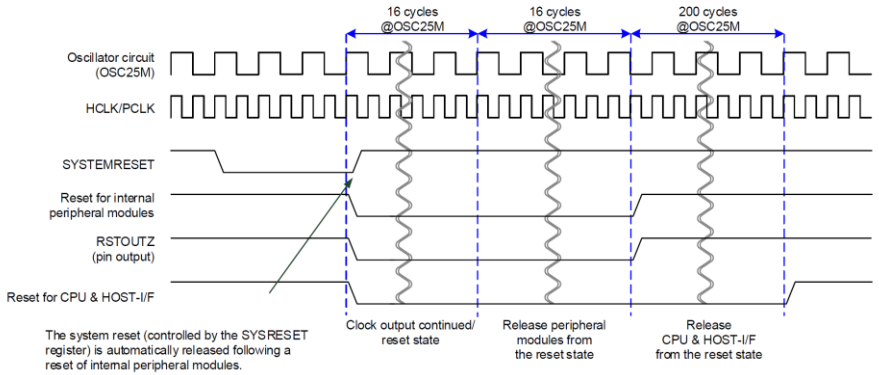
No.1-12 8.8.5 Serial Flash ROM Interface

Specifications of $t_{DSMCSCK}$ and $t_{DSMCKCS}$ were modified.

V1.02		V2.00	
Page	Description	Page	Revised Description
145	**[8.8.5 Serial Flash ROM Interface]** Parameter / Symbol / Conditions / MIN / MAX / Unit Delay time between SMCSZ falling and SMSCK rising / $t_{DSMCSCK}$ / C_L = 15 pF, Freq = 50 MHz / 7.5 Note / - / ns Hold time from SMSCK rising to SMCSZ rising / $t_{DSMCKCS}$ / C_L = 15 pF, Freq = 50 MHz / 11.5 Note / - / ns	149	**[8.8.5 Serial Flash ROM Interface]** Parameter / Symbol / Conditions / MIN / MAX / Unit Delay time between SMCSZ falling and SMSCK rising / $t_{DSMCSCK}$ / C_L = 15 pF, Freq = 50 MHz / 6.0 Note / - / ns Hold time from SMSCK rising to SMCSZ rising / $t_{DSMCKCS}$ / C_L = 15 pF, Freq = 50 MHz / 9.0 Note / - / ns

No.2-1 2.3.4 Operations for Reset

Timing charts were modified.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>2-11</td><td>[Figure 2.3 Timing of Reset at Power On]
 
</td><td>2-11</td><td>[Figure 2.3 Timing of Reset at Power On]
 
</td></tr>
<tr><td></td><td>[Figure 2.4 Timing of Reset at System Reset]
 
</td><td></td><td>[Figure 2.4 Timing of Reset at System Reset]
 
</td></tr>
</table>

No.2-2 5.1 Selecting the Boot Mode

Signal name corrected (STCSZ0 → CSZ0)

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>5-1</td><td>[Table 5.1 Selecting the Boot Mode]

<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Boot Area</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>Memory connected to the STCSZ0 pin of the external bus interface</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Serial flash ROM</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot (debugger used ONLY)</td><td>Instruction RAM</td></tr>
</table>
[(1) External memory boot mode]

The CPU is booted from the external memory connected to the STCSZ0 pin of the external bus interface.</td><td>5-1</td><td>[Table 5.1 Selecting the Boot Mode]

<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Boot Area</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>Memory connected to the CSZ0 pin of the external bus interface</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Serial flash ROM</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot (debugger used ONLY)</td><td>Instruction RAM</td></tr>
</table>
[(1) External memory boot mode]

The CPU is booted from the external memory connected to the CSZ0 pin of the external bus interface.</td></tr>
</table>

No.2-3 8.3.4.1 MIIM Register (GMAC_MIIM)

Caution was modified.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-9</td><td>[8.3.4.1 MIIM Register (GMAC_MIIM)]

Caution: The setting of this register is effective for the management interface selected by the MAC select register (MACSEL). In other cases, writing to this register has no effect and the value read is undefined.</td><td>8-9</td><td>[8.3.4.1 MIIM Register (GMAC_MIIM)]

Caution: The setting of this register is only effective when the general-purpose Ethernet port is selected by the MAC select register (MACSEL). In other cases, writing to this register has no effect and the value read is undefined.</td></tr>
</table>

No.2-4 8.3.4.5 RX Mode Register

(GMAC_RXMODE) Description of the SFRXFIFO bit

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-12</td><td>[8.3.4.5 RX Mode Register (GMAC_RXMODE)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>29</td><td>SFRXFIFO</td><td>Store & Forward For RX FIFO
1: Store & Forward mode
The reception DMA controller does not start to operate until data up to the end of the frame is written in RX FIFO.
0: Cut through mode</td></tr>
</table></td><td>8-12</td><td>[8.3.4.5 RX Mode Register (GMAC_RXMODE)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>29</td><td>SFRXFIFO</td><td>Store & Forward For RX FIFO
1: Store & Forward mode
The reception DMA controller starts to operate after data up to the end of the frame is written to the RX FIFO buffer.
0: Cut through mode
The reception DMA controller starts to operate after the number of words set in the RRTTH2-0 bits is written to the RX FIFO buffer.</td></tr>
</table></td></tr>
</table>

No.2-5 8.3.4.6 TX Mode Register (GMAC_TXMODE)

Description of the SF bit was modified and Caution 2 was added.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-14</td><td>[8.3.4.6 TX Mode Register (GMAC_TXMODE)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>29</td><td>SF</td><td>Store & Forward
1: Transmission starts after the end of a frame is written to the TX FIFO buffer.
If you are using a TCP/IP accelerator, this must be selected.
0: Transmission starts after words of data specified in the FSTTH1-0 bits are written to the TX FIFO buffer.</td></tr>
</table>
Caution: LPTXEN must be set to 1 since the frame size may exceed the maximum size of 1518 bytes while management tag insertion of the Ethernet switch is enabled (the SWTAGEN bit in the ETHSWMTC register is 1).</td><td>8-14</td><td>[8.3.4.6 TX Mode Register (GMAC_TXMODE)]

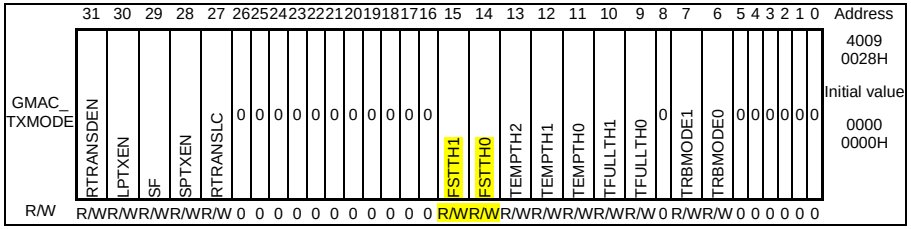
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>29</td><td>SF</td><td>Store & Forward
1: Transmission starts after the end of a frame is written to the TX FIFO buffer.
If you are using a TCP/IP accelerator, this must be selected.
0: Setting prohibited. Note 2</td></tr>
</table>
Cautions 1. LPTXEN must be set to 1 since the frame size may exceed the maximum size of 1518 bytes while management tag insertion of the Ethernet switch is enabled (the SWTAGEN bit in the ETHSWMTC register is 1).
2. Setting the SF bit to 0 is prohibited. Always start operation after setting this bit to 1. For details, see section 8.5.1, Transmitting Data in Cut-Through Mode.</td></tr>
</table>

No.2-6 8.3.4.6 TX Mode Register (GMAC_TXMODE)

Bits 15 and 14 (FSTTH) were changed to reserved

V2.00

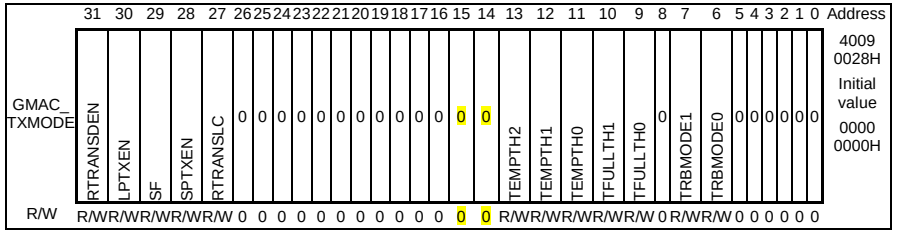
Page	Description
8-14	**[8.3.4.6 TX Mode Register (GMAC_TXMODE)]**



Bit Position	Bit Name	Description
15, 14	FSTTH1-0	15, 14 FSTTH1-0 Frame Start Threshold Transmission starts when the number of data words written to the TX FIFO buffer exceeds this value. 00: 4 words 01: 8 words 10: 16 words 11: 32 words

V3.00

Page	Revised Description
8-14	**[8.3.4.6 TX Mode Register (GMAC_TXMODE)]**



Bit Position	Bit Name	Description
15, 14	—	Reserved. The write value should be 0. Reading these bits returns 0.

No.2-7 8.4.1.2 Flow of Processing for Issuing the Hardware Function Call

Figure 8.3 Flow of Processing for Issuing the Hardware Function, modified

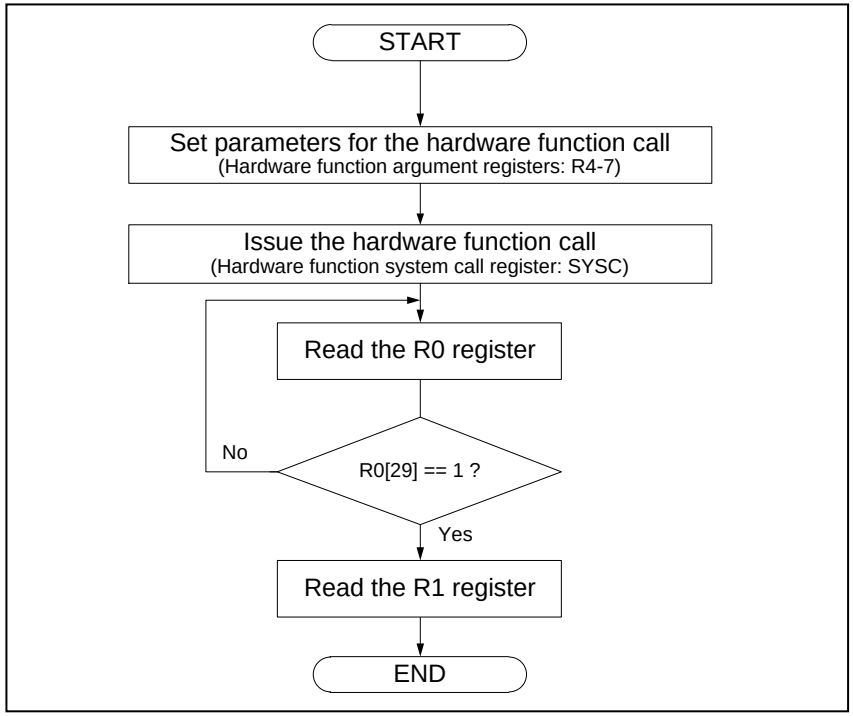
<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-33</td><td>[8.4.1.2 Flow of Processing for Issuing the Hardware Function Call]
 

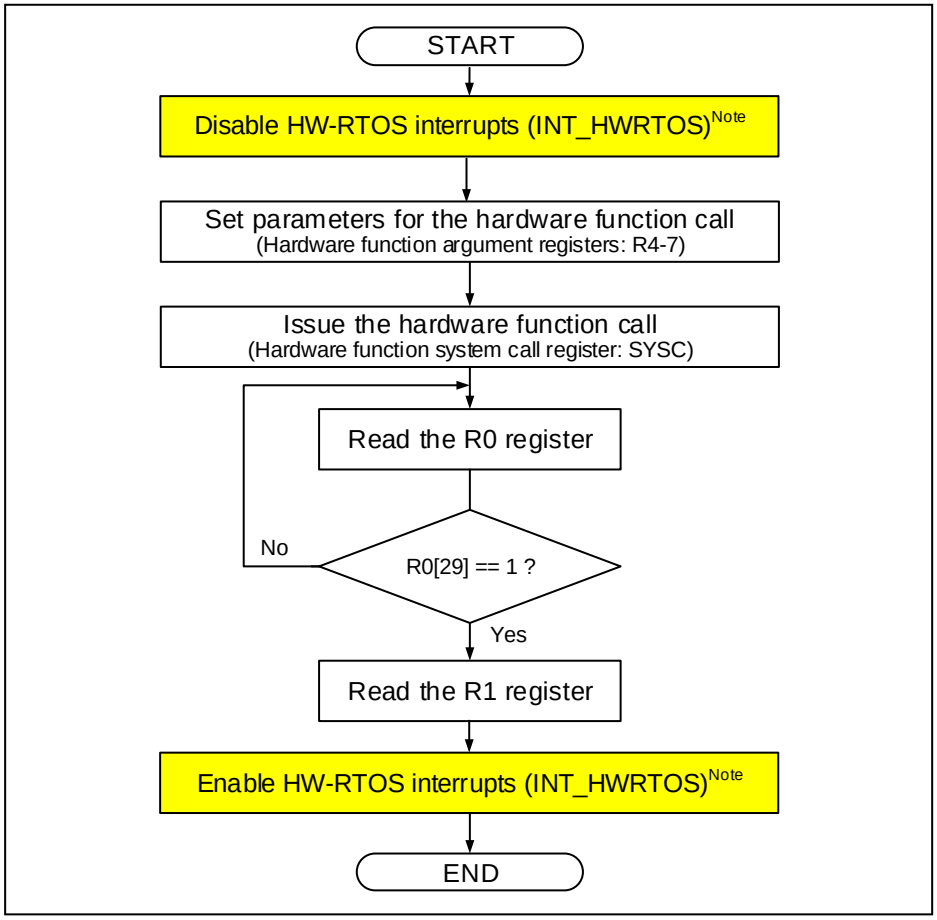
Figure 8.3 Flow of Processing for Issuing the Hardware Function</td><td>8-33</td><td>[8.4.1.2 Flow of Processing for Issuing the Hardware Function Call]
 

Figure 8.3 Flow of Processing for Issuing the Hardware Function

Note: This processing is required only when the hardware real-time OS is used.</td></tr>
</table>

No.2-8 8.4.1.3 Buffer Allocator

The description on an generation of an exception,

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-33</td><td>[(1) Functional Overview]

To use the buffer RAM, secure the required area (hereafter “buffer”) beforehand, and then issue the hardware function calls provided for the buffer allocator. Writing to an area which has not been secured by the CPU has no effect, but access to such area by the hardware function DMAC leads to the generation of an exception.</td><td>8-34</td><td>[(1) Functional Overview]

To use the buffer RAM, secure the required area (hereafter "buffer") beforehand, and then issue the hardware function calls provided for the buffer allocator. When writing to an area which has not been secured, access by the CPU or MAC DMA controller generates an interrupt, whereas access to such area by the buffer RAM DMA controller generates an interrupt or returns an exception to the return value register R0 depending on the type of hardware function calls.</td></tr>
</table>

No.2-9 8.4.1.3 Buffer Allocator

Return value registers, modified

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-36</td><td>[(2) Buffer Control Operation, (e) List of hardware function calls
Table 8.3 HWFNC_LongBuffer_Get]

<table>
<tr><td>R1[31:0]</td><td>First logical address of the buffer</td><td>[31:27] 5’b00001
[26] 1
[25:18] LLID
[17: 0] 0</td></tr>
</table>
</td><td>8-37</td><td>[(2) Buffer Control Operation, (e) List of hardware function calls
Table 8.3 HWFNC_LongBuffer_Get]

<table>
<tr><td>R1[31:0]</td><td>First logical address of the buffer</td><td>[31:27] 5’b00001
[26:24] 3'b100
[23:18] LLID
[17: 0] 0</td></tr>
</table>
</td></tr>
</table>

No.2-10 8.4.1.3 Buffer Allocator

Return value registers, modified

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-37</td><td>[(2) Buffer Control Operation, (e) List of hardware function calls
Table 8.4 HWFNC_ShortBuffer_Get]

R1[31:0] | First logical address of the buffer | [31:27] 5'b00001
[26] 0
[25:18] SBID
[18: 0] 0</td><td>8-38</td><td>[(2) Buffer Control Operation, (e) List of hardware function calls
Table 8.4 HWFNC_ShortBuffer_Get]

R1[31:0] | First logical address of the buffer | [31:27] 5'b00001
[26:25] 2'b00
[24:18] SBID
[17: 0] 0</td></tr>
</table>

No.2-11 8.4.1.4 MAC DMA Controller

Example modified

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-44</td><td>[(2) DMA for the Reception MAC, (b) Usage]
・ Procedure for reading and releasing buffers
[Example of reading and releasing a buffer]
(1) Read the BUFID register
(2) Shift the bits [27:16] read from BUFID 16 bits to the right to obtain the number of received words.
(3) The bits [15:0] read from the BUFID are bits [26:11] of the address where the acquired buffer starts.
The individual bits of the address where the acquired buffer starts are configured as follows.
[31:27]: 00001b
[26:19]: Equivalent to the bits [15:8] in the BUFID
([26] of the start address is always 1; [25:19] are LLID[6:0])
[18:11]: Equivalent to the bits [7:0] in the BUFID (always 0)
[10: 0]: Always 0
(4) After using the buffer, specify the start address as an argument and issue the buffer release function call to release the buffer.</td><td>8-45</td><td>[(2) DMA for the Reception MAC, (b) Usage]
・ Procedure for reading and releasing buffers
[Example of reading and releasing a buffer]
(1) Read the BUFID register
(2) Shift the bits [27:16] read from BUFID 16 bits to the right to obtain the number of received words.
(3) The bits [15:0] read from the BUFID are bits [26:11] of the address where the acquired buffer starts.
The individual bits of the address where the acquired buffer starts are configured as follows.
[31:27]: 00001b
[26:18]: Equivalent to the bits [15:7] in the BUFID
[17:11]: Equivalent to the bits [6:0] in the BUFID
[10: 0]: Always 0
(4) After using the buffer, specify the start address as an argument and issue the buffer release function call to release the buffer.</td></tr>
</table>

No.2-12 8.4.1.4 MAC DMA Controller

The description modified

V2.00		V3.00	
Page	Description	Page	Revised Description
8-45	**[(2) DMA for the Reception MAC, (c) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0. Access to an access-prohibited area (an area other than the buffer RAM, etc.) while the hardware function call is running leads to the return of an exception code in the return value register R0.	8-46	**[(2) DMA for the Reception MAC, (c) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0. If an error occurs while the hardware function call is running, an interrupt is generated.

No.2-13 8.4.1.4 MAC DMA Controller

The description modified

V2.00		V3.00	
Page	Description	Page	Revised Description
8-50	**[(3) DMA for the Transmission MAC, (d) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0.	8-51	**[(3) DMA for the Transmission MAC, (d) List of hardware function calls]** If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0. If an error occurs while the hardware function call is running, an interrupt is generated.

No.2-14 8.4.1.4 MAC DMA Controller

The description on the return value register R0,

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-50</td><td>[(3) DMA for the Transmission MAC, (d) List of hardware function calls
Table 8.12 HWFNC_MACDMA_TX_Errstat]
Return value registers
<table><tr><td>R0[1:0]</td><td>Result</td><td>[0]: Memory Access Violation
[1]: Memory Access Timeout</td></tr><tr><td>R0[28:2]</td><td>Unused</td><td>All 0s</td></tr></table></td><td>8-52</td><td>[(3) DMA for the Transmission MAC, (d) List of hardware function calls
Table 8.12 HWFNC_MACDMA_TX_Errstat]
Return value registers
<table><tr><td>R0[1:0]</td><td>Result</td><td>[0]: Memory Access Violation
• Access to the buffer that is not acquired
• The number of transfer bytes is not correct
• The start address of the descriptor is not on a 64-bit boundary.
[1]: Memory Access Timeout
• The start address of a transmission descriptor turns to be an end value (FFFF FFFFh)
• Releasing the buffer automatically is failed</td></tr><tr><td>R0[28:2]</td><td>Unused</td><td>All 0s</td></tr></table></td></tr>
</table>

No.2-15 8.4.1.5 Buffer RAM DMA Controller

The description modified

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-52</td><td>[(2) DMA Transfer, (d) List of hardware function calls]

If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0.
Access to an access-prohibited area (an area other than the buffer RAM, etc.) while the hardware function call is running leads to the return of an exception code in the return value register R0.</td><td>8-54</td><td>[(2) DMA Transfer, (d) List of hardware function calls]

If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0.
Access to an access-prohibited area (an area other than the buffer RAM, etc.) while the hardware function call is running leads HWFNC_Direct_Memory_Transfer and HWFNC_Direct_Memory_Replace to return an exception to the return value register R0, whereas it leads HWFNC_INTBUFF_DMA_Start and HWFNC_INTBUFF_DMA_Start (Descriptor) to generate an interrupt.</td></tr>
</table>

No.2-16 8.4.1.5 Buffer RAM DMA Controller The description on argument registers, modified

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-52</td><td>[(2) DMA Transfer, (d) List of hardware function calls
Table 8.13 HWFNC_Direct_Memory_Transfer]

Argument registers<table><tr><td>R4[31:0]</td><td>Address where the destination area for transfer starts</td><td>Specifies the address where the destination area for transfer starts.</td></tr><tr><td>R5[31:0]</td><td>Address where the source area for transfer starts</td><td>Specifies the address where the source address for transfer starts.</td></tr></table></td><td>8-54</td><td>[(2) DMA Transfer, (d) List of hardware function calls
Table 8.13 HWFNC_Direct_Memory_Transfer]

Argument registers<table><tr><td>R4[31:0]</td><td>Address where the source area for transfer starts</td><td>Specifies the address where the source area for transfer starts.</td></tr><tr><td>R5[31:0]</td><td>Address where the destination area for transfer starts</td><td>Specifies the address where the destination area for transfer starts.</td></tr></table></td></tr>
</table>

No.2-17 8.4.2 Interrupts

The condition to generate an MACDMA transmission error interrupt, that is related to operations for transmission, modified

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-56</td><td>[Table 8.17 Interrupts Related to Operations for Transmission]

<table><tr><th>Interrupt Name</th><th>Symbol</th><th>Conditions for Asserting and De-asserting Interrupts</th></tr><tr><td>MACDMA transmission error interrupt</td><td>INTETHTXDERR</td><td>This interrupt is generated when the address field of a descriptor is outside the range of the buffer, the number of bytes for transfer is invalid, or a descriptor is not set to start on a 64-bit boundary.
Modify the settings of the transmission descriptor for retransmission.
Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.</td></tr></table></td><td>8-58</td><td>[Table 8.17 Interrupts Related to Operations for Transmission]

<table><tr><th>Interrupt Name</th><th>Symbol</th><th>Conditions for Asserting and De-asserting Interrupts</th></tr><tr><td>MACDMA transmission error interrupt</td><td>INTETHTXDERR</td><td>This interrupt is generated, when an error occurs while the transmission MAC DMA is operating. As there are several error sources, HWFNC_MACDMA_TX_Errstat is used to obtain the error source.
Modify the settings of the transmission descriptor for retransmission.
Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.</td></tr></table></td></tr>
</table>

No.2-18 8.4.2 Interrupts

The buffer RAM area access error was added to interrupts related to other operations.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>8-58</td><td>[Table 8.19 Interrupts Related to Other Operations]
<table><tr><th>Interrupt Name</th><th>Symbol</th><th>Conditions for Asserting and De-asserting Interrupts</th></tr><tr><td colspan="3">N/A</td></tr></table></td><td>8-60</td><td>[Table 8.19 Interrupts Related to Other Operations]
<table><tr><th>Interrupt Name</th><th>Symbol</th><th>Conditions for Asserting and De-asserting Interrupts</th></tr><tr><td>Buffer RAM area access error</td><td>INTBRAMERR</td><td>This interrupt is generated, if the buffer that is not acquired by the CPU is accessed. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.</td></tr></table></td></tr>
</table>

No.2-19 8.5 Notes

Notes regarding transmission in cut-through mode and transmission and reception of jumbo frames were added.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>-</td><td>[8.5.5 Transmitting Data in Cut-Through Mode]

N/A</td><td>8-87</td><td>[8.5.5 Transmitting Data in Cut-Through Mode]

Setting the SF bit (b29) of the TX Mode register (GMAC_TXMODE) to 0 may lead to generation of an unexpected TX FIFO underflow interrupt. To avoid this, always set this bit to 1 (Store & Forward mode).</td></tr>
<tr><td></td><td>[8.5.6 Jumbo Frames]

N/A</td><td></td><td>[8.5.6 Jumbo Frames]

This product does not support transmission and reception of frames exceeding 1,518 bytes, i.e. jumbo frames.</td></tr>
</table>

No.2-20 9.3.1 List of Registers, (5) Timer Module

Registers Address of the interrupt status/ACK register,

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>9-4</td><td>[(5) Timer Module Registers]
<table>
<tr><th>Register Name</th><th>Symbol</th><th>Address</th></tr>
<tr><td>• Configuration and Setting</td><td></td><td></td></tr>
<tr><td>Timer module configuration register</td><td>TSM_CONFIG</td><td>4007 C004H</td></tr>
<tr><td>Interrupt status/ACK register</td><td>TSM_IRQ_STAT_ACK</td><td>4007 0008H</td></tr>
<tr><td>• Transmit Timestamp (n = 0, 1)</td><td></td><td></td></tr>
<tr><td>Port timestamp control/status register n</td><td>PORTn_CTRL</td><td>4007 C020H + 0008H*n</td></tr>
<tr><td>Port timestamp register n</td><td>PORTn_TIME</td><td>4007 0024H + 0008H*n</td></tr>
<tr><td>• Timer Settings</td><td></td><td></td></tr>
<tr><td>Timer control register</td><td>ATIME_CTRL</td><td>4007 C120H</td></tr>
<tr><td>Timer nanosecond register</td><td>ATIME</td><td>4007 C124H</td></tr>
<tr><td>Timer offset correction register</td><td>ATIME_OFFSET</td><td>4007 C128H</td></tr>
<tr><td>Timer periodic event generation register</td><td>ATIME_EVT_PERIOD</td><td>4007 C12CH</td></tr>
<tr><td>Timer drift correction register</td><td>ATIME_CORR</td><td>4007 C130H</td></tr>
<tr><td>Timer increment register</td><td>ATIME_INC</td><td>4007 C134H</td></tr>
<tr><td>Timer second register</td><td>ATIME_SEC</td><td>4007 C138H</td></tr>
<tr><td>Timer offset correction count register</td><td>ATIME_OFFS_CORR</td><td>4007 C13CH</td></tr>
</table></td><td>9-4</td><td>[(5) Timer Module Registers]
<table>
<tr><th>Register Name</th><th>Symbol</th><th>Address</th></tr>
<tr><td>• Configuration and Setting</td><td></td><td></td></tr>
<tr><td>Timer module configuration register</td><td>TSM_CONFIG</td><td>4007 C004H</td></tr>
<tr><td>Interrupt status/ACK register</td><td>TSM_IRQ_STAT_ACK</td><td>4007 C008H</td></tr>
<tr><td>• Transmit Timestamp (n = 0, 1)</td><td></td><td></td></tr>
<tr><td>Port timestamp control/status register n</td><td>PORTn_CTRL</td><td>4007 C020H + 0008H*n</td></tr>
<tr><td>Port timestamp register n</td><td>PORTn_TIME</td><td>4007 C024H + 0008H*n</td></tr>
<tr><td>• Timer Settings</td><td></td><td></td></tr>
<tr><td>Timer control register</td><td>ATIME_CTRL</td><td>4007 C120H</td></tr>
<tr><td>Timer nanosecond register</td><td>ATIME</td><td>4007 C124H</td></tr>
<tr><td>Timer offset correction register</td><td>ATIME_OFFSET</td><td>4007 C128H</td></tr>
<tr><td>Timer periodic event generation register</td><td>ATIME_EVT_PERIOD</td><td>4007 C12CH</td></tr>
<tr><td>Timer drift correction register</td><td>ATIME_CORR</td><td>4007 C130H</td></tr>
<tr><td>Timer increment register</td><td>ATIME_INC</td><td>4007 C134H</td></tr>
<tr><td>Timer second register</td><td>ATIME_SEC</td><td>4007 C138H</td></tr>
<tr><td>Timer offset correction count register</td><td>ATIME_OFFS_CORR</td><td>4007 C13CH</td></tr>
</table></td></tr>
</table>

No.2-21 9.3.1 List of Registers, (6) DLR Module

Registers Address of the interrupt status/ACK register,

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>9-5</td><td>[(6) DLR Module Registers]
<table>
<tr><th>Register Name</th><th>Symbol</th><th>Address</th></tr>
<tr><td>• Configuration and Setting</td><td></td><td></td></tr>
<tr><td>DLR control register</td><td>DLR_CONTROL</td><td>4007 E000H</td></tr>
<tr><td>DLR status register</td><td>DLR_STATUS</td><td>4007 E004H</td></tr>
<tr><td>DLR Ethernet type register</td><td>DLR_ETH_TYP</td><td>4007 E008H</td></tr>
<tr><td>DLR interrupt control register</td><td>DLR_IRQ_CTRL</td><td>4007 E00CH</td></tr>
<tr><td>DLR interrupt status/ACK register</td><td>DLR_IRQ_STAT_ACK</td><td>4007 E010H</td></tr>
<tr><td>DLR local MAC address low register</td><td>LOC_MAClo</td><td>4007 E014H</td></tr>
<tr><td>DLR local MAC address high register</td><td>LOC_MAChi</td><td>4007 0018H</td></tr>
<tr><td>• Beacon Frame Parameters</td><td></td><td></td></tr>
<tr><td>DLR supervisor MAC address low register</td><td>SUPR_MAClo</td><td>4007 E020H</td></tr>
<tr><td>DLR supervisor MAC address high register</td><td>SUPR_MAChi</td><td>4007 E024H</td></tr>
<tr><td>DLR ring status/VLAN register</td><td>STATE_VLAN</td><td>4007 E028H</td></tr>
<tr><td>DLR beacon timeout timer register</td><td>BEC_TMOUT</td><td>4007 E02CH</td></tr>
<tr><td>DLR beacon interval register</td><td>BEC_INTRVL</td><td>4007 E030H</td></tr>
<tr><td>DLR supervisor IP address register</td><td>SUPR_IPADR</td><td>4007 E034H</td></tr>
<tr><td>DLR sub type/protocol version register</td><td>ETH_STYP_VER</td><td>4007 E038H</td></tr>
<tr><td>DLR beacon invalid timeout timer register</td><td>INV_TMOUT</td><td>4007 E03CH</td></tr>
<tr><td>DLR sequence ID register</td><td>SEQ_ID</td><td>4007 E040H</td></tr>
<tr><td>• DLR statistics counters</td><td></td><td></td></tr>
<tr><td>DLR MAC statistics counters</td><td>Refer to section エラー! 参照元が見つかりません。</td><td>Refer to section エラー! 参照元が見つかりません。</td></tr>
</table></td><td>9-5</td><td>[(6) DLR Module Registers]
<table>
<tr><th>Register Name</th><th>Symbol</th><th>Address</th></tr>
<tr><td>• Configuration and Setting</td><td></td><td></td></tr>
<tr><td>DLR control register</td><td>DLR_CONTROL</td><td>4007 E000H</td></tr>
<tr><td>DLR status register</td><td>DLR_STATUS</td><td>4007 E004H</td></tr>
<tr><td>DLR Ethernet type register</td><td>DLR_ETH_TYP</td><td>4007 E008H</td></tr>
<tr><td>DLR interrupt control register</td><td>DLR_IRQ_CTRL</td><td>4007 E00CH</td></tr>
<tr><td>DLR interrupt status/ACK register</td><td>DLR_IRQ_STAT_ACK</td><td>4007 E010H</td></tr>
<tr><td>DLR local MAC address low register</td><td>LOC_MAClo</td><td>4007 E014H</td></tr>
<tr><td>DLR local MAC address high register</td><td>LOC_MAChi</td><td>4007 E018H</td></tr>
<tr><td>• Beacon Frame Parameters</td><td></td><td></td></tr>
<tr><td>DLR supervisor MAC address low register</td><td>SUPR_MAClo</td><td>4007 E020H</td></tr>
<tr><td>DLR supervisor MAC address high register</td><td>SUPR_MAChi</td><td>4007 E024H</td></tr>
<tr><td>DLR ring status/VLAN register</td><td>STATE_VLAN</td><td>4007 E028H</td></tr>
<tr><td>DLR beacon timeout timer register</td><td>BEC_TMOUT</td><td>4007 E02CH</td></tr>
<tr><td>DLR beacon interval register</td><td>BEC_INTRVL</td><td>4007 E030H</td></tr>
<tr><td>DLR supervisor IP address register</td><td>SUPR_IPADR</td><td>4007 E034H</td></tr>
<tr><td>DLR sub type/protocol version register</td><td>ETH_STYP_VER</td><td>4007 E038H</td></tr>
<tr><td>DLR beacon invalid timeout timer register</td><td>INV_TMOUT</td><td>4007 E03CH</td></tr>
<tr><td>DLR sequence ID register</td><td>SEQ_ID</td><td>4007 E040H</td></tr>
<tr><td>• DLR statistics counters</td><td></td><td></td></tr>
<tr><td>DLR MAC statistics counters</td><td>See section エラー! 参照元が見つかりません。</td><td>See section エラー! 参照元が見つかりません。</td></tr>
</table></td></tr>
</table>

No.2-22 10.7 Memory Access Timing Examples

The number of address setup waits in the SRAM write cycles was corrected.

V2.00		V3.00	
Page	Description	Page	Revised Description
10-20	**[Figure 10.11 SRAM Write Cycles (with No Wait)]** BSC: SBS3-SBS0 = 1111B (32 bits), SMCn: WWn3-WWn0 = 0000B/0001B (1 wait cycle) DWn3-DWn0 = 0000B (no wait), ACn3-ACn0 = 0000B/0001B (no wait)	10-20	**[Figure 10.11 SRAM Write Cycles (with No Wait)]** BSC: SBS3-SBS0 = 1111B (32 bits), SMCn: WWn3-WWn0 = 0000B/0001B (1 wait cycle) DWn3-DWn0 = 0000B (no wait), ACn3-ACn0 = 0000B/0001B (1 wait cycle)

No.2-23 10.7 Memory Access Timing Examples

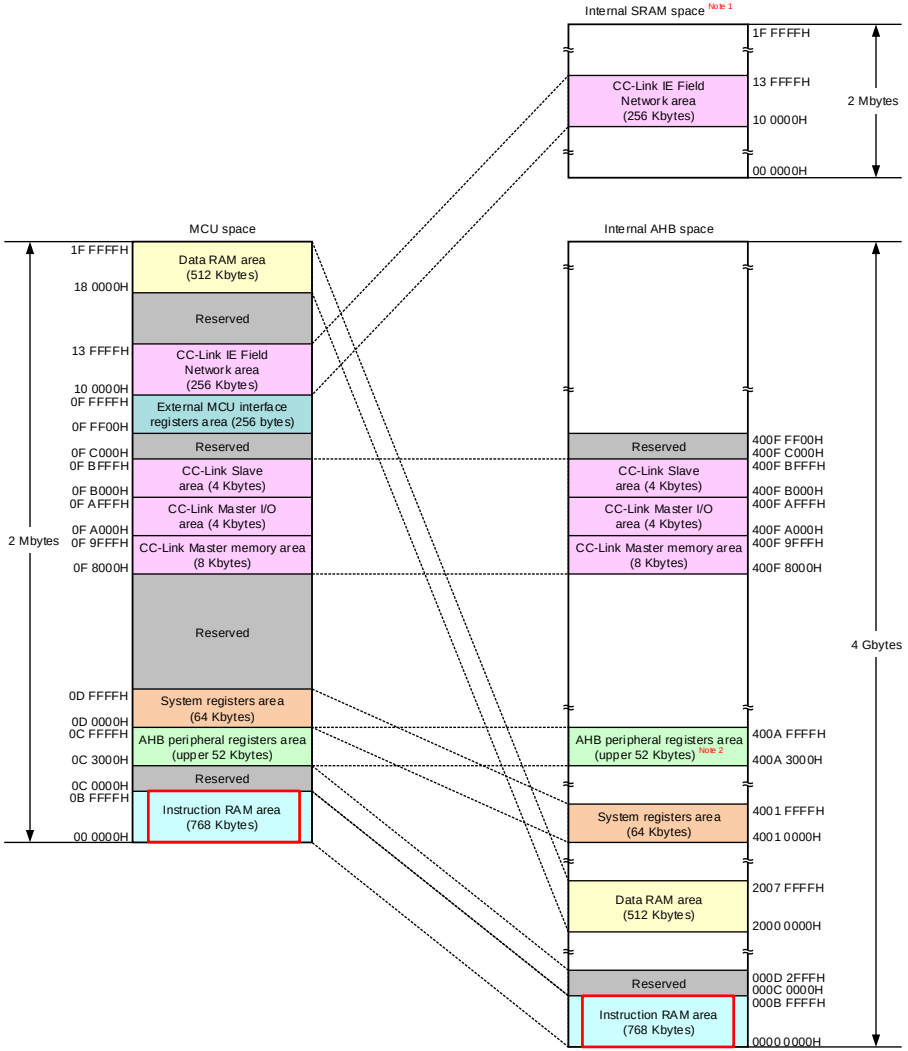
Signal name corrected (STCSZn → CSZn)

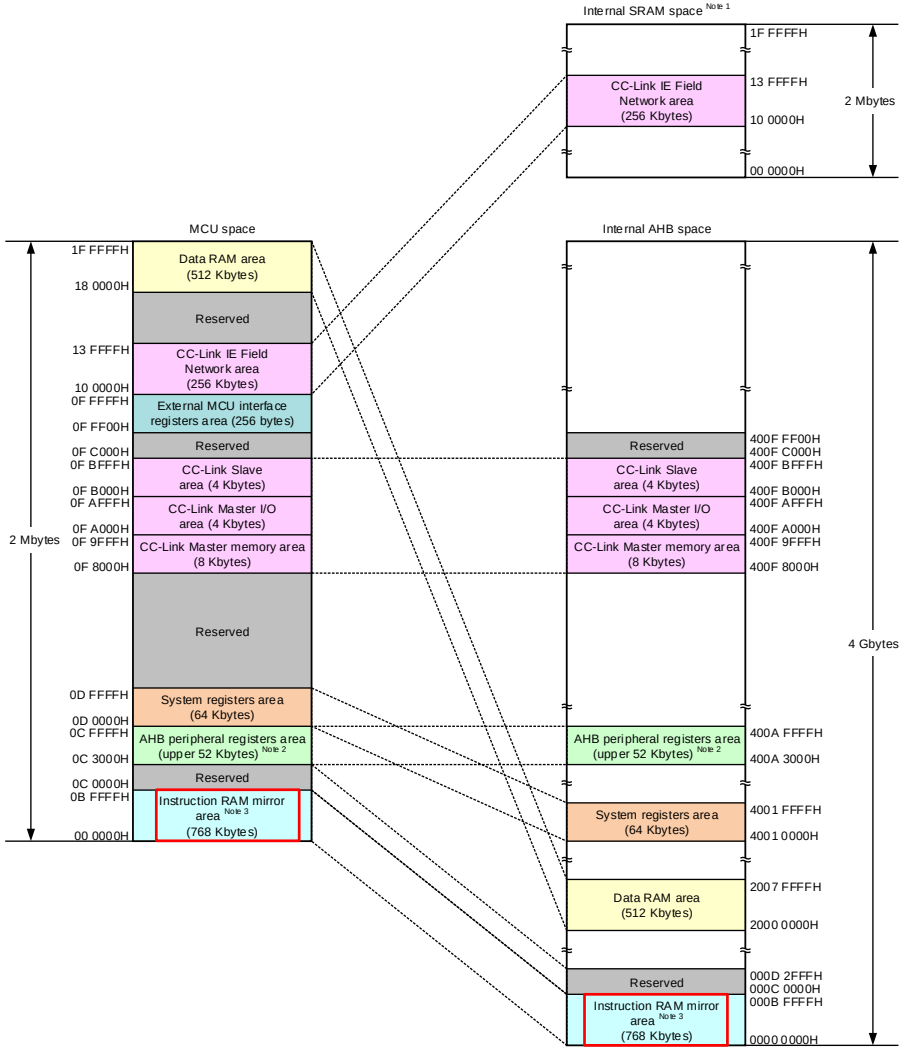
V2.00		V3.00	
Page	Description	Page	Revised Description
10-17 to 10-24	**[10.7 Memory Access Timing Examples]** Signal name corrected "STCSZn" was used. Figure 10.8 SRAM Read Cycles Figure 10.9 SRAM Read Cycles (with Wait Settings) Figure 10.10 SRAM Read Cycles (External Wait Insertion) Figure 10.11 SRAM Write Cycles (with No Wait) Figure 10.12 SRAM Write Cycles (with Wait States) Figure 10.13 SRAM Write Cycles (External Wait Insertion) Figure 10.14 Page ROM Read Cycles (Single Transfer) Figure 10.15 Page ROM Read Cycles (Four Burst Transfer)	10-17 to 10-24	**[10.7 Memory Access Timing Examples]** Signal name "CSZn" was used. Figure 10.8 SRAM Read Cycles Figure 10.9 SRAM Read Cycles (with Wait Settings) Figure 10.10 SRAM Read Cycles (External Wait Insertion) Figure 10.11 SRAM Write Cycles (with No Wait) Figure 10.12 SRAM Write Cycles (with Wait States) Figure 10.13 SRAM Write Cycles (External Wait Insertion) Figure 10.14 Page ROM Read Cycles (Single Transfer) Figure 10.15 Page ROM Read Cycles (Four Burst Transfer)

No.2-24 12.1 Memory Map

"Instruction RAM area" was corrected to "Instruction RAM mirror area".

V2.00		V3.00	
Page	Description	Page	Revised Description
12-3	**[Figure 12.1 External MCU Interface Space]**	12-3	**[Figure 12.1 External MCU Interface Space]**





No.2-25 12.1 Memory Map

Note regarding the instruction RAM mirror area was

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>12-3</td><td>[Figure 12.1 External MCU Interface Space]

Notes 1. The CC-Link IE Field Network area is only accessible in the mode for connection to synchronous SRAM supporting MCUs.
2. The upper 52 Kbytes of the AHB peripheral registers area covers the range from the GPIO area to the synchronous burst memory controller control registers. For details, see figure 3.1, Memory Map, in the R-IN32M4-CL2 User's Manual.</td><td>12-4</td><td>[Figure 12.1 External MCU Interface Space]

Notes 1. The CC-Link IE Field Network area is only accessible in the mode for connection to synchronous SRAM supporting MCUs.
2. The upper 52 Kbytes of the AHB peripheral registers area covers the range from the GPIO area to the synchronous burst memory controller control registers. For details, see figure 3.1, Entire Memory Map, in the R-IN32M4-CL2 User's Manual.
3. The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture.
<table><tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr><tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr><tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr><tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr><tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr></table></td></tr>
</table>

No.2-26 12.2.5 Control Registers, (2) HOSTIF Bus Control Register (HIFBCC)

The instruction RAM area was modified to the instruction RAM mirror area.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>12-17</td><td>[(2) HOSTIF bus control register (HIFBCC)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>1</td><td>RBUFON1</td><td>Enables or disables advance reading of the instruction RAM area.
0: Advance reading is disabled.
1: Advance reading is enabled.</td></tr>
</table></td><td>12-18</td><td>[(2) HOSTIF bus control register (HIFBCC)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>1</td><td>RBUFON1</td><td>Enables or disables advance reading of the instruction RAM mirror area.
0: Advance reading is disabled.
1: Advance reading is enabled.</td></tr>
</table></td></tr>
<tr><td>12-18</td><td>[Table 12.8 Address Range for which Advance Reading and Page ROM Reading are Selectable]

<table>
<tr><th rowspan="2">Target Macro</th><th colspan="2">Address Range</th><th colspan="2">Related Enable Bits</th></tr>
<tr><th>MPU Space</th><th>Internal AHB Space</th><th>Advance Reading</th><th>Page ROM</th></tr>
<tr><td>Instruction RAM</td><td>0B FFFFH
to
00 0000H</td><td>000B FFFFH
to
0000 0000H</td><td>HIFBCC.
RBUFON1</td><td>HIFPRC.
PAGEON1</td></tr>
</table></td><td>12-19</td><td>[Table 12.8 Address Range for which Advance Reading and Page ROM Reading are Selectable]

<table>
<tr><th rowspan="2">Target Macro</th><th colspan="2">Address Range</th><th colspan="2">Related Enable Bits</th></tr>
<tr><th>MPU Space</th><th>Internal AHB Space</th><th>Advance Reading</th><th>Page ROM</th></tr>
<tr><td>Instruction RAM mirror area</td><td>0B FFFFH
to
00 0000H</td><td>000B FFFFH
to
0000 0000H</td><td>HIFBCC.
RBUFON1</td><td>HIFPRC.
PAGEON1</td></tr>
</table></td></tr>
</table>

No.2-27 12.2.5 Control Registers, (2) HOSTIF bus control register (HIFBCC)

Caution regarding access to the instruction RAM mirror area while advance reading is enabled was added.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>12-18</td><td>[(2) HOSTIF bus control register (HIFBCC)]

Note: Some areas cannot be read in advance depending on the target macro even if advance reading is enabled.</td><td>12-19</td><td>[(2) HOSTIF bus control register (HIFBCC)]

Cautions 1. Some areas cannot be read in advance depending on the target macro even if advance reading is enabled.
2. If the last 16-byte area of the instruction RAM mirror area is read while advance reading is enabled, this will lead to assertion of the HERROUTZ pin.</td></tr>
</table>

No.2-28 12.2.5 Control Registers, (4) HOSTIF page ROM control register (HIFPRC)

The instruction RAM area was modified to the instruction RAM mirror area.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>12-20</td><td>[(4) HOSTIF page ROM control register (HIFPRC)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>1</td><td>PAGEON1</td><td>Page ROM reading of the instruction RAM area is set up.
0: SRAM reading
1: Page ROM reading</td></tr>
</table></td><td>12-21</td><td>[(4) HOSTIF page ROM control register (HIFPRC)]

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>1</td><td>PAGEON1</td><td>Page ROM reading of the instruction RAM mirror area is set up.
0: SRAM reading
1: Page ROM reading</td></tr>
</table></td></tr>
</table>

No.2-29 14.1.1 Overview

Description of skipping was modified.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>14-2</td><td>[14.1.1 Overview]

• Skipping
A continuous access size and separation access size can be set respectively for the area for access in DMA transfer. After access to a set size for continuous access, the set separation access size can be skipped before access to the next address.</td><td>14-2</td><td>[14.1.1 Overview]

• Skipping
A continuous access size and skip space size can be set respectively for the area for access in DMA transfer. After access to a set size for continuous access, the set skip space size can be skipped before access to the next address.</td></tr>
</table>

No.2-30 14.4.6 DMA Trigger Source Registers (DTFRn, RTDTFR)

Note regarding external DMA transfer request inputs that are selected as DMA transfer trigger sources was added.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>14-86</td><td>[14.4.6 DMA Trigger Source Registers (DTFRn, RTDTFR)]

<table>
<tr><th>IFCn6-IFCn0</th><th>Selection of a DMA Trigger Source</th></tr>
<tr><td>01H</td><td>DMAREQZ0 pin (DMA transfer request) input (Only the setting of the DTFR0 register is effective).</td></tr>
<tr><td>02H</td><td>DMAREQZ1 pin (DMA transfer request) input (Only the setting of the DTFR1 register is effective)</td></tr>
<tr><td>03H</td><td>RTDMAREQZ pin (DMA transfer request) input (Only the setting of the RTDTFR register is effective).</td></tr>
</table>
[14.4.6 DMA Trigger Source Registers (DTFRn, RTDTFR)]

N/A</td><td>14-87</td><td>[14.4.6 DMA Trigger Source Registers (DTFRn, RTDTFR)]

<table>
<tr><th>IFCn6-IFCn0</th><th>Selection of a DMA Trigger Source</th></tr>
<tr><td>01H</td><td>DMAREQZ0 pin (DMA transfer request) input Note</td></tr>
<tr><td>02H</td><td>DMAREQZ1 pin (DMA transfer request) input Note</td></tr>
<tr><td>03H</td><td>RTDMAREQZ pin (DMA transfer request) input Note</td></tr>
</table>
[14.4.6 DMA Trigger Source Registers (DTFRn, RTDTFR)]

Note: External DMA transfer request inputs on the DMAREQZ0, DMAREQZ1, and RTDMAREQZ pins can be individually set as DMA transfer trigger requests for the corresponding registers listed below.
DMAREQZ0 pin: DTFR0 register
DMAREQZ1 pin: DTFR1 register
RTDMAREQZ pin: RTDTFR register</td></tr>
</table>

No.2-31 14.6 Interrupt Output

Settings related to interrupt putout waveform of the general DMA controller and the DMA controller for real-time ports were deleted.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>14-91</td><td>

[Table 14.9 General DMA Controller Interrupt Output]

<table>
<tr><th>Interrupt Signal</th><th>Interrupt Source</th><th>Interrupt Detection Mask</th><th>Switch between Pulse Output and Interrupt Output</th><th>Interrupt Output Mask</th></tr>
<tr><td rowspan="2">INTDMAn</td><td>The DMA transaction is completed.</td><td>CHCFGn register DEM = 1</td><td rowspan="3">DCTRL register
LVINT = 0: Pulse output
LVINT = 1: Level output</td><td rowspan="2">CHSTATn. INTM = 1</td></tr>
<tr><td>An invalid descriptor is read in link mode.</td><td>DIM in the header = 1</td></tr>
<tr><td>INTDMEERR</td><td>An error response is returned in response to a transfer request issued by the master interface.</td><td>- (Not available)</td><td>- (Not available)</td></tr>
</table>

[Table 14.10 Interrupt Output of DMA Controller for Real-Time Ports]

<table>
<tr><th>Interrupt Signal</th><th>Interrupt Source</th><th>Interrupt Detection Mask</th><th>Switch between Pulse Output and Interrupt Output</th><th>Interrupt Output Mask</th></tr>
<tr><td rowspan="2">INTRTDMA</td><td>The DMA transaction is completed.</td><td>RTCHCFG register DEM = 1</td><td rowspan="3">RTDCTRL register
LVINT = 0: Pulse output
LVINT = 1: Level output</td><td rowspan="2">RTCHSTAT. INTM = 1</td></tr>
<tr><td>An invalid descriptor is read in link mode.</td><td>DIM in the header = 1</td></tr>
<tr><td>INTRTDMEERR</td><td>An error response is returned in response to a transfer request issued by the master interface.</td><td>- (Not available)</td><td>- (Not available)</td></tr>
</table>

</td><td>14-92</td><td>

[Table 14.9 General DMA Controller Interrupt Output]

<table>
<tr><th>Interrupt Signal</th><th>Interrupt Source</th><th>Interrupt Detection Mask</th><th>Interrupt Output Mask</th></tr>
<tr><td rowspan="2">INTDMAn</td><td>The DMA transaction is completed.</td><td>CHCFGn register DEM = 1</td><td rowspan="2">CHSTATn. INTM = 1</td></tr>
<tr><td>An invalid descriptor is read in link mode.</td><td>DIM in the header = 1</td></tr>
<tr><td>INTDMEERR</td><td>An error response is returned in response to a transfer request issued by the master interface.</td><td>- (Not available)</td><td>- (Not available)</td></tr>
</table>

[Table 14.10 Interrupt Output of DMA Controller for Real-Time Ports]

<table>
<tr><th>Interrupt Signal</th><th>Interrupt Source</th><th>Interrupt Detection Mask</th><th>Interrupt Output Mask</th></tr>
<tr><td rowspan="2">INTRTDMA</td><td>The DMA transaction is completed.</td><td>RTCHCFG register DEM = 1</td><td rowspan="2">RTCHSTAT. INTM = 1</td></tr>
<tr><td>An invalid descriptor is read in link mode.</td><td>DIM in the header = 1</td></tr>
<tr><td>INTRTDMEERR</td><td>An error response is returned in response to a transfer request issued by the master interface.</td><td>- (Not available)</td><td>- (Not available)</td></tr>
</table>

</td></tr>
</table>

No.2-32 20.4.2 Master/Slave Connections [1/2]

Diagram of connections between one master and one slave was modified. CSIH pin names were changed and the CSIHnTSSI pin was deleted.

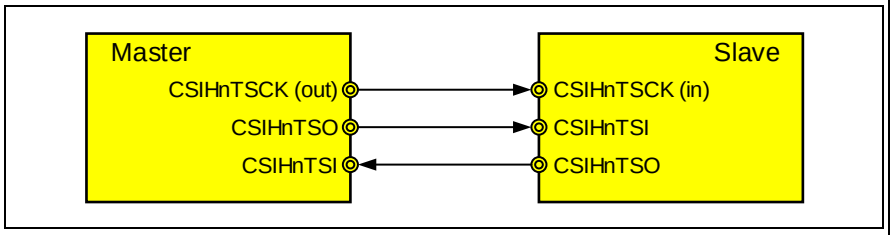
<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>20-38</td><td>[(1) One master and one slave]
 

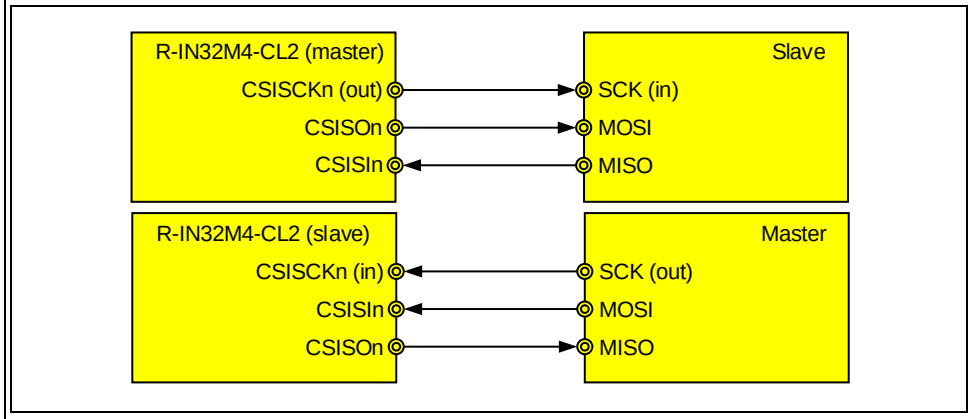
Figure 20.4 Direct Master/Slave Connection</td><td>20-38</td><td>[(1) One master and one slave]
 

Figure 20.4 Direct Master/Slave Connection</td></tr>
</table>

No.2-32 20.4.2 Master/Slave Connections [2/2]

Diagram of connections between one master and two slaves was modified. CSIH pin names were changed and the CSIHnTSSI pin was deleted.

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>20-38</td><td>[(2) One master and two slaves]

The following figure illustrates the connections between an R-IN32M4 as a master and two slaves. In this example, an R-IN32M4 can be configured to supply one chip select (CS) signal to each slave. This signal is connected to the slave select input CSIHnTSSI of the slave.

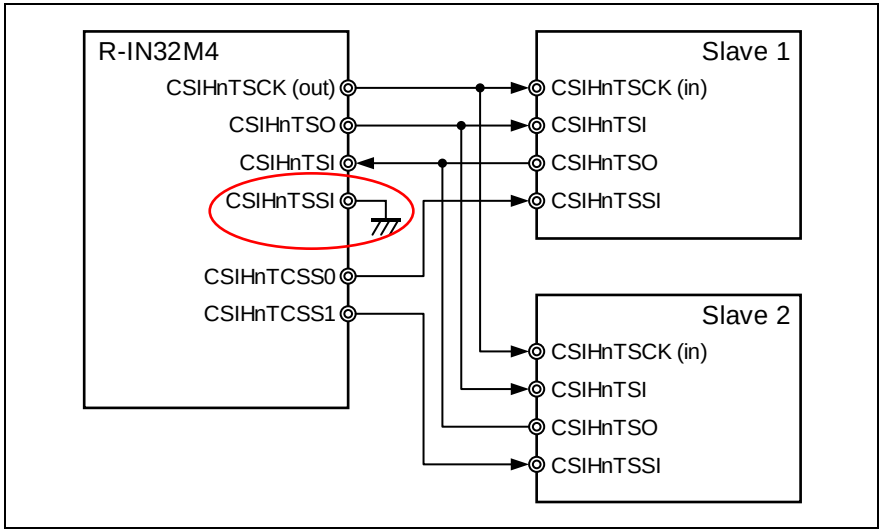
 

Figure 20.5 Connection between One Master and Two Slaves

The default chip select level is active low. In other words, when the slave select input signal (CSIHnTSSI) of a slave is at the low level, that slave is selected as a CSIH slave (and enabled). However, to use a chip select signal (CS) for another device, programming that sets the chip select signal output level to active high is possible.
If a slave is not selected, it will neither receive nor transmit data. In addition, its output CSIHnTSO is set to input mode in order to avoid interference with the output of another slave that was selected.</td><td>20-38, 39</td><td>[(2) One master and two slaves]

The following figure illustrates the connections between an R-IN32M4 as a master and two slaves. In this example, an R-IN32M4 can be configured to supply one chip select (CS) signal to each slave. This signal is connected to the slave select input SSI of the slave.

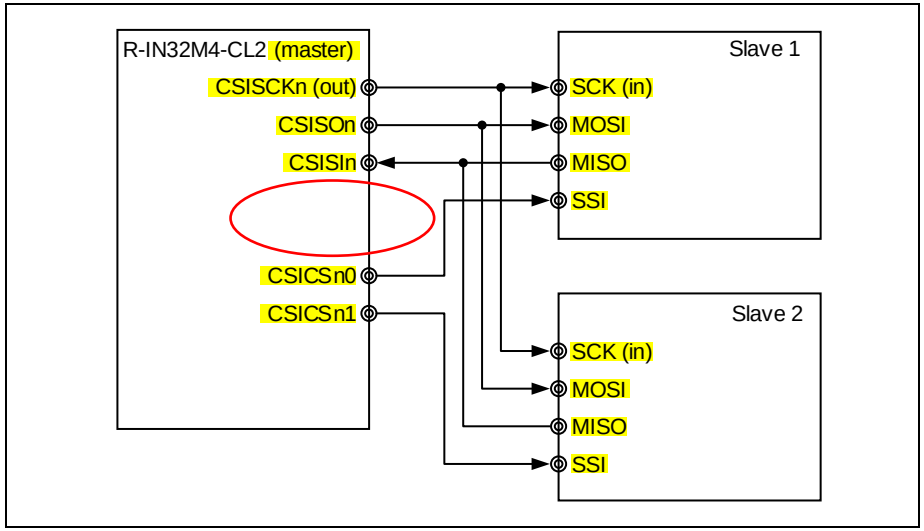
 

Figure 20.5 Connection between One Master and Two Slaves

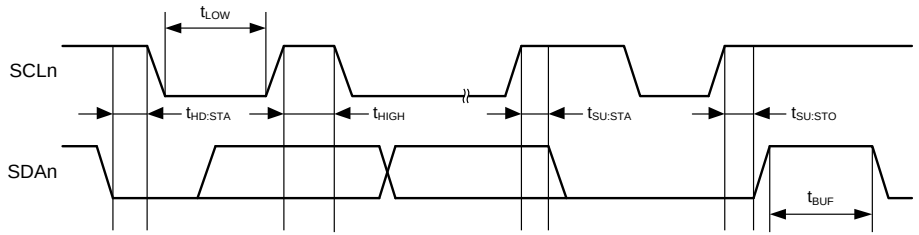
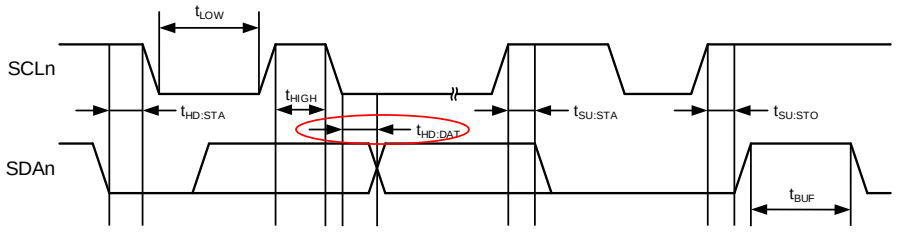
The default chip select level is active low. In other words, when the slave select input signal (SSI) of a slave is at the low level, that slave is selected as a CSIH slave (and enabled). However, to use a chip select signal (CS) for another device, programming that sets the chip select signal output level to active high is possible.
If a slave is not selected, it will neither receive nor transmit data. In addition, its output MISO is set to input mode in order to avoid interference with the output of another slave that was selected.</td></tr>
<tr><td>20-39</td><td>[(3) CSIHnTSO output control]

The CSIH can output CSIHnTSO when all of the following conditions are satisfied:
· The CSIH is enabled (CSIHnCTL0.CSIHnPWR = 1).
· The CSIH is operated in transmit-only or transmit/receive mode (CSIHnCTL0.CSIHnTXE = 1).
By using this function, signal congestions on the external CSIHnTSO signal line can be avoided.</td><td>20-39</td><td>[(3) CSISOn output control]

The CSIH can output CSISOn when all of the following conditions are satisfied:
· The CSIH is enabled (CSIHnCTL0.CSIHnPWR = 1).
· The CSIH is operated in transmit-only or transmit/receive mode (CSIHnCTL0.CSIHnTXE = 1).
By using this function, signal congestions on the external CSISOn signal line can be avoided.</td></tr>
</table>

No.2-33 21.3 (6) IICBn high-level width setting register (IICBnWH)

Generation timing of $t_{SU:STA}$ modified; $t_{HD:DAT}$ added in the timing chart

<table>
<tr><th colspan="2">V2.00</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>21-14</td><td>[Table 21.4 Conditions for Generating Serial Output Timing]
<table>
<tr><th>Symbol</th><th>Description</th><th>Standard Mode</th><th>Fast Mode</th></tr>
<tr><td>$t_{HD:STA}$</td><td>Start condition hold time</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>t_{LOW}</td><td>SCL low-level width period</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>t_{HIGH}</td><td>SCL high-level width period</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>$t_{SU:STA}$</td><td>Start condition setup time</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>$t_{SU:STO}$</td><td>Stop condition setup time</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>t_{BUF}</td><td>Bus free time (interval between stop condition and start condition)</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>$t_{HD:DAT}$</td><td>Data hold time</td><td>IICB0WL[9:2] / PCLK</td><td>IICB0WL[9:2] / PCLK</td></tr>
</table>

</td><td>21-14</td><td>[Table 21.4 Conditions for Generating Serial Output Timing]
<table>
<tr><th>Symbol</th><th>Description</th><th>Standard Mode</th><th>Fast Mode</th></tr>
<tr><td>$t_{HD:STA}$</td><td>Start condition hold time</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>t_{LOW}</td><td>SCL low-level width period</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>t_{HIGH}</td><td>SCL high-level width period</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>$t_{SU:STA}$</td><td>Start condition setup time</td><td>IICB0WL / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>$t_{SU:STO}$</td><td>Stop condition setup time</td><td>IICB0WH / PCLK</td><td>IICB0WH / PCLK</td></tr>
<tr><td>t_{BUF}</td><td>Bus free time (interval between stop condition and start condition)</td><td>IICB0WL / PCLK</td><td>IICB0WL / PCLK</td></tr>
<tr><td>$t_{HD:DAT}$</td><td>Data hold time</td><td>IICB0WL[9:2] / PCLK</td><td>IICB0WL[9:2] / PCLK</td></tr>
</table>

</td></tr>
</table>

No.2-34 21.6.1 Single Transfer Mode, (3) Example of communications in single transfer mode (slave reception)

Unnecessary bit was deleted from <5> Data reception completion processing.

V2.00		V3.00	
Page	Description	Page	Revised Description
21-42	**[<5> Data reception completion processing]** <5> Data reception completion processing ・ Set the IICBnCTL0.IICBnSLWT bit to 1 and the IICBnCTL0.IICBnSLAC bit to 0. ・ Next, exit the wait state by setting the IICBnTRG.IICBnWRET bit (to 1). The end of the data is notified to the transmitting device without outputting ACK.	21-42	**[<5> Data reception completion processing]** <5> Data reception completion processing ・ Set the IICBnCTL0.IICBnSLAC bit to 0. ・ Next, exit the wait state by setting the IICBnTRG.IICBnWRET bit (to 1). The end of the data is notified to the transmitting device without outputting ACK.

No.2-35 25.7 System Protect Command Register (SYSPCMD) Supplementary information was added to

V2.00		V3.00	
Page	Description	Page	Revised Description
25-7	**[25.7 System Protect Command Register (SYSPCMD)]** **Cautions 1. The registers cannot be written in steps <1>, <2>, and <3>.** **2. Be sure to clear this bit to 0 after the completion of writing to an applicable register.**	25-7	**[25.7 System Protect Command Register (SYSPCMD)]** **Cautions 1. The registers cannot be written in steps <1>, <2>, and <3>.** **2. Be sure to clear this bit to 0 (setting for protection) after the completion of writing to an applicable register.**

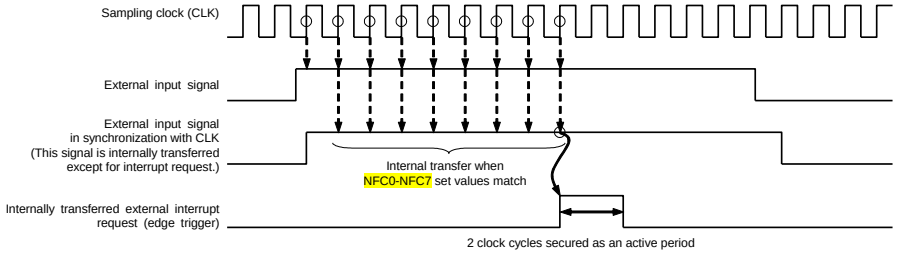
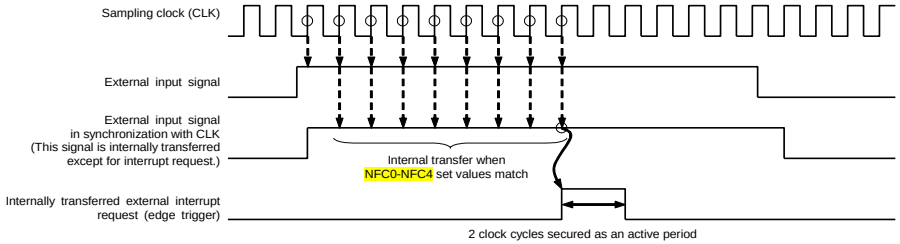
No.2-36 25.11.1 Noise Filter Configuration Registers (NFC0 to NFC4)

Errors in the cautions were corrected (NFC0-NFC3 → NFC0-NFC4).

V2.00		V3.00	
Page	Description	Page	Revised Description
25-18	**[25.11.1 Noise Filter Configuration Registers (NFC0 to NFC4)]** These registers are used to set a noise elimination level of the input signals shown in 0. **Cautions 1. When the input pulse width = NFC0-NFC3 setting value to (NFC0-NFC3 setting value – 1), whether to detect the signal as a valid signal or eliminate it as noise is undefined.** **2. Interrupt input signals (INTPZ0 to INTPZ28 and NMIZ) and LED output signals of the gigabit Ethernet PHY are transferred through the edge specification circuit, but alternative functions other than interrupts are not transferred through the edge specification circuit. Effective edges of timer array unit input pins are specified by the timer array unit edge specification register. No edge specification function is provided for the RXD0 and RXD1 input signals.** **3. When NFC0 to NFC3 registers are modified, an unintended interrupt may be generated in each register. Modify these registers in the Disable IRQ state, and then clear the corresponding interrupt pending bit.**	25-18	**[25.11.1 Noise Filter Configuration Registers (NFC0 to NFC4)]** These registers are used to set a noise elimination level of the input signals shown in Table 25.1. **Cautions 1. When the input pulse width = NFC0-NFC4 setting value to (NFC0-NFC4 setting value – 1), whether to detect the signal as a valid signal or eliminate it as noise is undefined.** **2. Interrupt input signals (INTPZ0 to INTPZ28 and NMIZ) and LED output signals of the gigabit Ethernet PHY are transferred through the edge specification circuit, but alternative functions other than interrupts are not transferred through the edge specification circuit. Effective edges of timer array unit input pins are specified by the timer array unit edge specification register. No edge specification function is provided for the RXD0 and RXD1 input signals.** **3. When NFC0 to NFC4 registers are modified, an unintended interrupt may be generated in each register. Modify these registers in the Disable IRQ state, and then clear the corresponding interrupt pending bit.**

No.2-37 25.11.2 Noise Filter Operation

Errors in the description and Figure 25.2 were corrected (NFC0 to NFC3 → NFC0 to NFC4).

V2.00		V3.00	
Page	Description	Page	Revised Description
25-23	**[25.11.2 Noise Filter Operation]** Input signals listed in Table 25.1 are sampled with the clock of the same frequency as the internal bus clock HCLK, and their noise is eliminated as specified by the noise filter configuration registers (NFC0 to NFC3). Because this sampling clock does not stop in standby mode, external interrupts NMI and INTPZ0 to INTPZ28 can be de-asserted from standby mode. In addition, for external interrupts INTPZ0 to INTPZ28, rising edges, falling edges, both edges, or low active level can be selected as effective triggers.  Figure 25.2 Operation of Digital Noise Filter for Interrupt Signals (Edge Trigger)	25-23	**[25.11.2 Noise Filter Operation]** Input signals listed in Table 25.1 are sampled with the clock of the same frequency as the internal bus clock HCLK, and their noise is eliminated as specified by the noise filter configuration registers (NFC0 to NFC4). Because this sampling clock does not stop in standby mode, external interrupts NMI and INTPZ0 to INTPZ28 can be de-asserted from standby mode. In addition, for external interrupts INTPZ0 to INTPZ28, rising edges, falling edges, both edges, or low active level can be selected as effective triggers.  Figure 25.2 Operation of Digital Noise Filter for Interrupt Signals (Edge Trigger)

No.2-38 26. Debugging

The recommended in-circuit emulator (ICE), modified

V2.00		V3.00	
Page	Description	Page	Revised Description
26-1	**[26. Debugging]** The recommended in-circuit emulators (ICE) to be connected to an R-IN32M4 are: I-jet (without trace feature) and JTAGjet (with trace feature) from IAR Systems, and adviceLUNA from Yokogawa Digital Computer Corporation.	26-1	**[26. Debugging]** The recommended in-circuit emulators (ICE) to be connected to an R-IN32M4 are: I-jet (without trace feature) and JTAGjet (with trace feature) from IAR Systems, and adviceLUNA II from DTS INSIGHT Corporation.

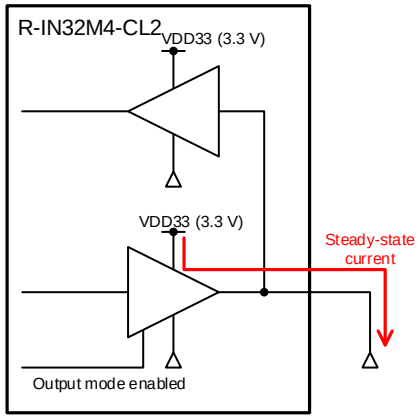
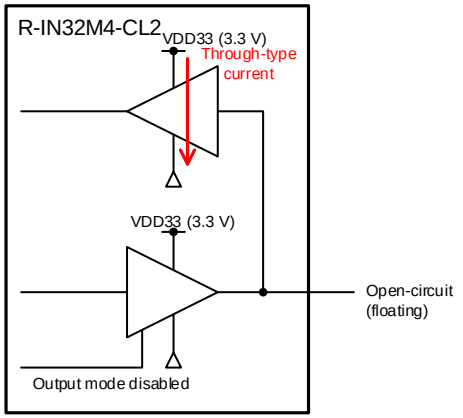
No.3-1 7. Guide to Thermal Design

Chapter title and section structure were modified.

V1.00		V2.00	
Page	Description	Page	Revised Description
22	**[7. Guide to Design]** This section describes the thermal characteristics of the R-IN32M4-CL2, and includes notes that require attention in the design of the board on which the device is mounted in terms of the dissipation of heat and the prevention of abnormal heating. Since the R-IN32M3-EC incorporates an Ethernet PHY module, large-capacity memory, and a regulator, it requires greater consideration of heat than most devices. Design the board and casing in consideration of heat dissipation.	22	**[7. Thermal Design]** This section describes the thermal characteristics of the R-IN32M4-CL2, and includes notes that require attention in the design of the board on which the device is mounted in terms of the dissipation of heat and the prevention of abnormal heating. Since the R-IN32M4-CL2 incorporates a Gigabit Ethernet PHY module and large-capacity memory, it requires greater consideration of heat than most devices. Design the board and casing in consideration of heat dissipation.

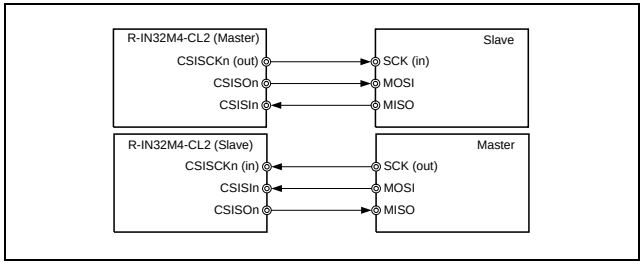
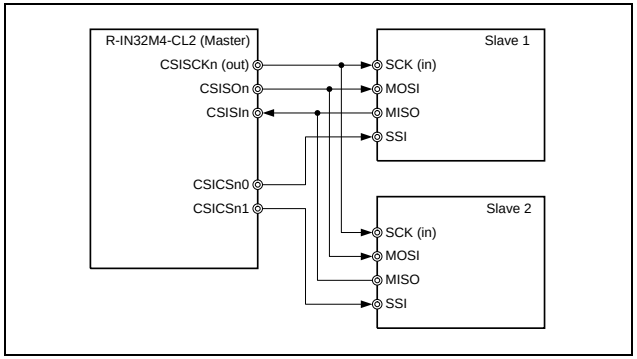
No.3-2 7.3 Notes

Complementary note was added.

V1.00		V2.00	
Page	Description	Page	Revised Description
-	N/A	30	**[7.3 Notes] Newly added** 7.3.1 Handling of Unused Pins If an unused pin is clamped to the GND or a power supply on the board, the corresponding pin must have the input attribute as a fixed setting. If it is set as an output, and the level at the point to which it is clamped is opposite that of the pin, a large steady-state current will continuously flow through the output buffer. On the other hand, if an unused pin is open-circuit on the board, the corresponding pin can have either the output attribute or the input attribute as a fixed setting, accompanied by enabling of the pull-up or pull-down resistor. Setting a pin as an input without enabling a pull-up or pull-down resistor may lead to the pin being in a floating state and the flow of a through-type current. Since the above factors lead to unnecessary heating, be sure to check the settings made by the software in these cases.  

No.3-3 15. CSIH Pins

Connection examples were added.

V1.00		V2.00	
Page	Description	Page	Revised Description
-	N/A	54	**[15. CSIH Pins]** Newly added 15. CSIH Pins Examples of connections of the R-IN32M4-CL2 with a CSI master and slave are given below. 15.1 One Master and One Slave The following figure illustrates the connections between one master and one slave.  Figure 15.1 Direct Master/Slave Connection **Remark: n = 0, 1** 15.2 One Master and Two Slaves The following figure illustrates the connections between an R-IN32M4-CL2 as a master and two slaves. In this example, the R-IN32M4-CL2 supplies one chip select (CS) signal to each of the slaves. This signal is connected to the slave select input (SSI) of the slave.  Figure 15.2 Connection between One Master and Two Slaves **Remark: n = 0, 1**

No.3-4 24. Countermeasure for Noise

Description on stopping clock output as a countermeasure for noise was added.

V1.00		V2.00	
Page	Description	Page	Revised Description
-	N/A	68	**[24. Countermeasure for Noise]** Newly added 24.1 Stopping Clock Output If the BUSCLK pin is not in use, output on the pin from the R-IN32M4-CL2 can be stopped. See section 2.2.2, Clock Control Registers (CLKGTD0, CLKGTD1) in the R-IN32M4-CL2 User's Manual: Peripheral Modules regarding control of the GCBCLK bit in the CLKGTD1 register, which enables or disables output from the BUSCLK pin.

No.4-1 3.2.1 Memory Maps

Note was added.

<table>
<tr><th colspan="2">V2.01</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>12</td><td>[Figure 3.2 Entire Memory Map]

N/A</td><td>12</td><td>[Figure 3.2 Entire Memory Map]

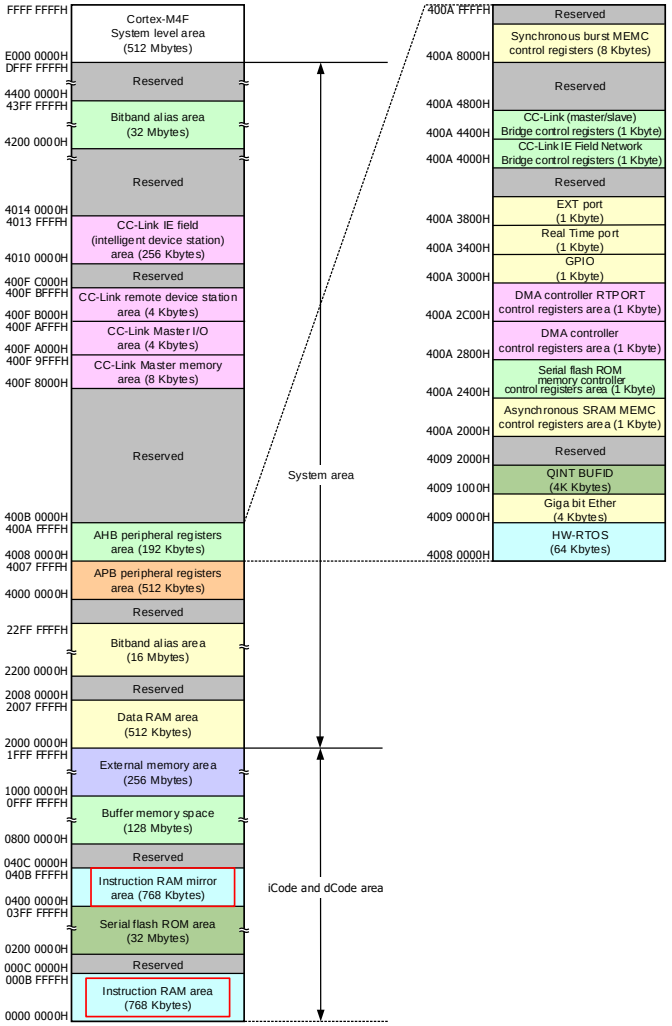
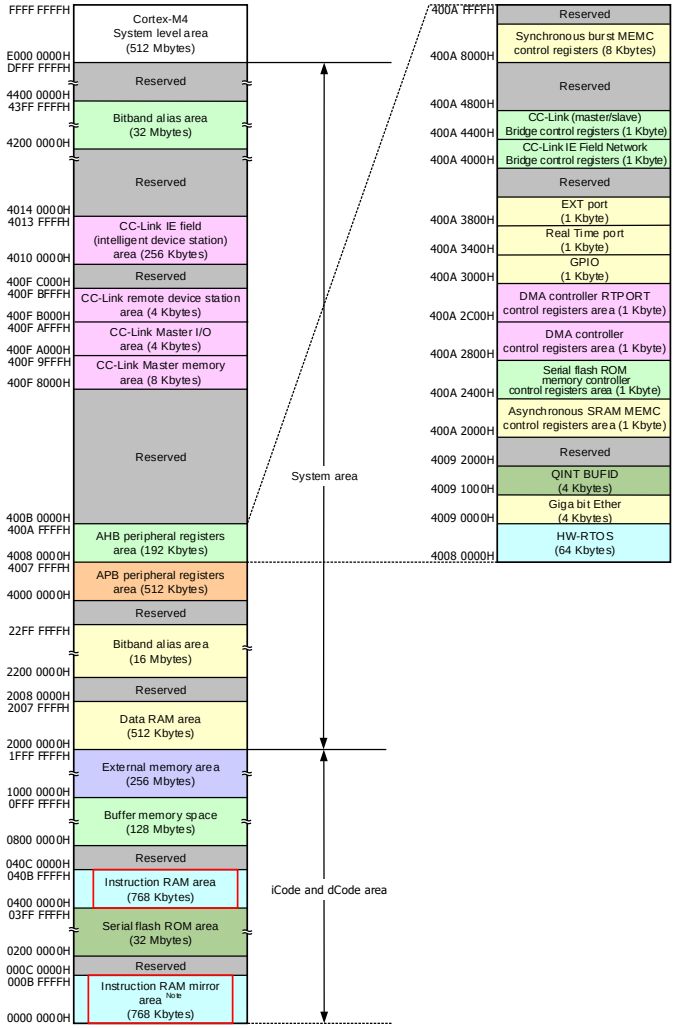
Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.</td></tr>
<tr><td>15</td><td>[Figure 3.6 External MCU Interface Space]

N/A</td><td>15</td><td>[Figure 3.6 External MCU Interface Space]

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M4-CL2 User's Manual: Peripheral Modules.
<table>
<tr><th>BOOT1</th><th>BOOT0</th><th>Boot Mode</th><th>Access Destination Area</th><th>Remarks</th></tr>
<tr><td>0</td><td>0</td><td>External memory boot</td><td>—</td><td>External MCU interface is disabled</td></tr>
<tr><td>0</td><td>1</td><td>External serial flash ROM boot</td><td>Reserved</td><td>Access disabled</td></tr>
<tr><td>1</td><td>0</td><td>External MCU boot</td><td>Instruction RAM area</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>Instruction RAM boot</td><td>Instruction RAM area</td><td>Enabled only for debugging</td></tr>
</table></td></tr>
</table>

No.4-2 3.2.1 Memory Maps

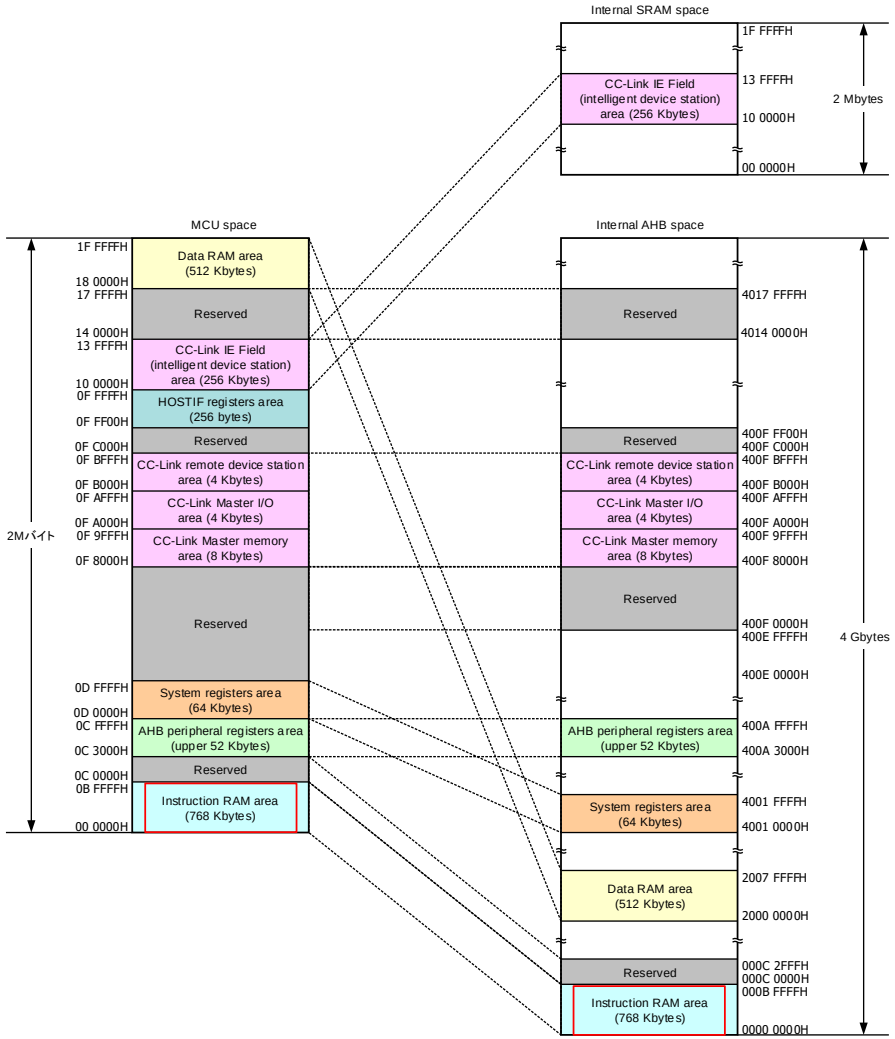
Memory areas were corrected.

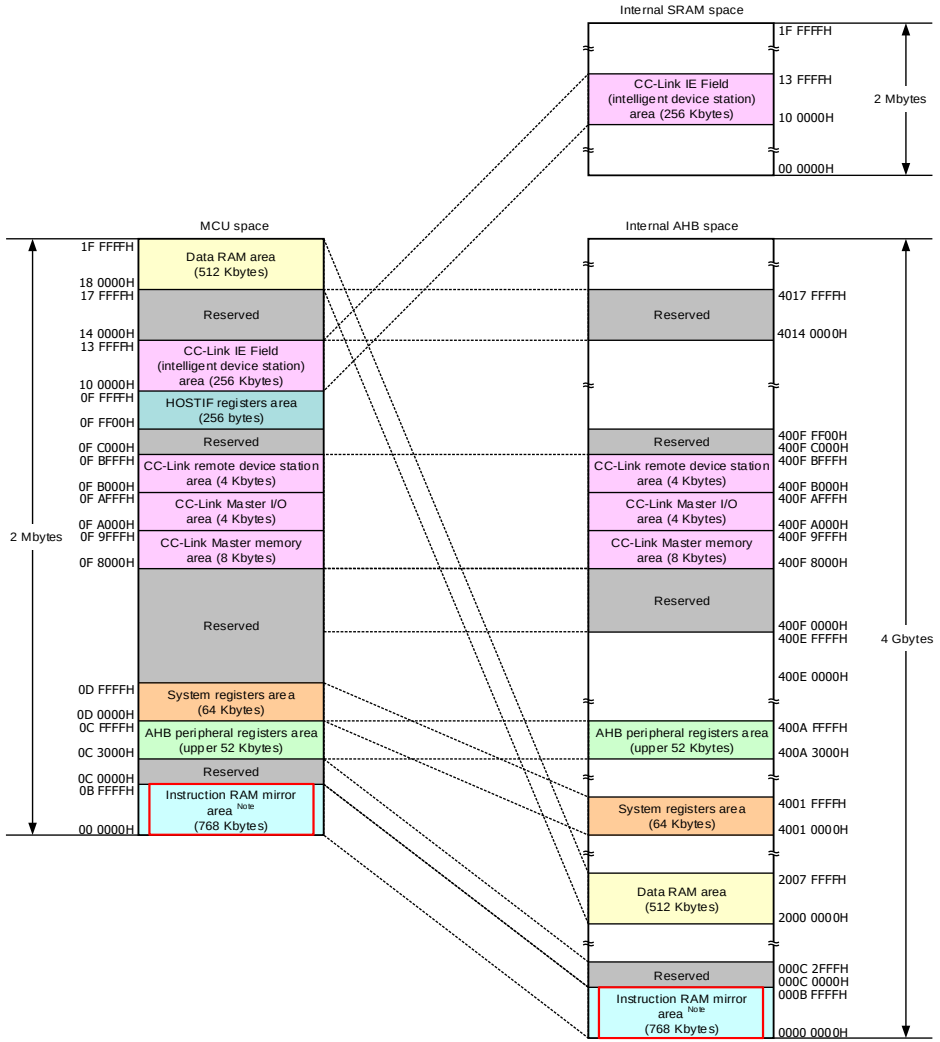
<table>
<tr><th colspan="2">V2.01</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>12</td><td>[Figure 3.2 Entire Memory Map]
 
</td><td>12</td><td>[Figure 3.2 Entire Memory Map]
 
</td></tr>
</table>

No.4-3 3.2.1 Memory Maps

Memory areas were corrected.

V2.01		V3.00	
Page	Description	Page	Revised Description
15	**[Figure 3.6 External MCU Interface Space]**	15	**[Figure 3.6 External MCU Interface Space]**





No.4-4 6.4.1 Initialization of IIC Controller

Timing setting values were modified and supplementary information was added.

<table>
<tr><th colspan="2">V2.01</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>34</td><td>[(4) Function]

This function initializes IIC of the selected channel.
ER_PARAM is returned if the selected channel is not 0 or 1.

• IIC clock setting
> Fast mode : 400kHz
• IIC timing setting
> Stop and start interval : 130 × 10 (ns)
SCL low-level width : 130 × 10 (ns)
SCL high-level width : 116 × 10 (ns)
> Setup cycles
Start condition : 116 × 10 (ns)
Stop condition : 116 × 10 (ns)
> Hold cycles
Start condition : 116 × 10 (ns)
Data : 32 × 10 (ns)

Remark: The IIC clock setting "400kHz" is based on the assumption that both the rise and fall times of SDAn and SCLn are 20 ns. Change the register settings appropriately according to your usage environment. For details, see R-IN32M4-CL2 User's Manual: Peripheral Modules.</td><td>34</td><td>[(4) Function]

This function initializes IIC of the selected channel.
ER_PARAM is returned if the selected channel is not 0 or 1.

• IIC clock setting
> Fast mode : 400kHz
• IIC timing setting
> Stop and start interval : 130 × Number of PCLK cycles (ns)
SCL low-level width : 130 × Number of PCLK cycles (ns)
SCL high-level width : 116 × Number of PCLK cycles (ns)
> Setup cycles
Start condition : 116 × Number of PCLK cycles (ns)
Stop condition : 116 × Number of PCLK cycles (ns)
> Hold cycles
Start condition : 116 × Number of PCLK cycles (ns)
Data : 32 × Number of PCLK cycles (ns)

Remarks 1. The IIC clock setting "400kHz" is based on the assumption that both the rise and fall times of SDAn and SCLn are 20 ns. Change the register settings appropriately according to your usage environment. For details, see R-IN32M4-CL2 User's Manual: Peripheral Modules.
2. The number of PCLK cycles = 10 ns.</td></tr>
</table>

No.4-5 6.5.5 Confirmation of Received Data (for Slave) Description modified

<table>
<tr><th colspan="2">V2.01</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>45</td><td>[(4) Function]

When the CSI controller is in master mode, ER_ NOTYET (no received data) is always returned because received data is not stored.
ER_PARAM is returned if the channel selection argument is not 0 or 1.
If the CSI controller is not in Tx mode, ER_INVAL (mode error) is returned.</td><td>45</td><td>[(4) Function]

When the CSI controller is in master mode, ER_ NOTYET (no received data) is always returned because received data is not stored.
ER_PARAM is returned if the channel selection argument is not 0 or 1.
If the CSI controller is not in Rx mode, ER_INVAL (mode error) is returned.</td></tr>
</table>

No.5-1 3. Specified Parts and Recommended Parts

One zener diode, added

<table>
<tr><th colspan="2">V1.01</th><th colspan="2">V1.02</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>4</td><td>[Table 3.1 Recommended Parts]

<table>
<tr><th>Product Name</th><th>Model Name^{Note1}</th><th>Manufacturer</th></tr>
<tr><td>Filter</td><td>MCT7050-A401</td><td>Sinka Japan Co.,ltd.</td></tr>
<tr><td>RS485 transceiver</td><td>SN75ALS181NS</td><td>Texas Instruments Japan, Inc.</td></tr>
<tr><td>Zener diode</td><td>RD6.2Z</td><td>Renesas Electronics.</td></tr>
</table>
</td><td>4</td><td>[Table 3.1 Recommended Parts]

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<tr><td rowspan="2">Zener diode</td><td>RD6.2Z</td><td>Renesas Electronics.</td></tr>
<tr><td>STZU6.2NT146</td><td>ROHM Co., Ltd.</td></tr>
</table>
</td></tr>
</table>

No.5-2 5. CC-Link Remote Device Station Pins

The function of the IOTENSU pin, Low fixed, was

<table>
<tr><th colspan="2">V1.01</th><th colspan="2">V1.02</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>6</td><td>[Table 5.1 Correspondence between CC-Link Remote Device Station Pins and R-IN32M3 Series Pins]
<table><tr><th>CC-Link Pin Name</th><th>R-IN32M3 Pin Name</th><th>Shared Port</th><th>Description</th></tr><tr><td>IOTENSU</td><td>CCS_IOTENSU</td><td>P22</td><td>Initial setting pin</td></tr></table></td><td>6</td><td>[Table 5.1 Correspondence between CC-Link Remote Device Station Pins and R-IN32M3 Series Pins]
<table><tr><th>CC-Link Pin Name</th><th>R-IN32M3 Pin Name</th><th>Shared Port</th><th>Description</th></tr><tr><td>IOTENSU</td><td>CCS_IOTENSU</td><td>P22</td><td>Initial setting pin (Low fixed)</td></tr></table></td></tr>
<tr><td>8</td><td>[Table 5.2 Correspondence between CC-Link Remote Device Station Pins and R-IN32M4-CL2 Pins]
<table><tr><th>CC-Link Pin Name</th><th>R-IN32M4-CL2 Pin Name</th><th>Shared Port</th><th>Description</th></tr><tr><td>IOTENSU</td><td>CCS_IOTENSU</td><td>P22</td><td>Initial setting pin</td></tr></table></td><td>8</td><td>[Table 5.2 Correspondence between CC-Link Remote Device Station Pins and R-IN32M4-CL2 Pins]
<table><tr><th>CC-Link Pin Name</th><th>R-IN32M4-CL2 Pin Name</th><th>Shared Port</th><th>Description</th></tr><tr><td>IOTENSU</td><td>CCS_IOTENSU</td><td>P22</td><td>Initial setting pin (Low fixed)</td></tr></table></td></tr>
</table>

No.5-3 6.1 Setting the Number of Occupied Stations

Caution on the IOTENSU pin, modified

V1.01		V1.02	
Page	Description	Page	Revised Description
9	**[6.1 Setting the Number of Occupied Stations]** **Caution When the IOTENSU terminal is set to "H," the number of I/O points is fixed at 32, regardless of the Number of Occupied Stations setting.**	9	**[6.1 Setting the Number of Occupied Stations]** **Caution: Fix the IOTENSU pin to the low level. Setting the pin to the high level is prohibited.**

No.5-4 14.1 Circuit Design in General, (3) Questions and Answers Related to Switches, Connectors, and Terminal Blocks

Answer updated and items added

<table>
<tr><th colspan="2">V1.01</th><th colspan="2">V1.02</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Revised Description</th></tr>
<tr><td>72</td><td>[14.1 Circuit Design in General, (3) Questions and Answers Related to Switches, Connectors, and Terminal Blocks]
<table>
<tr><th></th><th>Question</th><th>Answer</th></tr>
<tr><td>2</td><td>Regarding the setting of the station number
We are planning to fix the station number instead of using a rotary switch. Does this specification pose any problems?</td><td>Station number setting is mandatory. This is because if the customer cannot set the station number freely, it may not be possible to configure a system.
It is, however, all right to use dip switches or software processing instead of a rotary switch.</td></tr>
<tr><td>3</td><td>We want to install a communication connector (RS485) on the bottom surface of the station. Does this pose any problems? (We will make it possible to insert and remove the connector.)</td><td>It is all right to layout the connector as you like.</td></tr>
<tr><td>4</td><td>There is no specification for the external form. Can we decide the following as we like?
[1] The shape, layout, color, and size of the LEDs
[2] The type of connectors (we are considering
the use of Conbicon connectors made by Phoenix.)
[3] The size and type of rotary and dip switches (we are considering the use of S-3011A switches made by Copal.)</td><td>There is no specification for parts except the specified parts.
[1] Any design can be used for the LEDs.
[2] Use 2-piece connectors. If 2-piece connectors cannot be used, please specify in your manual that this product cannot be replaced in the link operation status (without shutting down the entire link). (Online connection and disconnection are not possible.)
[3] Any design can be used for the switches.</td></tr>
</table></td><td>72</td><td>[14.1 Circuit Design in General, (3) Questions and Answers Related to Switches, Connectors, and Terminal Blocks]
<table>
<tr><th></th><th>Question</th><th>Answer</th></tr>
<tr><td>2</td><td>Regarding the setting of the station number
We are planning to fix the station number instead of using a rotary switch. Does this specification pose any problems?</td><td>According to the CC-link standard, the station number should be freely configurable.</td></tr>
<tr><td>3</td><td>Could the station number be set by software?</td><td>There is no register to set the station number directly.
Station number is set by pin setting of "station number setting switch input terminal (CCS_STATION_NO_0-CCS_STATION_NO_7)".
When no switch is mounted, it is possible to set the station number by connecting the pins of "station number setting switch input terminal" to any general-purpose ports and setting the station number from the general-purpose port by software.
After setting the station number, the reset of CC-Link block should be released.</td></tr>
<tr><td>4</td><td>We want to install a communication connector (RS485) on the bottom surface of the station. Does this pose any problems? (We will make it possible to insert and remove the connector.)</td><td>It is all right to layout the connector as you like.</td></tr>
<tr><td>5</td><td>There is no specification for the external form. Can we decide the following as we like?
[1] The shape, layout, color, and size of the LEDs
[2] The type of connectors (we are considering
the use of Conbicon connectors made by Phoenix.)
[3] The size and type of rotary and dip switches (we are considering the use of S-3011A switches made by Copal.)</td><td>There is no specification for parts except the specified parts.
[1] Any design can be used for the LEDs.
[2] Use 2-piece connectors. If 2-piece connectors cannot be used, please specify in your manual that this product cannot be replaced in the link operation status (without shutting down the entire link). (Online connection and disconnection are not possible.)
[3] Any design can be used for the switches.</td></tr>
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</table>