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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-78K-A008B/E	Rev.	2.00
Title	Restriction regarding watchdog timer		Information Category	Technical Notification		
Applicable Product	78K0R/Fx3, 78K0/Fx2, 78K0/Fx2-L, 78K0/Kx2 (Automotive grade), 78K0/Kx2-L (Automotive grade), 78K0/Dx2, MCP products including 78K0/Kx2 (Automotive grade)	Lot No. –	Reference Document	Latest user's Manual of applicable products		

The restriction below applies to watchdog timer in the above mentioned Applicable Products.

78K0/Fx2, 78K0/Fx2-L, 78K0/Kx2 (Automotive grade), 78K0/Kx2-L (Automotive grade), 78K0/Dx2, and MCP products including 78K0/Kx2 (Automotive grade) are applicable to Restriction2 only.

1. Restriction1 watchdog timer window function

Wrong WDT-RESET may assert when WDT counter is cleared (writing ACh to WDTE register) at just 50% of count-overflow-value and when window open period of watchdog timer is set to 75%.

1.1 Applicable products

applicable product	78K0R/Fx3

1.2 Conditions

If following all conditions is established, customer's software is applicable to the restriction.

(1) "Operation of watchdog timer" is "enabled" (WDTON in User option byte = "1")

(2) "Operation of watchdog timer in the HALT or STOP mode" is "enabled" (WDSTBYON in User option byte = "1")

(3) "Setting of window open period of watchdog timer" is "75%" (WINDOW1, WINDOW0 in User option byte = "10b")

(4) During watchdog timer operates, counter is cleared at just 50% of count-overflow-value.

1.3 Countermeasure

Please apply any of the following measures.

Countermeasure1: Set "window open period" to "50%" or "100%".

Countermeasure2: If "window open period" is set to "75%", please perform Counter-clear with the period other than 50% counter value.

2. Restriction2 watchdog timer window function

WDT-RESET may not occur when "25%" is specified as "window open period" and when WDT counter is cleared at just 50% of count-overflow-value.

2.1 Applicable products

applicable products	78K0R/Fx3, 78K0/Fx2, 78K0/Fx2-L, 78K0/Kx2 (Automotive grade), 78K0/Kx2-L (Automotive grade), 78K0/Dx2, MCP products including 78K0/Kx2 (Automotive grade)

2.2 Conditions

If following all conditions is established, customer's software is applicable to the restriction.

(1) "Operation of watchdog timer" is "enabled" (WDTON in User option byte = "1")

(2) "Operation of watchdog timer in the HALT or STOP mode" is "enabled" (WDSTBYON in User option byte = "1") *1

(3) "Setting of window open period of watchdog timer" is "25%" (WINDOW1, WINDOW0 in User option byte = "00b")

(4) During watchdog timer operates, counter is cleared at just 50% of count-overflow-value.

*1: There is not this function in case of 78K0 products.

2.3 Countermeasure

Set "window open period" to "50%" or "75%" or "100%".

Note

- Each bits (WDTON, WDSTBYON, WINDOW1, and WINDOW0) is allocated in user option byte.
  78K0R/Fx3: It is allocated in user option byte (000C0h)
  78K0/Fx2, 78K0/Fx2-L, 78K0/Kx2 (Automotive grade), 78K0/Kx2-L (Automotive grade), 78K0/Dx2, MCP products including 78K0/Kx2 (Automotive grade): It is allocated in user option byte (0080h). There is not a function of WDTSTBYON bit.
- Set the same value as the following to each user option byte.
  78K0R/Fx3: 000C0h => 020C0h.
  78K0/Fx2, 78K0/Fx2-L, 78K0/Kx2 (Automotive grade), 78K0/Kx2-L (Automotive grade), 78K0/Dx2, MCP products including 78K0/Kx2 (Automotive grade): 0080h => 1080h.
- Products including 78K0/Kx2 (Automotive grade) is shown below.
  UPD78F8014A, UPD78F8015A, UPD78F8016A, UPD78F8017A, UPD78F8018A, UPD78F8019A, UPD78F8020A, UPD78F8020DA, UPD78F8026, UPD78F8027, UPD78F8028, UPD78F8029, UPD78F8030, UPD78F8032D, UPD78F8033, UPD78F8034, UPD78F8035, UPD78F8036, UPD78F8037, UPD78F8039D, UPD78F8071, UPD78F8072, UPD78F8073, UPD78F8074, UPD78F8075, UPD78F8077D