Microcomputer Technical Information

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QB-V850ESKX1H In-Circuit Emulator for V850ES/KE1, V850ES/KF1, V850ES/KG1, V850ES/KJ1, V850ES/KE1+, V850ES/KF1+, V850ES/KG1+, V850ES/KJ1+ Usage Restrictions		Document No.	ZBG-CD-05-0080		1/3
		Date issued	September 28, 2005		
		Issued by	Development Tool Group Multipurpose Microcomputer Systems Division 4th Systems Operations Unit NEC Electronics Corporation		
Related documents	QB-V850ESKX1H User's Manual: U17214EJ2V0 QB-V850ESKX1H (Control Code: A, B, C) Operating Precautions: ZUD-CD-05-0063	Notification classification	√	Usage restriction	
				Upgrade	
				Document modification	
				Other notification	

1. Target product

Product	Control Code[Note]	Remark
QB-V850ESKX1H-xxx-yyy	A, B, C	xxx and yyy are arbitrary codes.

Note For the identification method for the control code, see the Operating Precautions supplied with the product.

2. New restrictions

Restrictions No. 14 to No. 16 have been added. See the attachment for details.

No. 14 Fail-safe break function does not operate

No. 15 Illegal break occurs during program execution in internal RAM (2)

No. 16 Address is not retained during external bus access

The erroneous description on restriction No. 5 has been corrected. After correction, regard one of the restriction conditions as a permanent restriction.

- Corrected item: No. 5 Bug in program execution and DMA transfer in internal RAM
- Before correction:

[Description]

When a DMA transfer for the internal RAM and a bit manipulation instruction (SET1, CLR1, or NOT1) allocated in the internal RAM or a data access instruction for a misaligned address are executed simultaneously, the CPU may deadlock due to conflict between the internal bus operations. At this time, only a reset can be acknowledged. (An NMI or interrupt cannot be acknowledged.)

[Workaround]

Implement any of the following workarounds.

- Do not perform a DMA transfer for the internal RAM when an instruction allocated in the internal RAM is being executed.

- Do not execute an instruction allocated in the internal RAM when a DMA transfer for the internal RAM is being performed.

This bug has been corrected in control code B or later.

- After correction:

[Description]

When a DMA transfer for the internal RAM and an instruction of (1) or (2) described below are executed simultaneously, the CPU may deadlock due to conflict between the internal bus operations. At this time, only a reset can be acknowledged. (An NMI or interrupt cannot be acknowledged.)

(1) A bit manipulation instruction (SET1, CLR1, or NOT1) allocated in the internal RAM

(2) A data access instruction for a misaligned address allocated in the internal RAM

[Workaround]

Implement either of the following workarounds.

(1) For a bit manipulation instruction (SET1, CLR1, or NOT1) allocated in the internal RAM

- Do not perform a DMA transfer for the internal RAM when a bit manipulation instruction allocated in the internal RAM is being executed.
- Do not execute a bit manipulation instruction allocated in the internal RAM when a DMA transfer for the internal RAM is being performed.

This restriction has been corrected in control code B or later.

(2) For a data access instruction for a misaligned address allocated in the internal RAM

- Do not perform a DMA transfer for the internal RAM when a data access instruction for a misaligned address allocated in the internal RAM is being executed.
- Do not execute a data access instruction for a misaligned address allocated in the internal RAM when a DMA transfer for the internal RAM is being performed.

Please regard this item as a permanent restriction.

3. Workarounds

See the attachment for details on workarounds for restrictions added in this edition.

4. Modification schedule

No. 14 This restriction has been corrected in control code C or later.

No. 15 This item is not planned for correction. Please regard this item as a permanent restriction.

No. 16 This restriction will be corrected by upgrading the device file according to the following schedule.

DF703218 V2.01 (next version):	September 30, 2005
DF703318 V1.01 (next version):	Early October, 2005

* Note that this schedule is subject to change without notice. For the detailed release schedule of the modified products, contact an NEC Electronics sales representative.

5. List of restrictions

See the attachment for details.

6. Addition of supported devices

The devices described below are now supported by the QB-V850ESKX1H.

The use of the newly supported devices will be added to the next revision (3rd edition) of the “QB-V850ESKX1H User’s Manual (U17214E)”.

- Devices newly supported by QB-V850ESKX1H:

  V850ES/KE2, V850ES/KF2, V850ES/KG2, V850ES/KJ2

- QB-V850ESKX1H User’s Manual:

  Revision schedule: October 7, 2005

  Document title: QB-V850ESKX1H User’s Manual

  Document number: U17214EJ3V0

7. Document revision history

QB-V850ESKX1H In-Circuit Emulator for V850ES/KE1, V850ES/KF1, V850ES/KG1, V850ES/KJ1, V850ES/KE1+, V850ES/KF1+, V850ES/KG1+, V850ES/KJ1+ Usage Restrictions

Document Number	Issued on	Description
ZBG-CD-04-0062	September 10, 2004	Newly created.
ZBG-CD-05-0044	May 20, 2005	Addition of restrictions No. 12 and No. 13
ZBG-CD-05-0080	September 28, 2005	Addition of restrictions No. 14 to No. 16 Correction of erroneous description in No. 5 Addition of supported devices

Notes on Using QB-V850ESKX1H

This document describes restrictions applicable only to the emulator and restrictions that are planned for correction in the emulator.

Refer to the following documents for the restrictions in the target device.

- User's manual of target device
- Restrictions notification document for target device

Also refer to the user's manual of the emulator for cautions on using the emulator.

1. Product Version

Control Code[Note]	Remark
A	–
B	Version in which bugs No. 1 to No. 6 in control code A are corrected
C	Version in which bugs No. 12 and No. 14 in control code B are corrected

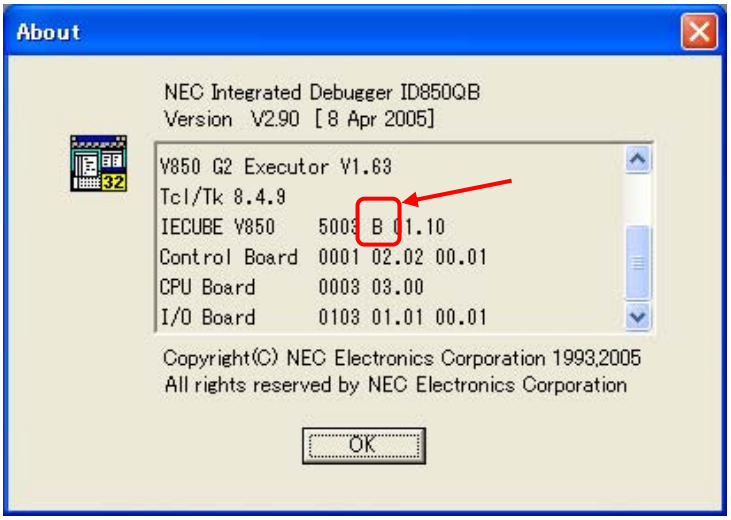
Note The “control code” is the second digit from the left in the 10-digit serial number printed on the sticker attached to the bottom side of IECUBE (if it has not been upgraded).

If the product has not been upgraded, the control code can also be checked with the following methods while the debugger is running.

- When using ID850QB

  Click the [Help] menu and then click the About submenu to display the About dialog box.

  “X” in “IECUBE V850 **** X **.**” is the control code.



- When using Green Hills Software (GHS)’s debugger MULTI®

  Execute the version command of 850eserv.

  “X” in “IECUBE Control Code=X” is the control code.

```
850eserv Version: 3.2342 (for MULTI V4.0.x)
IE type=NU85E Full ICE Generation 2 (IECUBE)
Executor Version=V850 G2 Executor V1.63  Copyright 2004
Device File Format Version=V2.18
Device File File Version=V2.10
IECUBE Control Code=B
IECUBE Firmware Version=V1.10
Control Board Version=V2.02 (FPGA Version=0.01)
CPU Board Version=V3.00
I/O Board Version=V1.01 (FPGA Version=0.01)
```

2. Product History

No.	Bugs and Changes/Additions to Specifications		Control Code		
			A	B	C
1	Restriction on pin status in bus hold or IDLE/STOP mode		×	√	√
2	Restriction on current flowing upon power application		×	√	√
3	Restriction on A/D conversion with $AV_{REF0} \leq 4.0$ V		×	√	√
4	Bug related to DMA transfer forcible termination		×	√	√
5	Bug in program execution and DMA transfer in internal RAM	(1) Bit manipulation instruction	×	√	√
		(2) Access for misaligned address	Permanent restriction		
6	Restriction on read access for buffer RAM of CSIA		×	√	√
7	Emulator hangs up while downloading data or setting software break		Avoidable by debugger upgrade		
8	Data loss occurs when external RAM is connected		Avoidable by debugger upgrade		
9	Restriction on option byte emulation		Avoidable by debugger upgrade		
10	Illegal break occurs during program execution in internal RAM (1)		Permanent restriction		
11	Restriction on power-on-clear circuit, low-voltage detector, and clock monitor		Permanent restriction		
12	Restriction related to current flowing from REGC pin		×	×	√
13	Restriction related to overflow reset of watchdog timer 1		Permanent restriction		
14	Fail-safe break function does not operate		×	×	√
15	Illegal break occurs during program execution in internal RAM (2)		Permanent restriction		
16	Address is not retained during external bus access		Avoidable by debugger upgrade		

×: Applicable, √: Not applicable or already corrected

3. Details of Bugs and Added Specifications

No. 1 Restriction on pin status in bus hold or IDLE/STOP mode

[Description]

The pin status is illegal in the following cases (a) and (b).

(a) When the following pins are used as output ports, the pins go into the high-impedance state in bus hold or IDLE/STOP mode (normally the pin status should be retained)

- PCT2, PCT3, PCT5, PCT7
- PCM0 to PCM5
- PCD0 to PCD3

(b) The pin status in the emulator differs from that in the target device when the external bus control pin is used in bus hold or IDLE/STOP mode (shaded portions).

Operating Status / Pin	Operation of Target Device		Operation of Emulator	
	IDLE Mode/ STOP Mode	Bus Hold	IDLE Mode/ STOP Mode	Bus Hold
AD0 to AD15 (PDL0 to PDL15)	Hi-Z	Hi-Z	Hi-Z	Hi-Z
A0 to A15 (P90 to P915)	Hi-Z	Hi-Z	Hi-Z	Hi-Z
A16 to A23 (PDH0 to PDH7)	Hi-Z	Hi-Z	**Retained**	**Retained**
WAIT (PCM0)	–	–	–	–
CLKOUT (PCM1)	L	Operates	**Hi-Z**	**Hi-Z**
CS0 to CS3 (PCS0 to PCS3)	H	Hi-Z	**Hi-Z**	Hi-Z
WR0, WR1 (PCT0, PCT1)	H	Hi-Z	**Hi-Z**	Hi-Z
RD (PCT4)	H	Hi-Z	**Hi-Z**	Hi-Z
ASTB (PCT6)	H	Hi-Z	**Hi-Z**	Hi-Z
HLDAK (PCM2)	H	L	**Hi-Z**	**Hi-Z**
HLDRQ (PCM3)	–	Operates	–	Operates

[Workaround]

There is no workaround.

This restriction has been corrected in control code B or later.

No. 2 Restriction on current flowing upon power application

[Description]

The pins shown below are pulled up to 5 V via a 33 kΩ resistor for approx. 0.3 seconds after power is applied to the emulator (normally they should be in the high-impedance state).

As a result, a current of approx. 0.15 mA per pin flows into the target system during this period.

- PCD0 to PCD3
- PCM0 to PCM5
- PCS0 to PCS7
- PCT0 to PCT7
- PDH0 to PDH7
- PDL0 to PDL15

[Workaround]

There is no workaround.

This restriction has been corrected in control code B or later.

No. 3 Restriction on A/D conversion with $AV_{REF0} \leq 4.0$ V

[Description]

A/D conversion may not be performed normally when the product is used with $V_{DD} = AV_{REF0} \leq 4.0$ V.

[Workaround]

Use the product with $V_{DD} = AV_{REF0} > 4.0$ V.

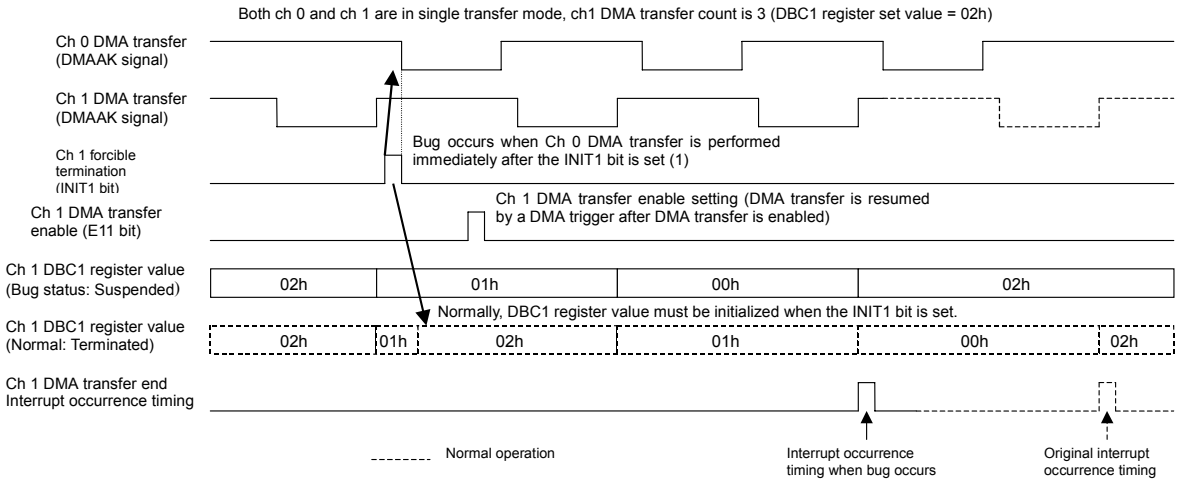
This restriction has been corrected in control code B or later.

No. 4 Bug related to DMA transfer forcible termination

[Description]

When terminating a DMA transfer by setting the INITn bit of the DCHCn register, the transfer may not be terminated, but just suspended, even though the INITn bit is set (1). As a result, when the DMA transfer of a channel that should have been terminated is resumed, the DMA transfer will terminate after an unexpected number of transfers are completed and a DMA transfer completion interrupt may occur (n = 0 to 3). This bug occurs if a DMA transfer is executed immediately after a forcible termination is set (by setting the INITn bit) (see the figure below).

This bug does not depend on the number of transfer channels, transfer type (2-cycle or flyby), transfer target (between memory and memory, memory and I/O; including internal resources), transfer mode (single, single-step, or block), or trigger (external request, interrupt from internal peripheral I/O, or software), and can occur with any combination of the above elements that can be set under the specifications. In addition, another channel may affect the occurrence of this bug.



The following registers are buffer registers with a 2-stage FIFO configuration of master and slave. If these registers are overwritten during a DMA transfer or in the DMA-suspended status, the value is written to the master register, and reflected in the slave register when the DMA transfer of the overwritten channel is terminated.

The “initialization” in the above figure means that the contents of the master register are reflected in the slave register.

2-stage FIFO configuration registers (n = 0 to 3):

- DMA source address register (DSAnH, DSAnL)
- DMA destination address register (DDAnH, DDAnL)
- DMA transfer count register (DBCn)

[Workaround]

This bug can be avoided by implementing any of the following procedures using the software.

(1) Stop all the transfers from DMA channels temporarily (n = 0 to 3)

The following measure is effective if the following condition is satisfied.

- Except for the following workaround processing, the program does not assume that the TCn bit of the DCHCn register is 1. (Since the TCn bit of the DCHCn register is cleared (0) when it is read, execution of the following procedure (b) under <5> clears this bit.)

[Procedure to avoid bug]

<1> Disable interrupts (DI state).

<2> Read the DMA restart register (DRST) and transfer the ENn bit of each channel to a general-purpose register (value A).

<3> Write 00H to the DMA restart register (DRST) twice[Note].
By executing twice[Note], the DMA transfer is definitely stopped before proceeding to <4>.

<4> Set (1) the INITn bit of the DCHCn register of the channel that should be terminated forcibly.

<5> Perform the following operations for value A read in <2>. (Value B)

(a) Clear (0) the bit of the channel that should be terminated forcibly

(b) If the TCn and ENn bits of the channel that is not terminated forcibly are 1 (AND makes 1), clear (0) the bit of the channel.

<6> Write value B in <5> to the DRST register.

<7> Enable interrupts (EI state).

Note Execute three times if the transfer target (transfer source or transfer destination) is the internal RAM.

Remark Be sure to execute <5> to prevent the ENn bit from being set illegally for channels that are terminated normally during the period of <2> and<3>.

(2) Repeat setting the INITn bit until the forcible DMA transfer termination is correctly performed (n = 0 to 3)

[Procedure to avoid bug]

<1> Copy the initial transfer count of the channel that should be terminated forcibly to a general-purpose register.

<2> Set (1) the INITn bit of the DCHCn register of the channel that should be terminated forcibly.

<3> Read the value of the DMA transfer count register (DBCn) of the channel that should be terminated forcibly and compare the value with the one copied in <1>. If the values do not match, repeat <2> and <3>.

Remarks 1. When the DBCn register is read in procedure <3>, the remaining transfer count will be read if the DMA is stopped due to this bug. If the forcible DMA termination is performed correctly, the initial transfer count will be read.

2. Note that it may take some time for forcible termination to take effect if this workaround is implemented in an application in which DMA transfers other than for channels subject to forcible termination are frequently performed.

This bug has been corrected in control code B or later.

No. 5 Bug in program execution and DMA transfer in internal RAM

[Description]

When a DMA transfer for the internal RAM and a bit manipulation instruction (SET1, CLR1, or NOT1) allocated in the internal RAM or a data access instruction for a misaligned address are executed simultaneously, the CPU may deadlock due to conflict between the internal bus operations. At this time, only a reset can be acknowledged. (An NMI or interrupt cannot be acknowledged.)

[Workaround]

Implement either of the following workarounds.

(1) For a bit manipulation instruction (SET1, CLR1, or NOT1) allocated in the internal RAM

- Do not perform a DMA transfer for the internal RAM when a bit manipulation instruction allocated in the internal RAM is being executed.
- Do not execute a bit manipulation instruction allocated in the internal RAM when a DMA transfer for the internal RAM is being performed.

This restriction has been corrected in control code B or later.

(2) For a data access instruction for a misaligned address allocated in the internal RAM

- Do not perform a DMA transfer for the internal RAM when a data access instruction for a misaligned address allocated in the internal RAM is being executed.
- Do not execute a data access instruction for a misaligned address allocated in the internal RAM when a DMA transfer for the internal RAM is being performed.

Please regard this item as a permanent restriction.

No. 6 Restriction on read access for buffer RAM of CSIA

[Description]

Read access for the buffer RAM (CSIAnBm) of clocked serial interface with automatic transmit/receive function A (CSIA) cannot be performed normally.

When performed, illegal data is read.

Write access can be performed normally.

Therefore, automatic transfer mode cannot be used for reception.

Automatic transfer mode can be used for transmission, but read access for transmit data cannot be performed. (n = 0 or 1, m = 0 to F)

[Workaround]

Use 1-byte transfer mode for reception.

Also use 1-byte transfer mode when performing transmission and the reading the transmit data.

This restriction has been corrected in control code B or later.

No. 7 Emulator hangs up while downloading data or setting software break

[Description]

The emulator may hang up if the WAIT pin or HLDRQ pin is at the active level while data is being downloaded to the internal ROM area or a software break is set to the internal ROM area.

[Workaround]

If the WAIT and HLDRQ pins are not used, mask the WAIT and HLDRQ pins using the pin mask function of the debugger.

If the WAIT and HLDRQ pins are used, do not make these pins active while data is being downloaded to the internal ROM area or a software break is set to the internal ROM area.

This restriction can be avoided by upgrading the debugger to the following version.

- When using ID850QB: Use V2.81 or later.
- When using MULTI: Use in combination with EXEC V1.57 or later.

No. 8 Data loss occurs when external RAM is connected

[Description]

A write cycle to the external bus is generated when downloading data to the internal ROM is executed or a software break is set to the internal ROM. Therefore, if RAM is connected to the target system, data in the RAM may be lost.

[Workaround]

There is no workaround if the bug occurs as a result of downloading data to the internal ROM. However, it does not cause any problem if the internal RAM values are initialized by program execution after download (all the values in the RAM are overwritten), because the lost data is overwritten by normal values.

If the bug occurs as a result of setting a software break to the internal ROM, do not use a software break for the internal ROM space; use a hardware break instead.

This restriction can be avoided by upgrading the debugger to the following version.

- When using ID850QB: Use V2.81 or later.
- When using MULTI: Use in combination with EXEC V1.57 or later.

No. 9 Restriction on option byte emulation

[Description]

The option byte function cannot be emulated.

The emulator ignores data at address 0x7A and operates in the same way as when address 0x7A is set to 0x00. Therefore, the emulator always operates in the following mode.

- Internal oscillation clock: Can be stopped by software
- Oscillation stabilization time: Shortened (initial value of OSTS register: 00H)

[Workaround]

There is no workaround.

This restriction can be avoided by upgrading the debugger to the following version.

- When using ID850QB: Use V2.81 or later.
- When using MULTI: Use in combination with EXEC V1.57 or later.

No. 10 Illegal break occurs during program execution in internal RAM

[Description]

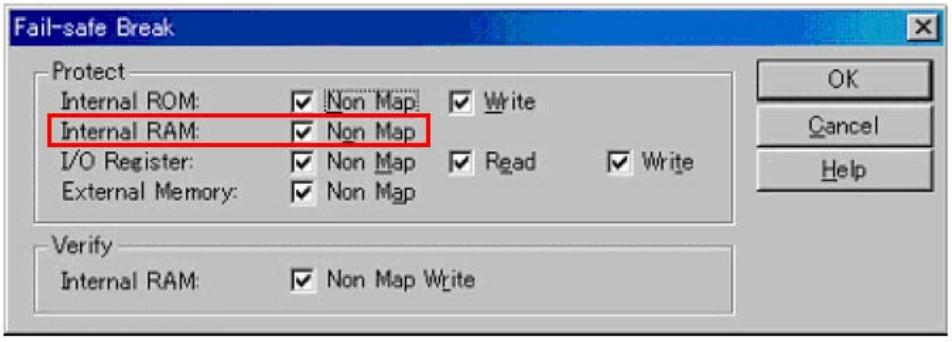
An illegal break may occur when a peripheral I/O register is accessed during program execution in the internal RAM.

[Workaround]

Cancel the fail-safe break setting for the internal RAM in the debugger.

- When using ID850QB

  Click the [Detail] button in the Fail-safe Break field in the Configuration window and clear the check box for “Internal RAM”.



- When using MULTI

  Cancel the fail-safe break for “ramgrd” and “ramgrdv” using the *Target flsf* command.

Please regard this item as a permanent restriction.

No. 11 Restriction on power-on-clear circuit, low-voltage detector, and clock monitor

[Description]

The power-on-clear circuit, low-voltage detector, and clock monitor cannot be emulated. Writing to the control registers is possible, but no reset or interrupt occurs. In addition, the CLMRF and LVIRF flags of the reset source flag register (RESF) do not change.

[Workaround]

There is no workaround.

Please regard this item as a permanent restriction.

No. 12 Restriction related to current flowing from REGC pin

[Description]

A 5.5 V current is output from the emulator's REGC pin to the target system.

When the REGC pin is connected to a power supply pin (such as VDD or EVDD) on the target system, a current flows into the power supply on the target system side. Consequently, TARGET LED on the emulator is lit even if the power supply to the target system is off.

[Workaround]

There is no workaround.

This restriction has been corrected in control code C or later.

No. 13 Restriction related to overflow reset of watchdog timer 1

[Description]

The reset operation varies as described below when watchdog timer 1 is used in watchdog timer mode 2 (mode in which the reset operation WDTRES1 is started upon the occurrence of an overflow) and an overflow occurs.

- When the target device is the V850ES/Kx1+

  It takes approximately 2.2 seconds ($2^{19}/f_R$) from when the reset of watchdog timer 1 is released until the program starts. In normal operation, the program starts immediately after the reset release.

  Both bit 4 (WDT2RF) and bit 7 (WDTRF1) of the reset source flag register (RESF) are set after the reset release. In normal operation, only bit 7 of RESF is set.

- When the target device is the V850ES/Kx1

  It takes approximately 6.7 seconds ($2^{25}/f_X$, f_X = 5 MHz) from when the reset of watchdog timer 1 is released until the program starts. In normal operation, the program starts immediately after the reset release.

  fx: Main clock oscillation frequency

  f_R: Internal oscillation clock frequency

[Workaround]

There is no workaround.

Please regard this item as a permanent restriction.

No. 14 Fail-safe break function does not operate

[Description]

The fail-safe break function does not operate for the following operations.

- Peripheral I/O register
  - Read or write to a peripheral I/O register that does not exist
  - Write to a read-only peripheral I/O register
  - Read to a write-only peripheral I/O register

- External memory area
  - Fetch from or access to an unmapped area
  - Write to ROM area

[Workaround]

There is no workaround.

This restriction has been corrected in control code C or later.

No. 15 Illegal break occurs during program execution in internal RAM (2)

[Description]

A non-map break occurs if all of the following conditions are satisfied, even if the program itself is correct.

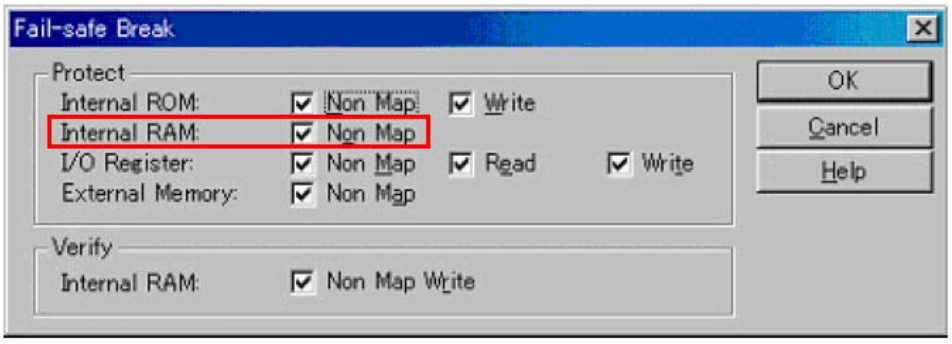
- A program is executed in the internal RAM area.
- Data access for the internal RAM area is performed twice in succession.
- An execution branches to the internal ROM area using a JR or JARL instruction immediately after the above successive data access, or one NOP instruction after the above successive data access.

[Workaround]

Implement either of the following workarounds.

- Cancel the fail-safe break setting for the internal RAM in the debugger.
  - When using ID850QB

    Click the [Detail] button in the Fail-safe Break field in the Configuration window and clear the check in the check box for “Internal RAM”.



  - When using MULTI

    Cancel the fail-safe break for “ramgrd” and “ramgrdv” using the Target flsf command.

- Insert two or more NOP instructions between the successive data access for the internal RAM area and an instruction to branch to the internal ROM area.

Please regard this item as a permanent restriction.

No. 16 Address is not retained during external bus access

[Description]

When the multiplexed bus output mode is selected for the external bus and its data bus size is 8 bits, the address is not retained after the T2 state is entered, but the low level is output.

[Workaround]

There is no workaround.

This restriction can be avoided by upgrading the device file to the following version.

- When using V850ES/Kx1: Use DF703218 V2.01 or later.
- When using V850ES/Kx1+: Use DF703318 V1.01 or later.

4. Cautions

4.1 General Cautions for Handling This Product

(a) Circumstances not covered by product guarantee

- If the product was disassembled, altered, or repaired by the customer
- If it was dropped, broken, or given another strong shock
- Use at overvoltage, use outside guaranteed temperature range, storing outside guaranteed temperature range
- If power was turned on while the AC adapter, USB interface cable, or target system connection was in an unsatisfactory state
- If the AC adapter cable, USB interface cable, emulation probe, or the like was bent or pulled excessively
- If an AC adapter other than the one supplied with the product is used
- If the product got wet
- If the product and target system were connected while a potential difference existed between the GND of the product and the GND of the target system
- If a connector or cable was removed while the power was being supplied to the product
- If an excessive load was placed on a connector or socket

(b) Safety precautions

- If used for a long time, the product may become hot (50°C to 60°C). Be careful of low temperature burns and other dangers due to the product becoming hot.
- Be careful of electrical shock. There is a danger of electrical shock if the product is used as described above in **(a) Circumstances not covered by product guarantee**.

4.2 Cautions on Extension Probe

- When using the extension probe, there is a restriction on the maximum operating frequency at which a high-speed signal such as a clock or external bus can be propagated. (See the table below.)
  Since the maximum operating frequency of the target device is 20 MHz, the extension probe can be used with the maximum operating frequency when using the QB-V850ESKX1H.

Use of Clock Signal (CLKOUT, BUSCLK, SDCLK, etc.)	Use of External Bus	Upper Limit of Frequency When Using Extension Probe
Used	Used	32 MHz
	Not used	
Not used	Used	64 MHz
	Not used	80 MHz

- An impedance of approx. 50 Ω is applied to the extension probe.

- The signal level decreases by approx. 0.1 V when it passes through the extension probe. This degrades the precision of analog signal propagation upon A/D conversion, etc.

- A delay of approx. 5 ns (propagation delay) occurs when a signal passes through the extension probe.
  Consequently, it may be necessary to set data waits or address waits when using the external bus.

- Be sure to connect IECUBE and the target to the GND line of the extension probe when using the extension probe; otherwise the level of the propagated signal may degraded.