NEC

Customer Notification

QB-V850ESFX3-ZZZ-EE

In-Circuit-Emulator

Operating Precautions

Target Devices:

V850ES/FE3:	V850ES/FF3:	V850ES/FG3:	V850ES/FJ3:	V850ES/FK3:
µPD70F3370	µPD70F3372	µPD70F3374	µPD70F3378	µPD70F3383
µPD70F3371	µPD70F3373	µPD70F3375	µPD70F3379	µPD70F3384
		µPD70F3376	µPD70F3380	µPD70F3385
		µPD70F3377	µPD70F3381	
			µPD70F3382	

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(A) Product Version

1. Product Code: QB-V850ESFX3-ZZZ-EE 'D'

Cautions: 1. In conjunction with the usable EXEC version a qualified device file (Dxxxxx.800) is additionally necessary for the corresponding device, which has to be emulated. Make sure that you use the appropriated version of the device file.

2. For operation with Green Hills MULTI a dedicated version of the
- EX850G32.dll (Version E1.72e or later) and
- 850eserv.exe (Version 3.2388 or later) is required.

3. DataFlash access is not supported by the IAR EW-V850-Full-EE or IAR EW-V850-KS64 products (both V3.20) yet.
DataFlash support will be added in a later version of the IAR Embedded Workbench.

(B) Table of Operating Precautions

No.	Outline		QB-V850ESFX3-ZZZ-EE			
		Control Code	A	B	C	D
1	Access of CnRGPT register during break (Specification change notice)		×	×	×	×
2	Access of CnTGPT register during break (Specification change notice)		×	×	×	×
3	Access of CnGNCTRL register during break (Specification change notice)		×	×	×	×
4	Emulator hangs up while downloading data or setting software break (Specification change notice)		×	×	×	×
5	External RAM connection (Technical limitation)		×	×	×	×
6	POC circuit and clock monitor (Technical limitation)		×	×	×	×
7	Illegal break during program execution in internal RAM (1) (Specification change notice)		×	×	×	×
8	Entering and releasing STOP mode when the RESET pin is masked (Specification change notice)		×	×	×	×
9	Illegal break during program execution in internal RAM (2) (Specification change notice)		×	×	×	×
10	LOCKR bit		×	✓	✓	✓
11	Programm execution and DMA transfer in internal RAM		×	×	×	×
12	Reset input during break		×	×	×	×
13	Accessing CBnRX register during break		×	×	×	×
14	RC oscillator Sub Clock frequency		×	×	✓	✓
15	WDT2 operation during STOP mode		×	×	×	✓

✓ Not applicable

× Applicable

Note: The Control Code is indicated by the letter appearing at the 2nd position from the left in the serial number of the product.

(C) Description of Operating Precautions

No. 1	Access of CnRGPT register during break (n = 0...3) (Specification change notice)

Details

Under the following conditions (a) and (b), the read pointer (RGPT) that should be incremented is not incremented and the same data as previously read is read again.

(a) If a software break occurs immediately after reading the CANn module receive history list register (CnRGPT)
(b) If a DMA transfer from the CANn module receive history list register (CnRGPT) is performed during a break**NOTE**.

Note: Including breaks by the RAM monitor function or DMM function. However the realtime RAM monitor function does not cause this behaviour since it does not set breaks.

Workaround

(a) Set a hardware break when setting a break immediately after reading the CnRGPT register.
(b) There is no workaround.

No. 2	Access of CnTGPT register during break (n = 0...3) (Specification change notice)

Details

Under the following conditions (a) and (b), the read pointer (TGPT) that should be incremented is not incremented and the same data as previously transmitted is transmitted again.

(a) If a software break occurs immediately after reading the CANn module transmit history list register (CnTGPT).
(b) If a DMA transfer from the CANn module transmit history list register (CnTGPT) is performed during a break**NOTE**.

Note: Including breaks by the RAM monitor function or DMM function. However the realtime RAM monitor function does not cause this behaviour since it does not set breaks.

Workaround

(a) Set a hardware break when setting a break immediately after reading the CnTGPT register.
(b) There is no workaround.

No. 3	Access of CnGNCTRL register during a break (n = 0...3) (Specificatin change notice)

Details

When a register access is performed in the following sequence, an unexpected forcible shutdown may occur after the sequence is complete.

Sequence :
(1) The EFSD bit of the CANn module control register (CnGMCTRL) is set.
(2) The I/O register**NOTE** is accessed.
(3) The GOM bit of the CANn mode control register (CnGMCTRL) is cleared.

Note: I/O register access except for clearing the GOM bit of the CnGMCTRL register

The conditions under which a forcible shutdown takes place are shown below:
(a) If a break occurs immediately after the I/O register access in (2) occurs.
(b) If a break by the RAM monitor function or the DMM function occurs immediately after the I/O register access in (2) occurs.
(c) Stepwise execution is performed for the I/O register access in (2).

Workaround

Be sure to set the EFSD bit and clear the GOM bit successively when executing a forcible shutdown. Do not perform a register access in the above sequence when not performing a forcible shutdown.

No. 4	Emulator hangs up while downloading data or setting software break (Specification change notice)

Details

The emulator may hang up when an active signal is connected to the WAIT or HLDRQ pin during program download or when a software break point is set to the internal ROM.

Workaround

When WAIT and HLDRQ are not used mask these signals using the pinmask function of the debugger.
When WAIT and HLDRQ are used do not connect an active signal to the WAIT or HLDRQ input pin during download or when a software break point is set to the internal ROM.

The above behaviour can be avoided using the following software components:
- ID850: Use the version 2.81 or later of the ID850 debugger.
- Green Hills Multi: Use the V1.57 or later of the exec.dll.

No. 5	External RAM connection (Technical limitation)

Details

When external RAM on the target system is connected to the CS0 area (0x100000 - 0x1fffff) and the bus control pins are active the data in this area may be overwritten by downloading data to the internal ROM area or by setting a software breakpoint in this area.

Workaround

Initialize the data in external RAM by program run after downloading data to the CS0 area or use a hardware break for the external RAM.

The above behaviour can be avoided using the following software components:
- ID850: Use the version 2.81 or later of the ID850 debugger.
- Green Hills Multi: Use the V1.57 or later of the exec.dll.

No. 6	POC circuit and clock monitor (Technical limitation)

Details

Emulation of the POC circuit and the clock monitor is not possible.

Workaround

There is no workaround.

No. 7	Illegal break during program execution in internal RAM (1) (Specification change notice)

Details

An illegal break may occur when a peripheral I/O register is accessed during program execution in internal RAM.

Workaround

Cancel the fail-safe break setting for the internal RAM in the debugger.
- In ID850QB debugger:
Click the button “Detail” in the “Fail-safe Break” field in the “Configuration” window and clear the check box for “Internal RAM”.
- In the MULTI debugger:
Cancel the fail-save break for “ramgrd” and “ramgrdv” using the target command “flsf”

No. 8	Entering and releasing STOP mode when the RESET pin is masked (Specification change notice)

Details

When the RESET pin is masked using the pin mask function of the debugger and watchdog timer 2 is used in reset mode, the CPU's internal operating clock is switched to the internal ring oscillator clock after STOP mode is released, depending on the timing for entering and releasing STOP mode (one of (1) to (4) of the below table). After the clock is switched to the ring oscillator clock, the CPU continues the operation with the ring oscillator clock until a reset is ececuted by the debugger.

No.	Operating clock for watchdog timer 2	Timing at which CPU operation clock switches to ring oscillator clock
1	Main clock	STOP mode is entered during the period from when a reset of watchdog timer 2 occurs until the reset is released **Note**.
2	Subclock	STOP mode is entered during the period from when a reset of watchdog timer 2 occurs until the reset is released **Note**.
3	Ring oscillator clock	STOP mode is entered during the period from when a reset of watchdog timer 2 occurs until the reset is released **Note**.
4		The internal oscillation clock is stopped during the the period from when a reset of watchdog timer 2 occurs until the rset is released **Note**, and then STOP mode is entered.

Note The period in which watchdog timer 2 generates a reset signal while the reset signal of watchdog timer 2 is masked as a result of masking RESET using the pin mask function of the debugger.

Workaround

Do not use watchdog timer 2.
To generate a reset of watchdog timer 2, do not mask the RESET pin using the pin mask function of the debugger.

No. 9	Illegal break during program execution in internal RAM (2) (Specification change notice)

Details

A non-map break occurs if all of the following conditions are satisfied, even if the program itself is correct:
- A program is executed in the internal RAM.
- Data access for the internal RAM area is performed twice successively.
- A branch occurs to the internal ROM area using a JR or JARL instruction immediately after the above successive data access or one NOP instruction after the above successive data access.

Workaround

Implement either one of the following workarounds.

1.
- When using ID850QB:
Click the “Detail” button in the fail save break field in the configuration window and clear the check box for “Internal RAM”.
- When using MULTI:
Cancel the fail save break for “ramgrd” and “ramgrdv” using the target command “flsf”.

2.
Insert two or more NOP instructions between the successive data access for the internal RAM area and the instruction to branch to the internal ROM area.

No. 10	LOCKR bit

Details

After the PLLON bit is set, the LOCKR bit might not be set.

Workaround

There is no workaround.
If the LOCKR does not become set, clear the PLLON bit and set it again.

No. 11	Programm execution and DMA transfer in internal RAM

Details

When a data access instruction for a misaligned address allocated in the internal RAM and a DMA transfer for the internal RAM are executed simultaneously, the CPU may stop working. At this time only a reset can be acknowledged (an NMI or interrupt cannot be acknowledged).

Workaround

Do not perform a DMA transfer for the internal RAM when a data access instruction for a misaligned address allocated in the internal RAM is being executed or vice versa.

No. 12	Reset input during break

Details

The emulator may stop working if a break occurs when the RESET pin is active (low level).

Workaround

Mask the RESET pin using the pin mask function of the debugger.

No. 13	Accessing CBnRX register during break

Details

When the CSIBn receive data register (CBnRX) is read, usually the next reception operation is started.
Under the following conditions (a) and (b) the next reception operation is not started even if CBnRX is read.
(a) If a software break occurs immediately after reading the CSIBn receive data register (CBnRX).
(b) If a DMA transfer from the CSIBn receive data register (CBnRX) is performed during a break.[Note]
As a result, communication stops or the DMA controller stops.

Note: Includes breaks by the RAM monitor function or DMM function but does not include the Real-time RAM monitor function as it does not set breaks.

Workaround

(a) Set a hardware break when setting a break immediately after reading the CBnRX register.
(b) There is no workaround.
Please regard items (a) and (b) as permanent restrictions.

No. 14	RC oscillator Sub Clock frequency

Details

The operation frequency of the RC oscillation Sub clock is not within the specified frequency range (20kHz to 40kHz).

Workaround

There is no workaround.

No. 15	WDT2 operation during STOP mode

Details

When the WDT2 is clocked on the external oscillator (fx) (WDCS23 = '1') the WDT2 clock will not stop its operation when the STOP mode is entered.
Depending on the count value of the WDT2 counter and the duration of the STOP mode, the WDT2 counter may overflow and the programmed operation mode of the WDTM2 register (RESET (WDT2RES signal) or NMI interrupt (INTWDT2 signal)) will occur. This may happen during STOP mode or after STOP mode release (Operating Mode).

Workaround

(1) Select a WDT2 overflow time that is longer than the duration of the STOP mode + the oscillation stabilization time programmed in the OSTS register. Trigger the WDT2 before entering STOP mode and trigger the WDT2 immediately after release of STOP mode.
(2) Switch off the WDT2 during intitialisation.

(D) Cautions

Cautions on Extension Probe

- When using the extension probe, there is a restriction on the maximum operating frequency at which a high-speed signal such as a clock or external bus can be propagated. (See the table below.)
- With the QB-V850ESFX3, the maximum operating frequency of the target device is 48 MHz, but it is 32 MHz when the clock signals are used.

Use of Clock Signal (CLKOUT, BUSCLK, SDCLK, etc.)	Use of External Bus	Upper Limit of Frequency When Using Extension Probe
Used	Used	32 MHz
	Not used	
Not used	Used	64 MHz
	Not used	80 MHz

- An impedance of approx. 50 Ohm is applied to the extension probe.
- The signal level decreases by approx. 0.1 V when it passes through the extension probe. This degrades the precision of analog signal propagation upon A/D conversion, etc.
- A delay of approx. 5 ns (propagation delay) occurs when a signal passes through the extension probe. Consequently, it may be necessary to set data waits or address waits when using the external bus.
- Be sure to connect IECUBE and the target to the GND line of the extension probe when using the extension probe; otherwise the level of the propagated signal may degraded.

(E) Valid Specification

Item	Date pulished	Document No.	Document Title
1	Dezember 2006	U17793EE2V1UM00	V850ES/FX3 Preliminary User's Manual
2	April 2004	U15943EJ3V0UM00	V850ES Architecture Manual

(F) Revision History

Item	Date pulished	Document No.	Comment
1	April 2006	EASE-CN-0008-1.0	Initial release
2	May 2006	EASE-CN-0008-1.1	Added precautions #11 and #12. Removed item #17 in chapter (c).
3	October 2006	EASE-CN-0008-1.2	Added Control Code 'B' in chapter (B) Added precaution #13 and #14.
4	March 2007	EASE-CN-0008-1.3	Added Control Code 'C' in chapter (B) Added item 15 Added items 13 and 14 to chapter (C) 'Table of Operating Precautions'
5	September 2007	EASE-CN-0008-1.4	Added Control Code 'D' in chapter (B)