Microcontroller Technical Information

PG-FP5 Flash Memory Programmer Usage Restrictions		Document No.	ZBG-CD-09-0063		1/2
		Date issued	December 24, 2009		
		Issued by	Development Tool Solution Group Multipurpose Microcomputer Systems Division Microcomputer Operations Unit NEC Electronics Corporation		
Related documents	PG-FP5 Flash Memory Programmer User's Manual: U18865EJ2V0UM00 PG-FP5 (Control Code: A, C) Operating Precautions: ZUD-CD-09-0129-02	Notification classification	√	Usage restriction	
				Upgrade	
				Document modification	
				Other notification	

1. Affected product

Product	Outline	Control Code[Note 1]
PG-FP5	Flash memory programmer	A, C (Firmware: V2.03 or earlier, FPGA: V2 or earlier, Programming GUI: V2.03 or earlier)[Note 2]

To check the version, perform the following procedure:

- Firmware: On the menu bar, click **Programmer**, and then select **Reset**.
- FPGA: On the menu bar, click **Programmer**, and then select **Reset**.
- Programming GUI: On the menu bar, click **Help**, and then select **About FP5...**.

Notes 1. The control code is the second digit from the left in the 10-digit serial number. If the product has been upgraded, a label indicating the new version is attached to the product and the *x* in **V-UP *x*** on this label indicates the control code.

2. Products with control code A and those with control code C are functionally equivalent. These products can be used in combination with the relevant version of firmware, FPGA, and programming GUI.

2. New restrictions

A new restriction (No. 15) has been added. See the attachment for details.

3. Workarounds

See the attachment for details.

4. Modification schedule

Products from which restrictions No. 14 and No. 15 are removed are scheduled for release with the next upgrade (to be released in mid-January 2010).

5. List of restrictions

See the attachment.

6. Document revision history

PG-FP5 Flash Memory Programmer - Usage Restrictions

Document Number	Issued on	Description
ZBG-CD-07-0040	July 4, 2007	Addition of specification change (No. 1) Addition of restriction (No. 2)
ZBG-CD-07-0071	October 11, 2007	Addition of restrictions (No. 3 to No. 8)
ZBG-CD-08-0011	March 24, 2008	Addition of restrictions (No. 9 to No. 11)
ZBG-CD-09-0038	July 16, 2009	Addition of restrictions (No. 12 and No. 13)
ZBG-CD-09-0055	October 15, 2009	Addition of restriction (No. 14)
ZBG-CD-09-0063	December 24, 2009	Addition of restriction (No. 15)

Restrictions on Using PG-FP5

1. Product Version

Item No.	Control Code	Firmware	FPGA	Programming GUI
<1>	A	V1.00	V1	V1.00
<2>		V1.01	V1	V1.00
<3>		V2.00	V2	V2.00
<4>		V2.01	V2	V2.01
<5>		V2.02	V2	V2.02
<6>	A, C	V2.03	V2	V2.03

2. Restrictions

2.1 Restriction List

No.	Restrictions	Product Version (Item No.)					
		<1>	<2>	<3>	<4>	<5>	<6>
1	Restriction whereby `Invalid Device Port` is displayed	×	×	○	○	○	○
2	Restriction whereby standalone operation can no longer be performed under specific conditions	×	○	○	○	○	○
3	Restriction whereby erasing is performed even if **Erase memory before download** is not selected	×	×	○	○	○	○
4	Restriction whereby the status bar is displayed incorrectly	×	×	○	○	○	○
5	Restriction whereby the RESET pin is always pulled up at 5 V when **Run after Disconnect** is specified	×	×	○	○	○	○
6	Restriction whereby no clock is supplied if **FP5CLK** is selected for pseudo 3-wire communication or I^2C communication	×	×	○	○	○	○
7	Restriction whereby Motorola S type program files are not displayed in the list box	×	×	○	○	○	○
8	Restriction whereby the FLMD0 pin outputs low level when 78K0S (single-wire UART) is used	×	×	○	○	○	○
9	Restriction whereby lowercase letters are illegally converted to uppercase letters when **upprm** or **upset** command is executed	×	×	×	○	○	○
10	Restriction whereby an invalid checksum result is obtained if a program file is downloaded in Simple mode	–	–	×	○	○	○
11	Restriction whereby bank switching for the program file cannot be specified in bank mode	–	–	×	○	○	○
12	Restriction on reading a Motorola S1-record hex format program file	×	×	×	×	×	○
13	Restriction related to installation of USB driver	–	–	–	–	×	○
14	Restriction whereby the error `NAND flash - Mapping Error` is displayed	×	×	×	×	×	×
15	Restriction whereby the message display is not updated	×	×	×	×	×	×

–: Not relevant, ×: Applicable, ○: Already corrected

2.2 Restriction Details

No. 1 Restriction whereby `Invalid Device Port` is displayed

Description:

When a PR5 file is downloaded, the message `Invalid Device Port` might be displayed in the action log window. After that, PR5 files can no longer be downloaded correctly.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. 2 Restriction whereby standalone operation can no longer be performed under specific conditions

Description:

If execution of a command is continued using control buttons on the PG-FP5 main unit while the Programming GUI is not running, the message `ERROR: 800 Res. by Watchdog` is displayed in the message display on the PG-FP5 main unit and the subsequent operations might no longer be able to be performed.

Workaround:

There is no workaround. When this situation occurs, control of the **POWER** button is also unavailable. Therefore, disconnect the AC adapter and connect it again to restart the PG-FP5.

Action:

This issue has been corrected in products with control code A (firmware: V1.01, FPGA: V1, GUI: V1.00) and later.

No. 3 Restriction whereby erasing is performed even if **Erase memory before download** is not selected

Description:

Erasing is performed even if the **Erase memory before download** check box is not selected in the **Download file** dialog box opened by clicking the browse button in the **Object HEX file** area on the **Target** tab in the **Device Setup** dialog box.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. 4 Restriction whereby the status bar is displayed incorrectly

Description:

The status bar is displayed incorrectly in the following cases:

(1) An error is displayed erroneously if it takes five or more seconds for SUM data to be returned during **Checksum** command execution.

(2) `PASS` is displayed erroneously if the code flash is verified to be OK and the data flash is verified to be error.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. 5 Restriction whereby the RESET pin is always pulled up at 5 V when **Run after Disconnect** is specified

Description:

The RESET pin of the PG-FP5 must go into the Hi-Z state when **Run after Disconnect** is specified, but it is pulled up at 5 V.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. 6 Restriction whereby no clock is supplied if **FP5CLK** is selected for pseudo 3-wire communication or I^2C communication

Description:

No clock is supplied if **FP5CLK** is selected for pseudo 3-wire communication or I^2C communication.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. 7 Restriction whereby Motorola S type program files are not displayed in the list box

Description:

When a Motorola S type program file (other than `*.hex` and `*.rec`) is selected in the **Download file** dialog box opened by clicking the browse button in the **Object HEX file** area on the **Target** tab in the **Device Setup** dialog box, the file is not displayed in the list box in the **Object HEX file** area.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. 8 Restriction whereby the FLMD0 pin outputs low level when 78K0S (single-wire UART) is used

Description:

If the CLK and FLMD0 pins are shorted in the target system when 78K0S (single-wire UART) is used, the FLMD0 pin that should output Hi-Z incorrectly outputs low level, which disturbs programming. (This restriction applies when using a microcontroller that uses the FLMD0 pin before using 78K0S (single-wire

UART).)

Workaround:

Execute the **Reset** command of the PG-FP5 or turn off and then on the PG-FP5 power before using 78K0S (single-wire UART); the FLMD0 pin afterward outputs Hi-Z.

Action:

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. 9 Restriction whereby lowercase letters are illegally converted to uppercase letters when **upprm** or **upset** command is executed

Description:

Letter “a” in the format version is illegally converted to “A” when the **upprm** command is executed. The extension of parameter files are illegally converted to uppercase letters when the **upset** command is executed. Use of the files created by these commands does not cause problems.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01) and later.

No. 10 Restriction whereby an invalid checksum result is obtained if a program file is downloaded in Simple mode

Description:

If a program file that includes the data flash is downloaded in Simple mode, the checksum result to be displayed in the message display on the PG-FP5 main unit, which should indicate the checksum of the code flash and data flash areas, indicates the checksum of the code flash area only.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01) and later.

No. 11 Restriction whereby bank switching for the program file cannot be specified in bank mode

Description:

When the PG-FP5 runs in bank mode and if a programming area is selected via a bank signal from the remote connector, the programming area selected via the bank signal should usually be selected, but the program file in the programming area selected by the Programming GUI is selected. To `PR5` and `ESF` files, the settings selected via the bank signal are applied.

Example:

Programming area number selected by Programming GUI: 0

Programming area number selected via bank signal: 1

In this case, `PR5` and `ESF` files in programming area 1 and the program file in programming area 0 are specified.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01) and later.

No. 12 Restriction on reading a Motorola S1-record hex format program file

Description:

If a program file in the Motorola S1-record hex format is read to the FP5, program files saved in the specified programming area become invalid.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A or C (firmware: V2.03, FPGA: V2, GUI: V2.03) and later.

No. 13 Restriction related to installation of USB driver

Description:

If an FP5 unit is connected to a USB port to which another FP5 unit with a different serial number was connected on the same host, the USB driver is not automatically recognized and installation of the USB driver is requested.

Workaround:

There is no workaround.

Action:

This issue has been corrected in products with control code A or C (firmware: V2.03, FPGA: V2, GUI: V2.03) and later.

No. 14 Restriction whereby the error `NAND flash - Mapping Error` is displayed

Description:

If the PG-FP5 is used continuously while conditions (1) and (2) below are satisfied, the error below might be displayed in the action log window when a program file is downloaded or a writing command is executed.

(1) A program file that has a cluster of FFh data that is 16 KB or longer is used.

(2) The program file described in (1) is frequently downloaded.

Displayed error:

```
*** System Error(s), Warning(s):
Warning: NAND flash - Mapping Error
```

Even if the above error is displayed, downloading the program or executing the writing command is performed correctly.

Workaround:

Contact an NEC Electronics sales representative or distributor.

Action:

This issue will be corrected in the next revision.

No. 15 Restriction whereby the message display is not updated

Description:

The writing status shown in the message display on the PG-FP5 unit might freeze and no longer be updated. (Even if this problem occurs, a command that downloads or writes a program runs normally.)

Workaround:

There is no workaround.

Action:

This issue will be corrected in the next revision.