Date: Mar. 24, 2017

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	System LSI	Document No.	TN-RIN-A019A/E	Rev.	1.00
Title	Notification of R-IN32M3 Series User's Manual: R-IN32M3-CL (Rev.3.00 to Rev.3.01) Revised contents: Corrections and new functions		Information Category	Technical Notification	
Applicable Product	See following	Lot No. / All lots	Reference Document	R-IN32M3 Series User's Manual: R-IN32M3-CL Rev. 3.01 (R18UZ0005EJ0301)	

R-IN32M3 Series User's Manual: R-IN32M3-CL Rev. 3.01 (R18UZ0005EJ0301) has been released on Renesas website. This technical update follows revision 3.00 and includes the entirety of revised items. For details, refer to "2. Documentation Updates" given below.

1 Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
	MC-10287BF1	MC-10287BF1-HN4-A
		MC-10287BF1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A
	D60510BF1	UPD60510BF1-HN4-A
		UPD60510BF1-HN4-M1-A

2 Documentation Updates

No	Applicable Item (Rev. 3.01 Section)	Applicable Page (Rev. 3.01)	Contents
1	2.1.13 CC-Link IE Field Pins (Intelligent Device Station)	18	Complement
2	2.1.14 CC-Link Pins (Intelligent Device Station)	19	Complement
3	2.1.16 System Pins	21	Expression alignment
4	4.2 List of Interrupts, Table 4.1 (2/4)	46	Expression alignment
5	4.2 List of Interrupts, Table 4.1 (3/4), (4/4)	48-49	New function
6	5. Peripheral Modules	50	Expression alignment
7	6.2 Cautionary Notes	55	Complement

No.1 2.1.13 CC-Link IE Field Pins (Intelligent Device Station)

Note to the section modified.

<table>
<tr><th colspan="2">V3.00</th><th colspan="2">V3.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>18</td><td>[2.1.13 CC-Link IE Field Pins (Intelligent Device Station)]

Note: When user does boot with the external memory boot mode, external serial flash ROM boot mode, or instruction RAM boot mode, be sure not to input the low level to P33 (multiplexed with CCI_WAITEDGEH) and P34 (CCI_WRLENH) pins during a reset. P33 and P34 pins should be left open circuit or the high level should be input to the pins during a reset.
If you input the low level to P33 and P34 pins during a reset, you cannot access the CC-Link IE field from the CPU of the R-IN32M3.</td><td>18</td><td>[2.1.13 CC-Link IE Field Pins (Intelligent Device Station)]

Note: When user does boot with the external memory boot mode, external serial flash ROM boot mode, or instruction RAM boot mode, be sure not to input the low level to P33 (multiplexed with CCI_WAITEDGEH) and P34 (multiplexed with CCI_WRLENH) pins during a reset. P33 and P34 pins should be left open circuit or the high level should be input to the pins during a reset.
If you input the low level to P33 and P34 pins during a reset, you cannot access the CC-Link IE field from the CPU and DMA controller of the R-IN32M3.</td></tr>
</table>

No.2 2.1.14 CC-Link Pins (Intelligent Device Station)

Description for the CCM_MDIN0-3 signals modified.

<table>
<tr><th colspan="2">V3.00</th><th colspan="2">V3.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>19</td><td>[2.1.14 CC-Link Pins (Intelligent Device Station)]

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th><th>Level during & after Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>O</td><td>Link error LED control output</td><td>P20</td><td>Low</td><td>Hi-Z(High)</td></tr>
<tr><td>CCM_ERRZ</td><td>O</td><td>Error LED control output</td><td>P21</td><td>Low</td><td></td></tr>
<tr><td>CCM_RUNZ</td><td>O</td><td>Run LED control output</td><td>P26</td><td>Low</td><td></td></tr>
<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>I</td><td>Mode setting switch input</td><td>P62-P65</td><td>–</td><td></td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>I</td><td>Station no. setting switch input</td><td>P70-P77</td><td>–</td><td></td></tr>
</table>
</td><td>19</td><td>[2.1.14 CC-Link Pins (Intelligent Device Station)]

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th><th>Level during & after Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>O</td><td>Link error LED control output</td><td>P20</td><td>Low</td><td>Hi-Z(High)</td></tr>
<tr><td>CCM_ERRZ</td><td>O</td><td>Error LED control output</td><td>P21</td><td>Low</td><td></td></tr>
<tr><td>CCM_RUNZ</td><td>O</td><td>Run LED control output</td><td>P26</td><td>Low</td><td></td></tr>
<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>I</td><td>Transfer rate and mode setting switch input</td><td>P62-P65</td><td>–</td><td></td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>I</td><td>Station no. setting switch input</td><td>P70-P77</td><td>–</td><td></td></tr>
</table>
</td></tr>
</table>

No.3 2.1.16 System Pins
Function of PONRZ modified

<table>
<tr><th colspan="2">V3.00</th><th colspan="2">V3.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>22</td><td>[2.1.16 System Pins]
<table><tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Active</th><th>Level during & after Reset</th></tr><tr><td>PONRZ</td><td>I</td><td>Internal RAM power on reset input</td><td>Low</td><td>-</td></tr></table></td><td>22</td><td>[2.1.16 System Pins]
<table><tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Active</th><th>Level during & after Reset</th></tr><tr><td>PONRZ</td><td>I</td><td>Power on reset input</td><td>Low</td><td>-</td></tr></table></td></tr>
</table>

No.4 4.2 List of Interrupts
Exception No.54 INTETHSW: Interrupt source name changed

<table>
<tr><th colspan="2">V3.00</th><th colspan="2">V3.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>47</td><td>[4.2 List of Interrupts]
[Table 4.1 List of Interrupts]
(2/4)<table><tr><th rowspan="2">Exception No.</th><th rowspan="2">Name</th><th rowspan="2">Interrupt Source</th><th colspan="5">Connected to</th></tr><tr><th>NVIC</th><th>HW-RTOS</th><th>DMAC</th><th>Real Time Port</th><th>Timer</th></tr><tr><td>54</td><td>INTETHSW</td><td>Ether SWITCH interrupt</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr></table></td><td>47</td><td>[4.2 List of Interrupts]
[Table 4.1 List of Interrupts]
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</table>

No.5 4.2 List of Interrupts

ECC error interrupts are added to exception numbers 115 to 120 of Table 4.1.

V3.00

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[4.2 List of Interrupts]

[Table 4.1 List of Interrupts]

(3/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	NVIC
114	–	Reserved	–	–	–	–	–
115	–	Reserved	–	–	–	–	–
116	–	Reserved	–	–	–	–	–
117	–	Reserved	–	–	–	–	–
118	–	Reserved	–	–	–	–	–
119	–	Reserved	–	–	–	–	–

(4/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	NVIC
120	–	Reserved	–	–	–	–	–

V3.01

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[4.2 List of Interrupts]

[Table 4.1 List of Interrupts]

(3/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
114	–	Reserve	–	–	–	–	–
115	IRAMECCSEC	Internal instruction RAM 1-bit ECC error correction interrupt	✓	–	–	–	–
116	DRAMECCSEC	Data RAM 1-bit ECC error correction interrupt	✓	–	–	–	–
117	BRAMECCSEC	Buffer RAM 1-bit ECC error correction interrupt	✓	–	–	–	–
118	IRAMECCDED	Internal instruction RAM 2-bit ECC error detection interrupt	✓	–	–	–	–
119	DRAMECCDED	Data RAM 2-bit ECC error detection interrupt	✓	–	–	–	–

(4/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
120	BRAMECCDED	Buffer RAM 2-bit ECC error detection interrupt	✓	–	–	–	–

No.6 5. Peripheral Modules

Expressions of peripheral functions are unified to that in the User's Manual (Peripheral Modules).

V3.00		V3.01	
Page	Description	Page	Description
50	**[5. Peripheral Modules]** ● Clock function ● CPU ● Bus structure ● Hardware real-time OS ● Gigabit Ethernet interface ● Asynchronous SRAM memory controller ● Synchronous burst access memory controller ● Serial flash ROM memory controller ● DMA function ● Timer array unit J (TAUJ) ● Window watchdog timer A (WDTA) ● Asynchronous serial interface J (UARTJ) ● Clocked serial interface H (CSIH) ● I2C BUS (IICB) ● CAN controller (FCN) ● CC-Link (Intelligent device station) ● CC-Link (Remote device station) ● Other interface control	50	**[5. Peripheral Modules]** ● Clock function/Reset function ● CPU/Internal RAM ● Bus structure ● Hardware real-time OS ● Gigabit Ethernet interface ● Asynchronous SRAM memory controller ● Synchronous burst access memory controller ● External MCU interface ● Serial flash ROM memory controller ● DMA function ● Timer array unit J (TAUJ2) ● Window watchdog timer A (WDTA) ● Asynchronous serial interface J (UARTJ) ● Clocked serial interface H (CSIH) ● I2C BUS (IICB) ● CAN controller (FCN) ● CC-Link (Intelligent device station, Remote device station) ● System registers (APB peripheral register area) ● Debug function

No.7 6.2 Cautionary Notes

"6.2 Cautionary Notes" newly added.

V3.00		V3.01	
Page	Description	Page	Description
-	**[6.2 Cautionary Notes]** (No description)	55	**[6.2 Cautionary Notes]**