To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Jul.21.2005

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-MC*-A013A/E	Rev.	1.00
Title	Notes on WAIT function of the I^2C bus interface		Information Category	Technical Notification		
Applicable Product	H8/3664 group H8S/2148 group, H8S/2138 group H8S/2149,H8S/2169 group H8S/2140B group H8S/2110B H8S/2111B H8S/2114 group H8S/2128 group H8S/2158 group H8S/2168 group H8S/2194 group H8S/2199R group H8S/2258, H8S/2239, H8S/2238 group H8S/2268, H8S/2264 group H8S/2633 group H8S/2638, H8S/2636 group H8S/2643 group SH7144 group, SH7145 group	Lot No. All	Reference Document	H8/3664 series Rev.5.00 H8S/2148 series Rev.3.00 H8S/2138 series Rev.3.00 H8S/2149,69 series Rev.2.00 H8S/2140B series Rev.2.00 H8S/2110B Rev.1.00 H8S/2111B Rev.1.00 H8S/2114 group Rev.2.00 H8S/2128 series Rev.3.00 H8S/2158 series Rev.2.00 H8S/2168 group Rev.3.00 H8S/2194 series Rev.2.00 H8S/2199R series Rev.1.00 H8S/2258,39,38,37,27 series Rev.4.00 H8S/2268,64 group Rev.3.00 H8S/2633 group Rev.5.00 H8S/2636,38,39,30 group Rev.6.00 H8S/2643 series Rev.3.00 SH7144, SH7145 group Rev.3.00		

We would like to inform you of our notes on the WAIT function of the IIC bus interface in master mode.

Please read the following descriptions carefully.

1.Applicable function

IIC bus interface module

2.Conditions to cause this phenomenon

When both of the following conditions are satisfied, the clock pulse of the 9th clock could be outputted continuously in master mode using the WAIT function due to the failure of the WAIT insertion after the 8th clock fall.

(1) Setting the WAIT bit of the ICMR register to 1 and operating WAIT, in master mode

(2) If the IRIC bit of interrupt flag is cleared from 1 to 0 between the fall of the 7th clock and the fall of the 8th clock.

3.Error Phenomenon

Normally, WAIT State will be cancelled by clearing the IRIC flag bit from 1 to 0 after the fall of the 8th clock in WAIT State.

In this case, if the IRIC flag bit is cleared between the 7th clock fall and the 8th clock fall, the IRIC flag clear- data will be retained internally. Therefore, the WAIT State will be cancelled right after WAIT insertion on 8th clock fall.

4.Restrictions

Please clear the IRIC flag before the rise of the 7th clock (the counter value of BC2 through BC0 should be 2 or greater), after the IRIC flag is set to 1 on the rise of the 9th clock.

If the IRIC flag-clear is delayed due to the interrupt or other processes and the value of BC counter is turned to 1 or 0, please confirm the SCL pins are in L' state after the counter value of BC2 through BC0 is turned to 0, and clear the IRIC flag. (See Figure 1)

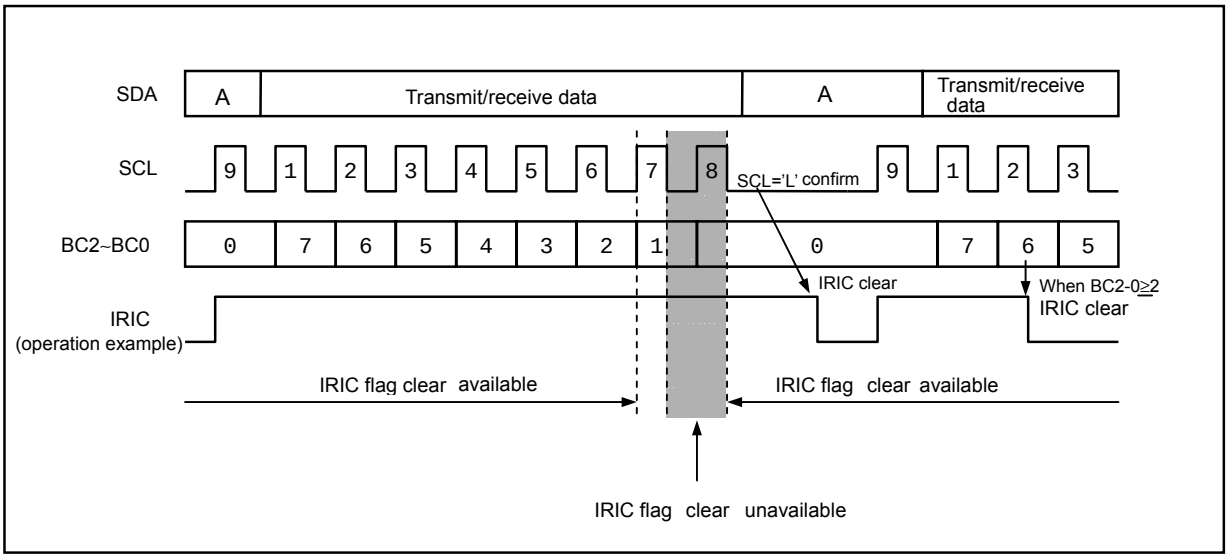

Figure 1. IRIC flag clear timing on WAIT operation

[Note] Limitation on use of H8S/2140B series, H8S/2110B, H8S/2111B, and H8S/2114 group can be cleared by setting the FNC1 and the FNC0 bit of the ICXR register to B'11.