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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A117A/E	Rev.	1.00
Title	Notes on using the 12-Bit A/D Converter (S12ADB) in extended operation in double trigger mode		Information Category	Technical Notification		
Applicable Product	RX63T Group	Lot No.	Reference Document	RX63T Group User's Manual: Hardware Rev.2.10 (R01UH0238EJ0210)		

We have identified some restrictions on usage of 12-Bit A/D Converter (S12ADB) in extended operation in double trigger mode.

The following describes the usage limitations and the corrections in the manual.

■Usage Limitations

Using A/D Conversion in Extended Double Trigger Mode, when A/D conversion is stopped by ADCSR.ADST bit set to 0, S12ADI interrupt is occurred, but data may not be stored away by A/D Data Duplication Register A and A/D Data Duplication Register B (ADDBLDRA,ADDBLDRB).

When A/D conversion is stopped by ADCSR.ADST bit set to 0, please do in the following procedures.

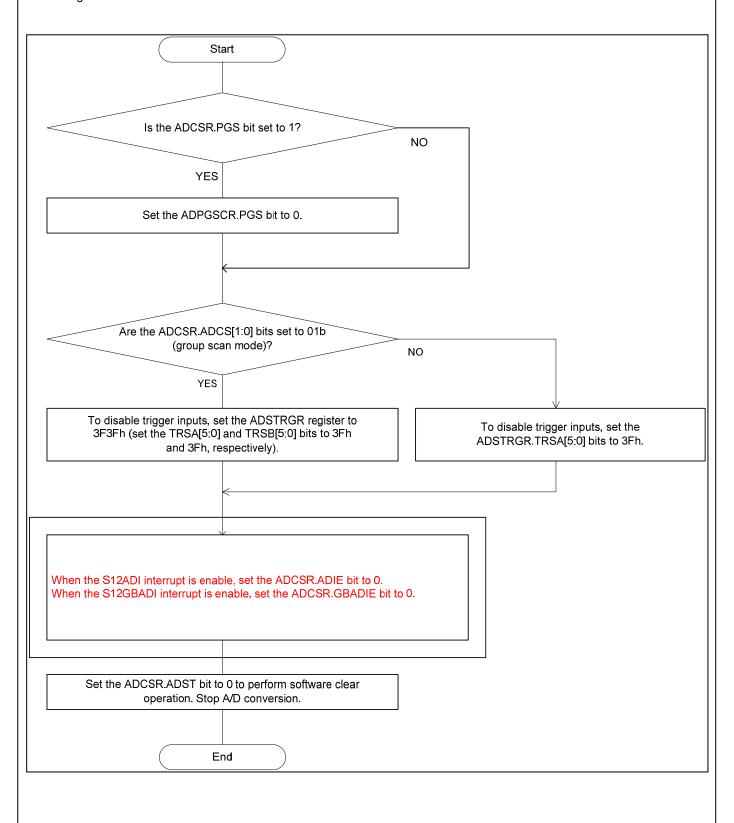
- 1) To disable trigger inputs, set the ADSTRGR register to 3F3Fh.
- 2) Set the ADCSR.ADIE bit to 0, and the ADCSR.GBADIE bit to 0 to disable A/D conversion end interrupt.
- 3) Set the ADCSR.ADST bit to 0 to perform software clear operation. Stop A/D conversion.



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- **■**Corrections in the Manual
- 1) Page 1534 of 1851

The description of Figure 34.32 Procedures for Clear Operation by Software through the ADCSR.ADST Bit has been changed as follows.



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2) Page 1534 of 1851

The description of Figure 35.7 Procedures for Clear Operation by Software through the ADCSR.ADST Bit has been changed as follows.

