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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A126A/E	Rev.	1.00
Title	Notes on Selecting Open-Drain Outputs for the Serial Peripheral Interface (RSPI)		Information Category	Technical Notification		
Applicable Product	RX63T Group	Lot No. All lots	Reference Document	RX63T Group User's Manual: Hardware Rev.2.10 (R01UH0238EJ0210)		

We have found that correctly selecting open-drain outputs for the serial peripheral interface (RSPI) of the above products by using the manual for guidance was not possible due to incorrect and incomplete descriptions in the manual. Therefore, we would like to inform you of the correct method for selecting open-drain outputs and the accompanying change to the manual.

■ How to select open-drain outputs for the serial peripheral interface (RSPI)

The open-drain outputs are selectable in products in 144-, 120-, 112-, and 100-pin packages, but not in those in 64- and 48-pin packages. However, even in the 144-, 120-, 112, and 100-pin versions, the open-drain output cannot be selected by following the guidance of the description in the current manual.

In the following, the method for selecting the open-drain output in the 144-, 120-, 112, and 100-pin products will be described.

Setting the ODRn.Bi bit to 1 described in Section 32.3.2, Controlling RSPI Pins, in RX63T Group User's Manual: Hardware Rev.2.10 does not select the open-drain output. Selecting it requires setting of the SPOM bit, which is listed as a reserved bit in Section 32.2.3, RSPI Pin Control Register (SPPCR). The changes to Section 32.2.3, RSPI Pin Control Register (SPPCR) are shown below.

32.2.3 RSPI Pin Control Register (SPPCR)

Address(es): RSPI0.SPPCR 0008 8382h, RSPI1.SPPCR 0008 83A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	SPOM	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPLP	RSPI Loopback	0: Normal mode 1: Loopback mode (reversed transmit data = receive data)	R/W
b1	SPLP2	RSPI Loopback 2	0: Normal mode 1: Loopback mode (transmit data = receive data)	R/W

Bit	Symbol	Bit Name	Description	R/W
b2	SPOM	RSPI Output Pin Mode	[In 144-, 120-, 112-, and 100-pin versions] 0: CMOS output 1: Open-drain output [In 64- and 48-pin versions] 0: CMOS output 1: Setting prohibited	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MOIFV	MOSI Idle Fixed Value	0: The level output on the MOSIn pin during MOSI idling is low. 1: The level output on the MOSIn pin during MOSI idling is high.	R/W
b5	MOIFE	MOSI Idle Value Fixing Enable	0: MOSI output value equals final data from previous transfer 1: MOSI output value equals the value set in the MOIFV bit	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Do not execute the subsequent operations if the contents of SPPCR are changed while the SPCR.SPE bit is 1.

SPLP Bit (RSPI Loopback)

The SPLP bit selects the mode of the RSPI pins.

When the SPLP bit is set to 1, the RSPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects (reverses) the input path and output path for the shift register (loopback mode).

SPLP2 Bit (RSPI Loopback 2)

The SPLP2 bit selects the mode of the RSPI pins.

When the SPLP2 bit is set to 1, the RSPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path for the shift register (loopback mode).

SPOM Bit (RSPI Output Pin Mode)

For 144-, 120-, 112-, and 100-pin products, the SPOM bit selects CMOS output or open-drain output as the form of output from the RSPI pin. For 64- and 48-pin products, leave this bit at its initial value.

MOIFV Bit (MOSI Idle Fixed Value)

If the MOIFE bit is 1 in master mode, the MOIFV bit determines the MOSIn pin output value during the SSL negation period (including the SSL retention period during a burst transfer).

MOIFE Bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the RSPI in master mode is in an SSL negation period (including the SSL retention period during a burst transfer). When the MOIFE bit is 0, the RSPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIn pin. When the MOIFE bit is 1, the RSPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

■ The change in the manual

■ The changes and additions in red text below have been made in Section 32.2.3, RSPI Pin Control Register (SPPCR), on page 1383.

Address(es): RSPI0.SPPCR 0008 8382h, RSPI1.SPPCR 0008 83A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	SPOM	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPLP	RSPI Loopback	0: Normal mode 1: Loopback mode (reversed transmit data = receive data)	R/W
b1	SPLP2	RSPI Loopback 2	0: Normal mode 1: Loopback mode (transmit data = receive data)	R/W
b2	SPOM	RSPI Output Pin Mode	In 144-, 120-, 112-, and 100-pin products 0: CMOS output 1: Open-drain output In 64- and 48-pin products 0: CMOS output 1: Setting prohibited	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MOIFV	MOSI Idle Fixed Value	0: The level output on the MOSIn pin during MOSI idling is low. 1: The level output on the MOSIn pin during MOSI idling is high.	R/W
b5	MOIFE	MOSI Idle Value Fixing Enable	0: MOSI output value equals final data from previous transfer 1: MOSI output value equals the value set in the MOIFV bit	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Do not execute the subsequent operations if the contents of SPPCR are changed while the SPCR.SPE bit is 1.

SPLP Bit (RSPI Loopback)

The SPLP bit selects the mode of the RSPI pins.

When the SPLP bit is set to 1, the RSPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects (reverses) the input path and output path for the shift register (loopback mode).

SPLP2 Bit (RSPI Loopback 2)

The SPLP2 bit selects the mode of the RSPI pins.

When the SPLP2 bit is set to 1, the RSPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path for the shift register (loopback mode).

SPOM Bit (RSPI Output Pin Mode)

For 144-, 120-, 112-, and 100-pin products, the SPOM bit selects CMOS output or open-drain output as the form of output from the RSPI pin. For 64- and 48-pin products, leave this bit at its initial value.

MOIFV Bit (MOSI Idle Fixed Value)

If the MOIFE bit is 1 in master mode, the MOIFV bit determines the MOSIn pin output value during the SSL negation period (including the SSL retention period during a burst transfer).

MOIFE Bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the RSPI in master mode is in an SSL negation period (including the SSL retention period during a burst transfer). When the MOIFE bit is 0, the RSPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIn pin. When the MOIFE bit is 1, the RSPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

・The changes and additions in red text and the deletion in red struck-out text below have been made in Section 32.3.2, Controlling RSPI Pins, and Table 32.6, Relationship between Pin States and Bit Settings, including notes, on Page 1401.

The RSPI can switch pin states is response to the settings of the MSTR, MODFEN, and SPMS bits in SPCR and the SPOM bit in SPPCR. Setting the SPOM bit in SPPCR to 0 selects CMOS output; setting it to 1 selects open-drain output. Table 32.6 lists the relationship between pin states and bit settings. In 64- and 48-pin versions, only the CMOS output mode is supported, so do not set the SPOM bit in SPPCR to 1.

Table 32.6 Relationship between Pin States and Bit Settings

Mode	Pin	Pin State*2	
		SPPCR.SPOM = 0	SPPCR.SPOM = 1*6
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (Clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Slave mode (Clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.

Note 2. RSPI settings are not reflected in the multiplexed pins for which the RSPI function is not selected. ~~If the ODRnBi bit is not present for the corresponding multiplexed pin, the pin is placed in the same state as is indicated for ODRnBi = 0.~~

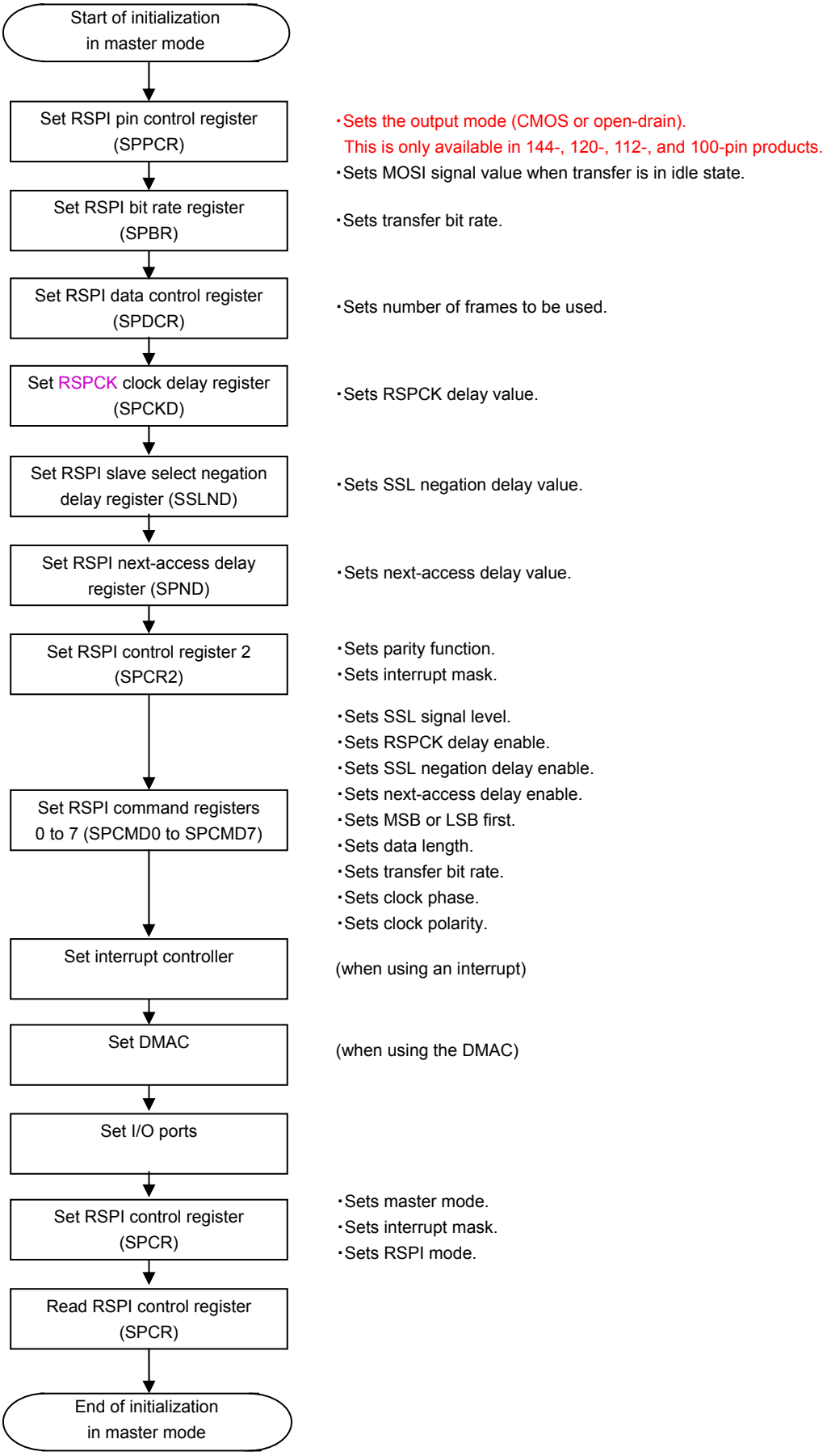
Note 3. When SSLn0 is at the active level, the pin state is Hi-Z.

Note 4. When SSLn0 is at the non-active level or the SPCR.SPE bit is cleared (= 0), the pin state is Hi-Z.

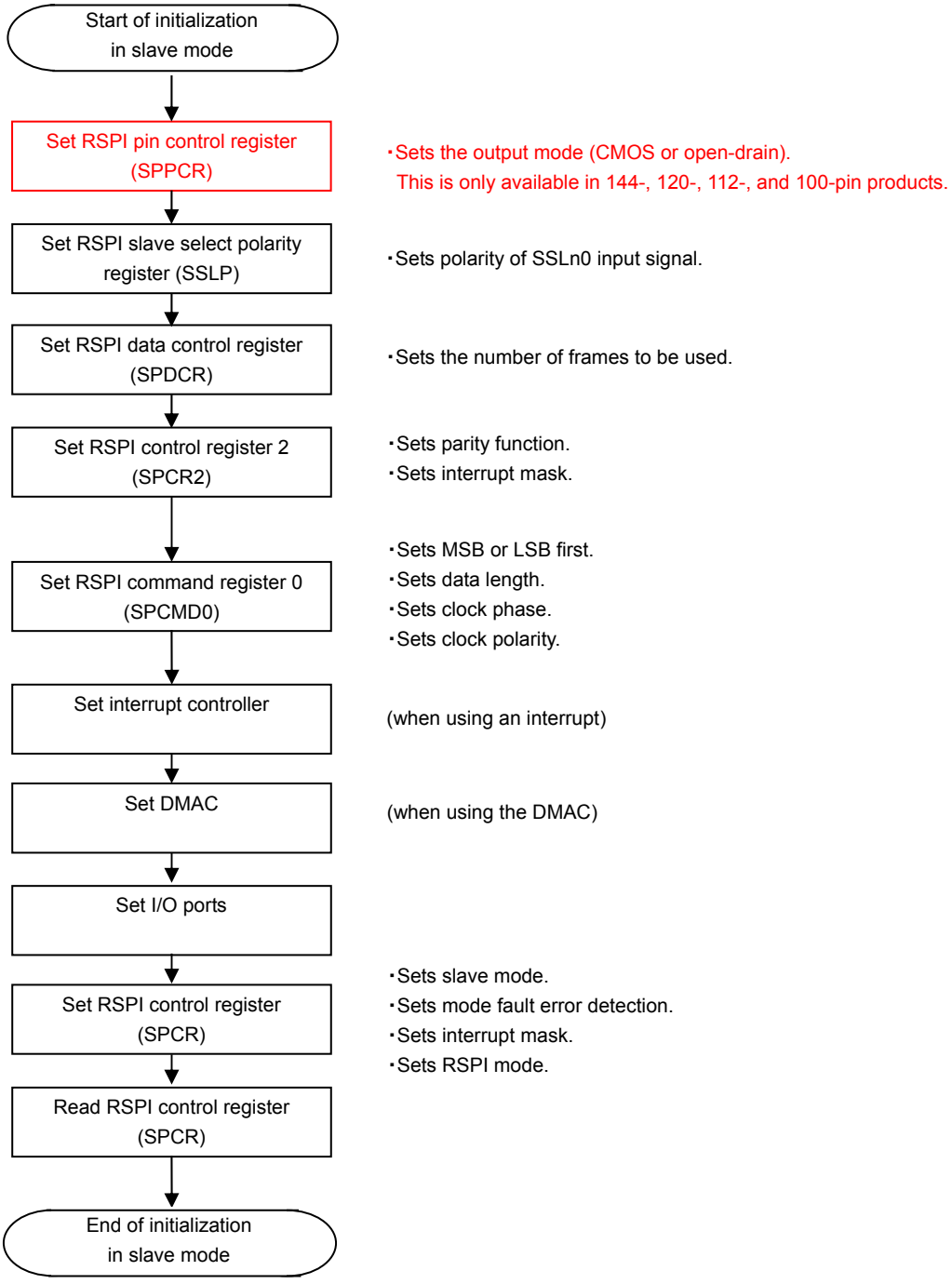
Note 5. These pins are available for use as I/O port pins.

Note 6. Open-drain output is only selectable in 144-, 120-, 112-, and 100-pin products. In 64- and 48-pin products, do not set the SPOM bit in SPPCR to 1.

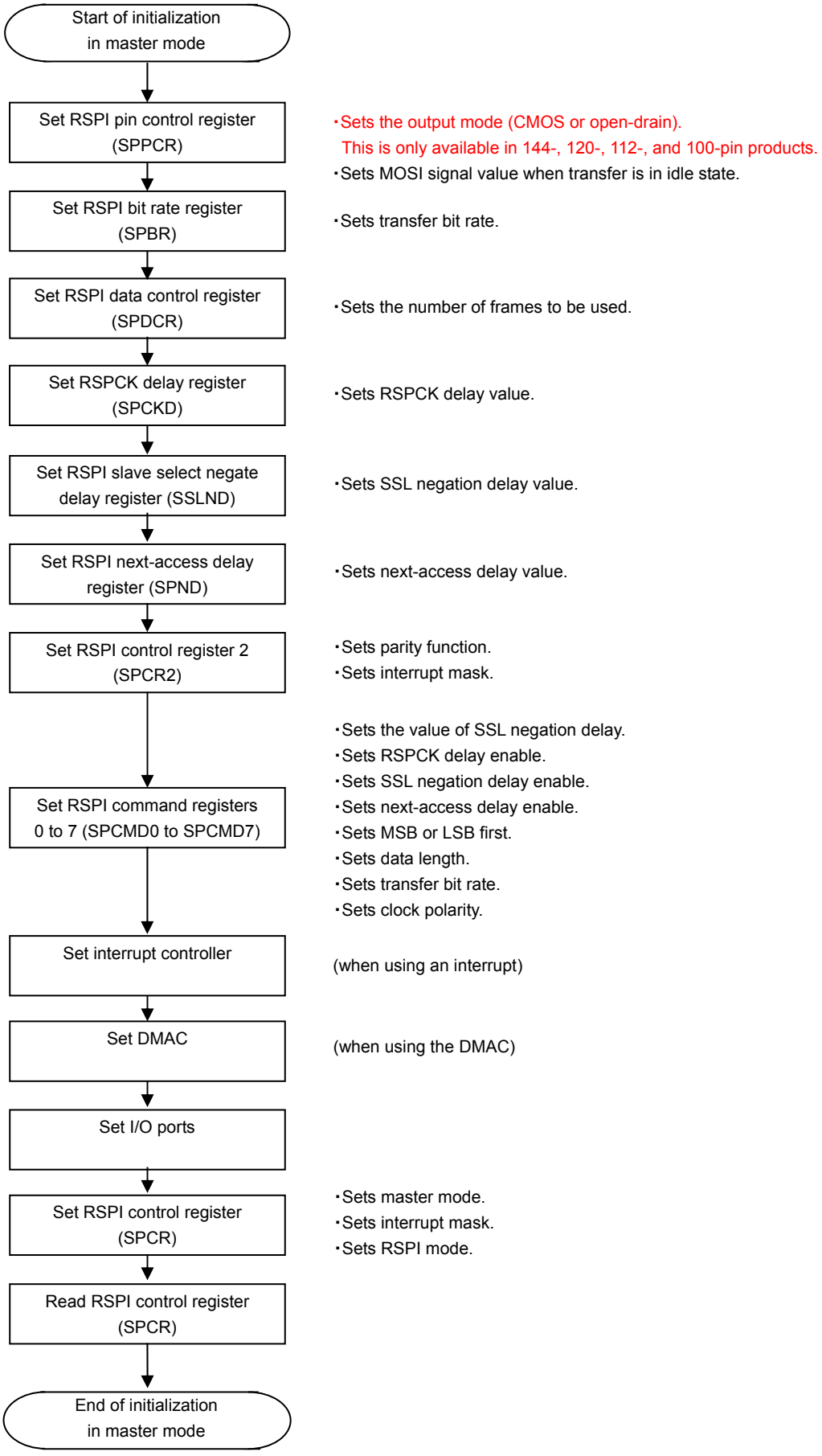
・The red text below was added to Figure 32.34, Example of Initialization Flowchart in Master Mode (SPI Operation), on page 1434.



・The red text below was added to Figure 32.38, Example of Initialization Flowchart in Slave Mode (SPI Operation), on page 1439.



・The red text below was added to Figure 32.45, Example of Initialization Flowchart in Master Mode (Clock Synchronous Operation), on page 1445.



・The red text below was added to Figure 32.46, Example of Initialization Flowchart in Slave Mode (Clock Synchronous Operation), on page 1447.