RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan Renesas Electronics Corporation

Product Category	MPU/MCU				Document No.	TN-V8	5-A012A/E	Rev.	1.00	
Title	Note about the RYO out synchronous serial interf	tput delay time of the clock face (CSIH, CSIG)			Information Category	Technic	Technical Notification			
				Lot No.						
Applicable Product	V850E2/Mx4 series			All lots	Reference Document	User Ma	User Manual of each product			
 Thoro is mod	lification in an electrical ch		f clock ev	(nebronous	sorial interfac			rout dolay	,	
	AS Technical update will m		-					put delay	-	
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1 Madifiaati	ion itomo									
1. Modificati										
	al characteristic change at									
When S	SCKn cycle time (tKCYS) is	s smaller thar	n 8 times	of the Clo	ck source cycle	e (tKCY), 1	cycle tKCY is	added to		
the CSI	n_RYO output delay (tSRI	DYIO).								
There is	s no spec change when SO	CKn cycle tim	e (tKCYS	S) is more	than 8 times of	the Clock	source cycle.			
(2) Electric	al characteristic change at	t the CSIH els	ave mode	a (RYO out	nut delav)					
	al characteristic change a							a addad t		
When S	SCKnF cycle time (tKCYS)	is smaller that				e (tKCY),	1 cycle tKCY i	s added t	:0	
When S	-	is smaller that				ele (tKCY),	1 cycle tKCY i	s added t	0	
When S the CSI	SCKnF cycle time (tKCYS)	is smaller tha RDYIO).	an 8 time	s of the Cl	ock source cyc		-		o	
When S the CSI	SCKnF cycle time (tKCYS) nF_RYO output delay (tSF	is smaller tha RDYIO).	an 8 time	s of the Cl	ock source cyc		-		:0	
When S the CSI	SCKnF cycle time (tKCYS) nF_RYO output delay (tSF	is smaller tha RDYIO).	an 8 time	s of the Cl	ock source cyc		-		O	
When S the CSI There is	SCKnF cycle time (tKCYS) nF_RYO output delay (tSF s no spec change when SC	is smaller tha RDYIO).	an 8 time	s of the Cl	ock source cyc		-		0	
When S the CSI There is 2. Manual m	SCKnF cycle time (tKCYS) nF_RYO output delay (tSF s no spec change when SC	is smaller tha RDYIO). CKnF cycle tir	an 8 time me (tKC\	s of the Cl	ock source cyc		-		0	
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When S the CSI There is 2. Manual m (1) CSIG E The CSI	SCKnF cycle time (tKCYS) nF_RYO output delay (tSF s no spec change when SC <u>nodification</u> Electrical characteristic mod n_RYO output delay time <u>Item</u> n_RYO output delay time	is smaller tha RDYIO). CKnF cycle tir dification poir (tSRDYIO) is	an 8 time me (tKC)	s of the Cl (S) is more as below. <u>Conditio</u> tKCYS	n ≥ 8×tKCY	of the Clock	Source cycle	Unit ns	0	
When S the CSI There is 2. Manual m (1) CSIG E The CSI	SCKnF cycle time (tKCYS) nF_RYO output delay (tSF s no spec change when SC <u>nodification</u> Electrical characteristic mod n_RYO output delay time (from SCKn ↑)	is smaller tha RDYIO). CKnF cycle tir dification poir (tSRDYIO) is Symbol	an 8 time me (tKC) nts changec	s of the Cl (S) is more as below. <u>Conditio</u> tKCYS	n ≥ 8×tKCY < 8×tKCY	of the Clock	MAX. 26.0 26.0 + t _{KCY}	Unit ns ns	0	
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