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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-V85-A034A/E	Rev.	1.00
Title	Misdescription in the electrical characteristics of the bus timing		Information Category	Technical Notification		
Applicable Product	In the main part	Lot No. All lots	Reference Document	User's Manual : Hardware of affected products		

In the User's Manual: hardware of the following Applicable Products of the electrical characteristics of the bus timing, it is corrected as follows.

1. Notification

Misdescription in the electrical characteristics of the bus timing is the item of $\overline{RD}\uparrow \rightarrow \overline{CSn}$ holding time (tHRDC 2).

(1) In multiplexed bus mode/separate bus mode

(a) Read/write cycle (CLKOUT asynchronous)

(T_A = -40～+85℃, $V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$, $V_{SS} = AV_{SS}$ = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Hold time from $\overline{RD}\uparrow \rightarrow \overline{CSn}$	t_{HRDC2}	<31>		(1+i) T - 5		ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

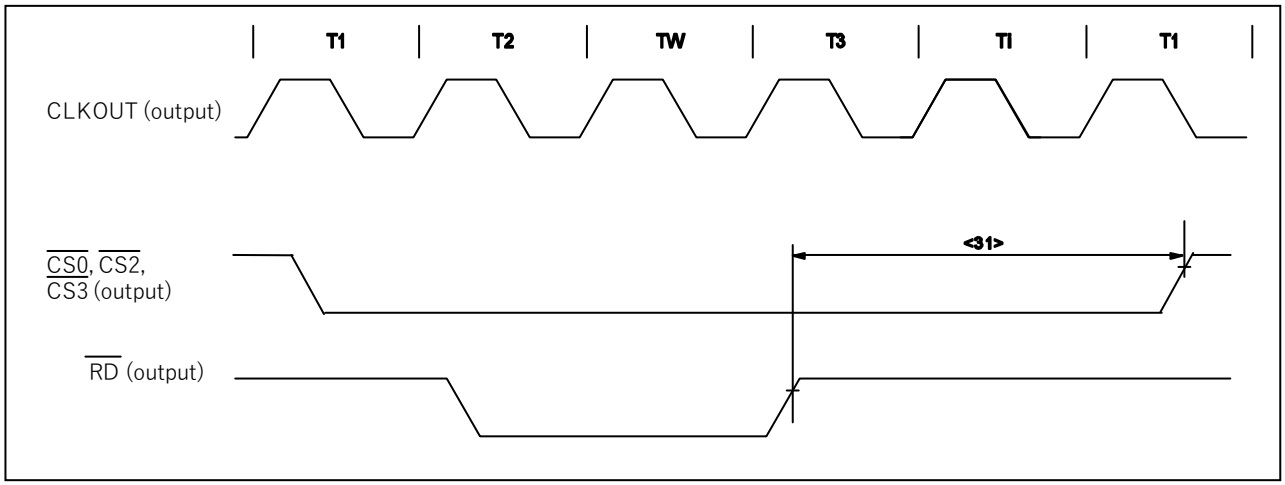
2. n: Number of wait clocks inserted in the bus cycle

The sampling timing changes when a programmable wait is inserted.

3. i: Number of idle states inserted after a read cycle (0 or 1)

4. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Read Cycle (CLKOUT Asynchronous): In Multiplexed Bus Mode/Separate Bus Mode



2. Applicable Products

Products Series			
V850ES/JH3-E	V850ES/JJ3-E	V850ES/JG3-H	V850ES/JH3-H
V850ES/JG3-U	V850ES/JH3-U	V850ES/ST3	