To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Date: Dec.17.2004

RENESAS TECHNICAL UPDATE

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Product Category	Application specific IC		Document No.	TN-ASP-A017A/E	Rev.	1.0
Title	M66291/M66290 Receive Data Length Limitations		Information Category	Technical Notification		
Applicable Product	USB ASSP M66291GP/M66291HP USB ASSP M66290AGP/M66290AFP	Lot No. ALL	Reference Document	M66291GP/HP Datasheet Rev.1.01 M66290AGP/FP Datasheet Rev.1.0		

1. Phenomenon

Concerning EP0_FIFO or CPU_FIFO (Note 1):
After a write to the FIFO Select Register, if data is read from the FIFO Control Register when the FIFO Ready bit = "0", the data length value of the data read from the FIFO Control Register may not be the same as the actual received data length.

2. Occurring Conditions

This phenomenon does not occur in applications that use the receive data length value which was re-read from the FIFO Control Register after the FIFO Ready bit was confirmed to be "0".

This phenomenon occurs when the RCNT setting is "1" and a read to the FIFO Control Register occurs within approximately 21ns (Note 2) after the FIFO Ready bit changes from "1" to "0" after EP0_FIFO or CPU_FIFO data (Note 1) is written to the FIFO Select Register. In this condition, the value will become "the actual receive data length +2".

3. Solutions

This phenomenon can be worked around with any of the following methods:

(1) To abstract the receive data length, wait until after the data is written to the FIFO Select Register, confirm that the FIFO Ready Bit is "0", then re-read the FIFO Control Register.
(2) Set RCNT to "0" in the initial settings to use EP0_FIFO and CPU_FIFO.

(Note 1) The following tables shows the relationship between EP0_FIFO/CPU_FIFO to the FIFO Select Register, the FIFO Ready Bit, and the receive data bit length.

	FIFO Select Register	FIFO Ready Bit	Receive Data Length
EP0_FIFO	EP0_FIFO_SELECT (H'30)	E0_req (H'32:bit11)	ODLN (H'32:bit8-0)
CPU_FIFO	CPU_FIFO_SELECT (H'40)	Creq (H'42:bit11)	CPU_DTLN (H'42:bit10-0)

(Note 2) One clock period at 48MHz = 20.83ns ≒ 21ns.