To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	Application specific IC		Document No.	TN-ASP-A015A/E	Rev.	1.0
Title	M66291 Control transfer status stage transition interrupt Limitations		Information Category	Technical Notification		
Applicable Product	USB ASSP M66291GP,M66291HP	Lot No. ALL	Reference Document	M66291GP/HP Datasheet Rev.1.01		

1.Phenomenon
In system that uses control transfer status stage transition interrupt, control transfer status stage transition interrupt may be incorrect.

2.Occurring Conditions
This limitation does not apply to systems that use (WDST=1 and RDST=1) or (WDST=0 and RDST=0).
This phenomenon occurs when the conditions listed in Type(1) or Type(2) are present.

Type(1)When use WDST=1 and RDST=0:
CTRT is not set to "1" at the time of control write transfer status stage transition.
Type(2)When use WDST=0 and RDST=1:
CTRT is set to "1" at the time of control write transfer status stage transition.

3.Solutions
The phenomenon can be worked around with the following methods.
(1)When M66291 set to CTRT=1 at the time of control write transfer status stage transition .
Please set to WDST=1 and RDST=1.

(2)When M66291 don't set to CTRT=1 at the time of control write transfer status stage transition .
Please set to WDST=0 and RDST=0.

4.Term and definitions
WDST: Control Write Transfer Status Stage (H'10:bit3)
CTRT is set to "1" at the time of WDST=1 and control write transfer status stage transition .
RDST: Control Read Transfer Status Stage (H'10:bit2)
CTRT is set to "1" at the time of RDST=1 and control read transfer status stage transition .
CTRT: Control Transfer Stage Transition Interrupt (H'18:bit11)
This bit is set to “1” when the stage transition of control transfer takes place (control transfer stage transition interrupt occurs).

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