To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Apr.26.2006

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-16C-A151A/E	Rev.	1.00
Title	M32C/80 Series Document Revision for Intelligent I/O Clock Asynchronous Serial I/O Mode (UART)		Information Category	Technical Notification		
Applicable Product	M32C/81 Group, M32C/82 Group M32C/83 Group, M32C/84 Group M32C/85 Group, M32C/86 Group M32C/87 Group, M32C/88 Group	Lot No. ---	Reference Document			

The description of G0TMCR2 register (Group 0 Time Measurement Control Register 2) and G1TMCR2 register (Group 1 Time Measurement Control Register 2) have been revised. When using the subject documents, please pay attention to the changes.

1. Subject Documents

M32C/83 Group (M32C/83,M32C/83T) Hardware Manual Rev. 1.20

M32C/84 Group (M32C/84,M32C/84T) Hardware Manual Rev. 1.01

M32C/85 Group (M32C/85,M32C/85T) Hardware Manual Rev. 1.03

M32C/86 Group (M32C/86,M32C/86T) Hardware Manual Rev. 1.00

M32C/87 Group (M32C/87,M32C/87A,M32C/87B) Hardware Manual Rev. 1.00

M32C/88 Group (M32C/88T) Hardware Manual Rev. 1.10

2. Correction

Refer to the following pages.

M32C/83 Group (M32C/83,M32C/83T) Hardware Manual Rev. 1.20

Page 300 (Table 21.23)

(Before) "$0000\ 0010_2$"

(After) "$0000\ 0011_2$"

Table 21.23 Registers to be Used and Settings

Register	Bit	Function
GiBCR0	BCK1 to BCK0	Set to "11_2"
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
GiBCR1	7 to 0	Set to "$0001\ 0010_2$"
GiPOCR0	7 to 0	Set to "$0000\ 0111_2$"
GiPOCR2	7 to 0	Set to "$0000\ 0110_2$"
GiPOCR3	7 to 0	Set to "$0000\ 0010_2$"
GiTMCR2	7 to 0	Set to "$0000\ 0010_2$"
GiPO0	15 to 0	Set bit rate $\frac{f_{BTi}}{2 \times (\text{setting value} + 2)}$ = transfer clock frequency
GiPO3	15 to 0	Set to a value smaller than the GiPO0 register
GiFS	FSC3 to FSC0	Set to "0100_2"
GiFE	IFE3 to IFE0	Set to "1101_2"
GiMR	GMD1 to GMD0	Set to "00_2"
	CKDIR	Set to "0"
	STPS	Select stop bit length
	UFORM	Select LBS first or MSB first
	IRS	Select how the receive interrupt is generated
GiCR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission
	RE	Set to "1" to enable reception
	IPOL	Set to "1"
	OPOL	Set to "1"
GiTB	7 to 0	Write data to be transmitted
GiRB	15 to 0	Received data and error flag are stored

i = 0 to 1

M32C/84 Group (M32C/84,M32C/84T) Hardware Manual Rev. 1.01

Page 315 (Table 22.22)

(Before) "0000 0010_2"

(After) "0000 0011_2"

Table 22.22 Register Settings in UART Mode (Communication Unit 1)

Register	Bit	Function
G1BCR0	BCK1, BCK0	Set to "11_2" (f_1)
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G1BCR1	7 to 0	Set to "0001 0010_2"
G1POCR0	7 to 0	Set to "0000 0111_2"
G1POCR2	7 to 0	Set to "0000 0110_2"
G1POCR3	7 to 0	Set to "0000 0010_2"
G1TMCR2	7 to 0	Set to "0000 0010_2"
G1PO0	15 to 0	Set bit rate $\frac{f_{BT1}}{2 \times (\text{setting value} + 2)}$ = transfer clock frequency
G1PO3	15 to 0	Set to a value smaller than the G1PO0 register
G1FS	FSC3 to FSC0	Set to "0100_2"
G1FE	IFE3 to IFE0	Set to "1101_2"
G1MR	GMD1, GMD0	Set to "00_2"
	CKDIR	Set to "0"
	STPS	Select length of stop bit
	PRY, PRYE	Select either parity enabled or disabled and either odd parity or even parity
	UFORM	Select either the LSB first or MSB first
	IRS	Select how the receive interrupt is generated
G1CR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission and reception
	RE	Set to "1" to enable reception
	IPOL	Set to "1"
	OPOL	Set to "1"
G1TB	7 to 0	Write data to be transmitted
G1RB	15 to 0	Received data and error flag are stored
CCS	CCS3, CCS2	Set to "00_2"

M32C/85 Group (M32C/85,M32C/85T) Hardware Manual Rev. 1.03

Page 313 (Table 22.22)

(Before) "$0000\ 0010_2$"

(After) "$0000\ 0011_2$"

Table 22.22 Register Settings in UART Mode (Communication Unit 1)

Register	Bit	Function
G1BCR0	BCK1, BCK0	Set to "11_2" (f_1)
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G1BCR1	7 to 0	Set to "$0001\ 0010_2$"
G1POCR0	7 to 0	Set to "$0000\ 0111_2$"
G1POCR2	7 to 0	Set to "$0000\ 0110_2$"
G1POCR3	7 to 0	Set to "$0000\ 0010_2$"
G1TMCR2	7 to 0	Set to "$0000\ 0010_2$"
G1PO0	15 to 0	Set bit rate $\frac{f_{BT1}}{2 \times (\text{setting value} + 2)}$ = transfer clock frequency
G1PO3	15 to 0	Set to a value smaller than the G1PO0 register
G1FS	FSC3 to FSC0	Set to "0100_2"
G1FE	IFE3 to IFE0	Set to "1101_2"
G1MR	GMD1, GMD0	Set to "00_2"
	CKDIR	Set to "0"
	STPS	Select length of stop bit
	PRY, PRYE	Select either parity enabled or disabled and either odd parity or even parity
	UFORM	Select either the LSB first or MSB first
	IRS	Select how the receive interrupt is generated
G1CR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission and reception
	RE	Set to "1" to enable reception
	IPOL	Set to "1"
	OPOL	Set to "1"
G1TB	7 to 0	Write data to be transmitted
G1RB	15 to 0	Received data and error flag are stored
CCS	CCS3, CCS2	Set to "00_2"

M32C/86 Group (M32C/86,M32C/86T) Hardware Manual Rev. 1.00

Page 304 (Table 22.22)

(Before) "0000 0010_2"

(After) "0000 0011_2"

Table 22.22 Register Settings in UART Mode (Communication Unit 1)

Register	Bit	Function
G1BCR0	BCK1, BCK0	Set to "11_2" (f_1)
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G1BCR1	7 to 0	Set to "0001 0010_2"
G1POCR0	7 to 0	Set to "0000 0111_2"
G1POCR2	7 to 0	Set to "0000 0110_2"
G1POCR3	7 to 0	Set to "0000 0010_2"
G1TMCR2	7 to 0	Set to "0000 0010_2"
G1PO0	15 to 0	Set bit rate $\frac{f_{BT1}}{2 \times (\text{setting value} + 2)}$ = transfer clock frequency
G1PO3	15 to 0	Set to a value smaller than the G1PO0 register
G1FS	FSC3 to FSC0	Set to "0100_2"
G1FE	IFE3 to IFE0	Set to "11012"
G1MR	GMD1, GMD0	Set to "00_2"
	CKDIR	Set to "0"
	STPS	Select stop bit length
	PRY, PRYE	Select either parity enabled or disabled and either odd parity or even parity
	UFORM	Select either the LSB first or MSB first
	IRS	Select what causes the receive interrupt to be generated
G1CR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission and reception
	RE	Set to "1" to enable reception
	IPOL	Set to "1"
	OPOL	Set to "1"
G1TB	7 to 0	Write data to be transmitted
G1RB	15 to 0	Received data and error flag are stored
CCS	CCS3, CCS2	Set to "00_2"

M32C/87 Group (M32C/87,M32C/87A,M32C/87B) Hardware Manual Rev. 1.00

Page 344 (Table 22.26)

(Before) "0000 0010_2"

(After) "0000 0011_2"

Table 22.26 Register Settings in UART Mode (Group 1)

Register	Bit	Function
G1BCR0	BCK1, BCK0	Set to "11_2" (f_1)
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G1BCR1	-	Set to "0001 0010_2"
G1POCR0	-	Set to "0000 0111_2"
G1POCR2	-	Set to "0000 0110_2"
G1POCR3	-	Set to "0000 0010_2"
G1TMCR2	-	Set to "0000 0010_2"
G1PO0	-	Set bit rate $\frac{f_{BT1}}{2 \times (\text{setting value} + 2)}$ = transfer clock frequency
G1PO3	-	Set to a value smaller than the G1PO0 register
G1FS	FSC3 to FSC0	Set to "0100_2"
G1FE	IFE3 to IFE0	Set to "1101_2"
G1MR	GMD1, GMD0	Set to "00_2"
	CKDIR	Set to "0"
	STPS	Select stop bit length
	PRY, PRYE	Select either parity enabled or disabled and either odd parity or even parity
	UFORM	Select either the LSB first or MSB first
	IRS	Select what causes the receive interrupt to be generated
G1CR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission and reception
	RE	Set to "1" to enable reception
	IPOL	Set to "1"
	OPOL	Set to "1"
G1TB	-	Write data to be transmitted
G1RB	-	Received data and error flag are stored
CCS	CCS3, CCS2	Set to "00_2"

M32C/88 Group (M32C/88T) Hardware Manual Rev. 1.10

Page 287 (Table 21.22)

(Before) "$0000\ 0010_2$"

(After) "$0000\ 0011_2$"

Table 21.22 Register Settings in UART Mode (Communication Unit 1)

Register	Bit	Function
G1BCR0	BCK1, BCK0	Set to "11_2" (f_1)
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G1BCR1	7 to 0	Set to "$0001\ 0010_2$"
G1POCR0	7 to 0	Set to "$0000\ 0111_2$"
G1POCR2	7 to 0	Set to "$0000\ 0110_2$"
G1POCR3	7 to 0	Set to "$0000\ 0010_2$"
G1TMCR2	7 to 0	Set to "$0000\ 0010_2$"
G1PO0	15 to 0	Set bit rate $\frac{f_{BT1}}{2 \times (\text{setting value} + 2)}$ = transfer clock frequency
G1PO3	15 to 0	Set to a value smaller than the G1PO0 register
G1FS	FSC3 to FSC0	Set to "0100_2"
G1FE	IFE3 to IFE0	Set to "1101_2"
G1MR	GMD1, GMD0	Set to "00_2"
	CKDIR	Set to "0"
	STPS	Select stop bit length
	PRY, PRYE	Select either parity enabled or disabled and either odd parity or even parity
	UFORM	Select either the LSB first or MSB first
	IRS	Select what causes the receive interrupt to be generated
G1CR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission and reception
	RE	Set to "1" to enable reception
	IPOL	Set to "1"
	OPOL	Set to "1"
G1TB	7 to 0	Write data to be transmitted
G1RB	15 to 0	Received data and error flag are stored
CCS	CCS3, CCS2	Set to "00_2"