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April 1st, 2010
Renesas Electronics Corporation

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GRADE A

MAEC TECHNICAL NEWS No.M16C-87-0207

M16C/80 Group Cautions for Using DMA (2)

Classification	Products Effected
Corrections and supplementary explanation of document ✔Notes Knowhow Others	M16C/80 Group

1. Cautions

The followings are additional notes to the MESC Technical News No. M16C-44-0001, cautions in using the DMAC of the M16C/80 group.

(1) While enabling DMA(see Note 1), ensure that a DMA request for the channel is not generated.

(2) After writing to the DMAi request cause select register, wait at least 26 BCLK cycles before enabling DMA by software.

Note 1: "Enabling DMA" means changing the channel i transfer mode select bit (i=0 to 3) of DMA mode registers 0 and 1 is changed from 00b to 01b or 11b.

2. Details

2-1. If a channel i DMA request is generated at the time the channel i DMA is being enabled, the following behavior may occur:

(1) The CPU does not operate properly;

(2) If the DMA requests of the channel i and another channel (referred to as channel j) are generated simultaneously and at the time the channel i DMA is being enabled, channel j DMA request will be ignored (a DMA transfer for channel j will not happen and no interrupt request will be generated).

(3) If the number of transfer of channel i is 1, an interrupt request is not generated after the completion of the channel i DMA transfer (however, the DMA transfer is performed).

(4) If the number of transfer of channel i is 1 and the DMA requests of the channel i and channel j are generated simultaneously and at the time channel i DMA is being enabled, an interrupt request will be generated for channel j but not for channel i (however, both DMA transfers are performed).

2-2. After writing to the DMAi request cause register, if the DMA is enabled within M cycles (see Note 2), the CPU may not run properly.

Note 2: M cycles is equal to 26 cycles (max). This is calculated as 8+6N, where N is the number of other DMA channels (N = Total No. of DMA channels - 1) that may generate a DMA request.

3. Recommended procedure for starting DMA transfer

3-1. When writing to the DMAi request cause register including overwriting the same value to the DMAi request cause register;

(1) Disable the corresponding channel i DMA in DMA mode registers 0 and 1.

(2) Set up the peripheral used as the source of the DMA transfer. However, the peripheral should remain disabled at this time. For example, when using UART0 transmit, disable UART0 transmit.

(3) Set the DMAi request cause select register. At this time, write a '1' to the DMA request bit (bit 7)(see Note 3).

(4) Set the following SFR registers:

- DMAiSFR address register
- DMAi memory address reload register
- DMAi memory address register
- DMAi transfer count reload register
- DMAi transfer count register

(5) At this point, if the number of elapsed cycles are less than 26, add code (NOP's or other processing) to make up some time.

(6) Enable the corresponding channel i DMA in the DMA mode registers 0 and 1.

(7) Enable the peripheral used as the source of the DMA transfer. For example, when using UART0 transmit, enable UART0 transmit.

Note 3: Do not write a '0' to the DMA request bit (bit 7) of the DMAi request cause select register. (It is not necessary to write a '0' to the DMA request bit in your program for the M16C/80 group).

3-2. When not writing to the DMAi request cause register;

(1) Disable the corresponding channel i DMA in the DMA mode registers 0 and 1.

(2) Set up the peripheral used as the source of the DMA transfer. However, the peripheral should remain disabled at this time. For example, when using UART0 transmit, disable UART0 transmit.

(3) Set up the following SFR registers:

- DMAiSFR address register
- DMAi memory address reload register
- DMAi memory address register
- DMAi transfer count reload register
- DMAi transfer count register

(4) Enable the corresponding channel i DMA in the DMA mode registers 0 and 1.

(5) Enable the peripheral used as the source of the DMA transfer. For example, when using UART0 transmit, enable UART0 transmit.

4. Recommended procedure after completing DMA transfer

(1) Disable the peripheral used as source of the DMA transfer to prevent generating a DMA request.

(2) Disable the corresponding channel i DMA in the DMA mode registers 0 and 1.