# Old Company Name in Catalogs and Other Documents

On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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# **RENESAS TECHNICAL UPDATE**

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| Product<br>Category   | MPU&MCU  |                     | Document<br>No.         | TN-SH7-A637A/E   | Rev. | 1.00 |
|-----------------------|--|---------------------|-------------------------|--|------|------|
| Title                 | Limitation of SH7780 DDR-SDRAM bus operating frequency |                     | Information<br>Category | Technical Notification   |      |      |
| Applicable<br>Product | SH7780 (R8A77800A)                                     | Lot No.<br>All lots | Reference<br>Document   | SH7780 Hardware Manual<br>Rev.1.00<br>Dec. 13, 2005<br>(REJ09B0158-0100) |      |      |

When using the DDRIF of the SH7780, specify clock mode 12 and the operating frequency of the DDR-SDRAM bus must not exceed 134 MHz. The DDR-SDRAM cannot use in clock mode 0, 1, 2 and 3.

Note that, regarding this limitation, it has already been fixed by the mask change and the mask-changed product is available

for shipping now. The new part number of the mask-changed product is R8A77800B.

The current product (R8A77800A) that has this limitation will be discontinued.

Please change to the mask-changed product as soon as possible whether or not applied this limitation.

#### [Summary]

When using clock mode 0, 1, 2 or 3 with the following conditions, the internal VDD and ground are influenced, and the access from the DDRIF to the DDR-SDRAM may not be performed correctly. For the system operation, these phenomena cause a read/write error of the DDR-SDRAM.

## [Condition]

When using clock mode 0, 1, 2 or 3 of the SH7780, the DDR-SDRAM bus operating frequency is 134 MHz or more and using the DDRIF with one or more condition of the following 1) to 3).

1) The SH-4A CPU core may operate with maximum power consumption.

2) The input/output pins level of the DDRIF may be alternately repeated high and low.

3) The continuous DMA transfer is performed and the SuperHyway bus transaction of the SH7780 may become high density.

## [Workaround]

When using the DDRIF with above condition, use clock mode 12 and the operating frequency of the DDR-SDRAM bus must not exceed 134 MHz.

Note that, the VDD/VDD-PLL power supply would be set highly as possible and stable.

- End of text -

