To our customers,

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# HITACHI SEMICONDUCTOR TECHNICAL UPDATE

| Classification of Production | MCU | | | No | TN-SH7-402B/E | |
|---|---|---|---|---|---|---|
| THEME | Information about bug with FDIV on SH7055RF | Classification of Information | 1. Spec change<br>2. Supplement of Documents<br>③ Limitation of Use | 4. Change of Mask<br>5. Change of Production Line | | |
| PRODUCT NAME | SH7055RF | Lot No.<br>SH7055RF :ALL lots | Reference Documents | SH-2E Programming Manual Rev.1.0 ADE-602-178 | Rev.<br>2.0 | Effective Date<br>Unlimited |

We would like to inform you that there is a bug with FDIV on SH7055RF.

1 Phenomena

When 1) there are only CPU instructions (see below) between FDIV and FPU instruction (see below) which refers to the destination of the FDIV, 2) the last E1 stage of the FDIV and the D stage of the FPU instruction overlap, and 3) the E1 stage is more than one cycle by system clock, the FPU instruction can't use the result of FDIV and will use the value of former FRn . (Nonetheless the result of FDIV is OK.)

[FPU instruction which refers to the destination of the FDIV]

| instruction | register to be referred |
|---|---|
| FABS FRn | : FRn |
| FADD FRm, FRn | : FRm, FRn |
| FCMP/EQ FRm, FRn | : FRm, FRn |
| FCMP/GT FRm, FRn | : FRm, FRn |
| FDIV FRm, FRn | : FRm, FRn |
| FLDS FRm, FPUL | : FRm |
| FMAC FR0, FRm, FRn | : FR0, FRm, FRn |
| FMOV FRm, FRn | : FRm |
| FMOV.S FRm, @(R0,Rn) | : FRm |
| FMOV.S FRm, @ Rn | : FRm |
| FMOV.S FRm, @Rn | : FRm |
| FMUL FRm, FRn | : FRm, FRn |
| FNEG FRn | : FRn |
| FSUB FRm, FRn | : FRm, FRn |
| FTRC FRm, FPUL | : FRm, |

[ CPU instruction ]

Any instructions of Table 6.3, Table 6.4, Table 6.5, Table 6.6, Table 6.7 and Table 6.8 in SH-2E programming manual Rev1.0.

We would like to show two examples about this bug.

[ Example 1]

In this example, FDIV operates FR1/FR0 -> FR1, and then FMUL at the 13th instruction after FDIV operates FR1 x FR2 -> FR2. If the number of the fetch cycle of the next instruction of FMUL is more than one cycle, the number of the last E1 cycle of FDIV is extended to more than one cycle due to it. So there is no stall stage in FMUL and FMUL uses the FR1 value before FDIV operation, not the FR1 value after FDIV operation. But FDIV operates itself correctly.

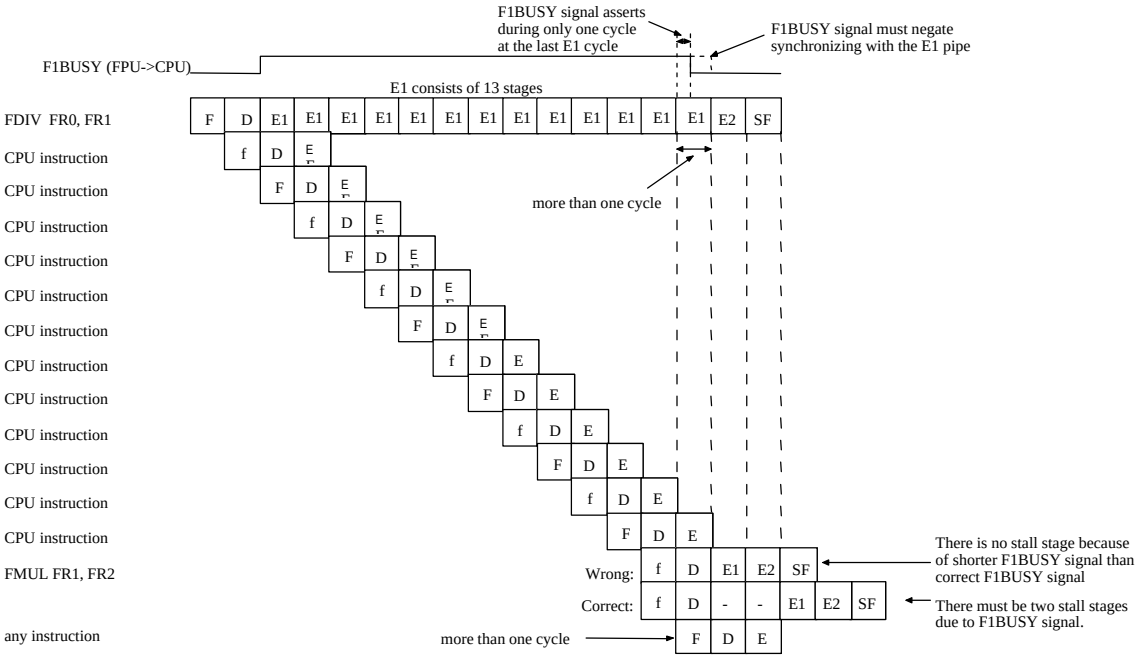


Fig1. Example 1 about bug with FDIV

[ Example 2]

In this example, FDIV operates FR1/FR0 -> FR1, and then FMUL at the 13th instruction after FDIV operates FR1 x FR2 -> FR2. If the 2nd instruction before FMUL operates memory access which is more than one cycle and there is no IF-MA contention at the memory access, the number of the last E1 cycle of FDIV is extended to more than one cycle due to it. So there is no stall stage in FMUL and FMUL uses the FR1 value before FDIV operation, not the FR1 value after FDIV operation. But FDIV operates itself correctly.

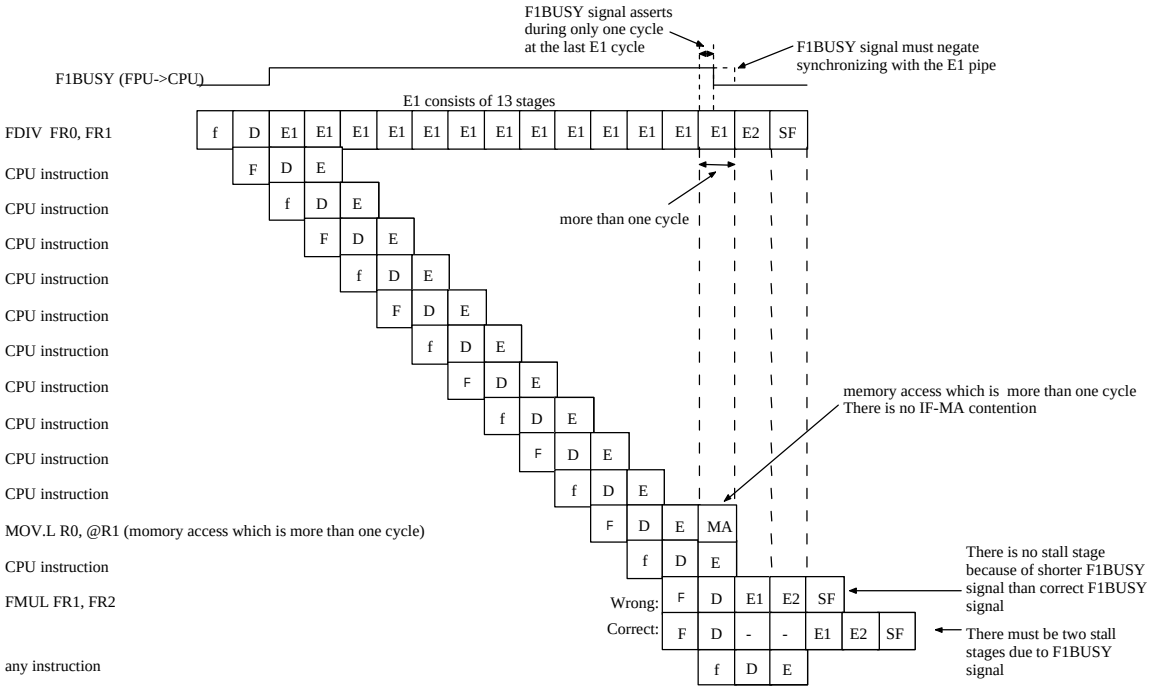


Fig2. Example 2 about bug with FDIV

2 Cause

As shown in Fig 1 and Fig 2, the F1BUSY signal is the control signal from FPU to CPU, which asserts during E1 stages of FDIV to prevent CPU in the pipe of FPU instruction to proceed during FDIV operation.

If the F1BUSY signal asserts at the D stage of FPU instruction, CPU stalls the E1 stage of the FPU instruction until the end of the FDIV operation.

Therefore, F1BUSY signal must negate synchronizing with the E1 stage of FDIV. But FPU negates F1BUSY signal at the one cycle of the last E1 stage.

So there is no stall stage of the FPU instruction, which refers to the result of FDIV, because CPU judges that FDIV operation has already finished. Then the FPU instruction uses the value before FDIV operation.

3 Case where this bug occurs

The case where this bug occurs is limited in next

(1) [ There are only CPU instructions(see Page 1) between FDIV and the FPU instruction which refers to the result of the FDIV]

And

(2) [ The D stage of the FPU instruction which refers to the result of the FDIV overlaps the last E1 stage of the FDIV]

And

(3) [ The last E1 stage of the FDIV is more than one cycle ] which means

1) [ The fetch cycle of the next instruction of the FPU instruction is more than one cycle ]
Example 1 of Fig 1 is an example of this. There is no this case if the program is located on the internal flash memories and rams.

Or

2) [ The last E1 stage of the FDIV overlaps MA stage of more than one cycle and there is no IF-MA contention]
Example 2 of Fig 2 is an example of this. There is no this case if there is no instruction with MA of more than one cycle at one or two instruction before the FPU instruction.

Or

3) [ DMA cycle, AUD cycle or bus release extends the last E1 stage ]

If you uses LSI under single chip mode, there is no (3)-1) case and (3)-2) case is limited to the case that [ The last E1 stage of the FDIV overlaps I/O-MA stage and there is no IF-MA contention].

4 Lot No. etc.

SH7055RF:ALL lots

5 Plan to fix the bug

SH7055RF: We are very sorry that we would like to keep it unchanged. We would like to fix this bug for our successor product. We appreciate your patience.

We prepared a check program which checks if this bug exists in your application under mass production. When an error or a warning message comes out from the check program, the portion where the message comes from needs to be analyzed if this bug occurs at pipeline execution. Please contact us for the check program and pipeline execution analysis.

Hitachi compilers will be modified to output code which will not generate this bug. The schedule and version of the compilers are followings.

| Compiler Version | Product No. | Schedule |
|---|---|---|
| SHC Compiler Ver5.1 : | P0700CAS5-MWR (Windows version only) | Sep-02 |
| SHC Compiler Ver6.0 : | P0700CAS6-MWR | Sep-02 |
| | P0700CAS6-H7R | Sep-02 |
| | P0700CAS6-SLR | Sep-02 |
| SHCCompiler Ver7.1 : | P0700CAS7-MWR | Sep-02 |
| | P0700CAS7-H7R | Sep-02 |
| | P0700CAS7-SLR | Sep-02 |