Microcomputer Technical Information

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IE-78K0K1-ET In-Circuit Emulator for 78K0/KB1, KC1, KD1, KE1, KF1, KB1+, KC1+, KD1+, KE1+, KF1+ Usage Restrictions		Document No.	ZBG-CD-04-0077		1/2
		Date issued	September 28, 2004		
		Issued by	Development Tool Group Multipurpose Microcomputer Systems Division 3rd Systems Operations Unit NEC Electronics Corporation		
Related documents	IE-78K0K1-ET Preliminary User's Manual: U16604EJ1V0UM00	Notification classification	√	Usage restriction	
				Upgrade	
				Document modification	
				Other notification	

1. Affected product

   IE-78K0K1-ET Control code[Note]: A, B, C, D

2. Details of restrictions

   Bugs No. 14 to No. 18 have been corrected. See the attachment for details.

3. Workarounds

   See the attachment for details.

4. Modification schedule

   Products in which No. 14 to No. 18 are modified are scheduled for release as follows.

   Newly shipped products: From the shipment of October 2004 (control code: D)

   Upgrade for already shipped products: Available from October 2004

   * Note that this schedule is subject to change without notice. For the detailed release schedule of modified products, contact an NEC Electronics sales representative.

5. List of restrictions

   See the attachment.

Note The "control code" is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased. If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

6. Document revision history

IE-78K0K1-ET In-Circuit Emulator for 78K0/KB1, KC1, KD1, KE1, KF1, KB1+, KC1+, KD1+, KE1+, KF1+

Usage Restrictions

Document Number	Issued on	Description
SBG-DT-03-0074-E	February 26, 2003	Addition of bugs (No. 1 to No. 10)
SBG-DT-04-0114	March 12, 2004	Addition/change of specification (No. 11 to No. 14)
ZBG-CD-04-0035	July 8, 2004	Addition of bugs (No. 15 to No. 18) Addition of attachment 2
ZBG-CD-04-0077	September 28, 2004	Correction of bugs (No. 14 to No. 18)

Notes on Using IE-78K0K1-ET

1. Product Version

Control Code[Note]	Remark
A	μPD78F0148GC 2.0
B	μPD78F0148GC 2.1
C	μPD78F0148HGC 1.0
D	μPD78F0148HGC 1.2

Note The "control code" is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased. If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code[Note]			
		A	B	C	D
1	The initial value of the SFR PCC differs between the target device and IE system	Permanent restriction			
2	The connection of the $\overline{\text{RESET}}$ pin differs from that in the target device	Permanent restriction			
3	Do not use an accessing method that generates a wait request for the WDTM, ASIS0, ASIS6, ADM, ADS, PFM, PFT, and ADCR registers when operating with the subsystem clock and with the input clock stopped	Permanent restriction			
4	SFRs may not be able to be accessed when operating at a frequency of over 5 MHz and at 3.3 to 4.0 V	×	√	√	√
5	Transmit data cannot be written to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0) of the target device 78K0/KF1	×	√	√	√
6	The values of the RESF, LVIM, and LVIS registers are initialized by applying a reset from the target system even if RESET is masked	Permanent restriction			
7	The values of the RESF, LVIM, and LVIS registers are not initialized by the CPU reset button of the integrated debugger ID78K0-NS	Permanent restriction			
8	Some restrictions apply if Break (peripheral functions stopped) is specified as Peripheral Break in the Configuration dialog box of the integrated debugger ID78K0-NS	Permanent restriction			
9	The long-type emulation probe for 80-pin package cannot be used	×	√	√	√
10	An internal reset may not be generated by the watchdog timer	×	√	√	√
11	The integrated debugger may not start when it is restarted	×	×	√	√
12	Some 78K0/Kx1+ functions are now supported [Addition of specification]	–	–	√	√
13	Restrictions on using 78K0/Kx1+	Permanent restriction			
14	Bug related to RINGMSK operation during HALT	×	×	×	√
15	Bug related to reset	×	×	×	√
16	Bug related to STOP mode	×	×	×	√

×: Restriction applies
√: Restriction does not apply or already corrected
–: Specification not supported

No.	Bugs and Changes/Additions to Specifications	Control Code[Note]			
		A	B	C	D
17	Bug related to conflict between write to SFR in which a wait occurs and interrupt	√	√	×	√
18	Bug related to conflict between SFR access and interrupt	√	√	×	√

×: Restriction applies
√: Restriction does not apply or already corrected
–: Specification not supported

3. Details of Bugs and Additions to Specifications

No. 1 The initial value of the SFR PCC differs between the target device and IE system.

[Description]

The initial value of the SFR PCC differs between the target device and IE system.

Target device: 00H IE system: 04H

[Workaround]

Set 00H when the target device is started or reset.

Regard this as a permanent restriction.

No. 2 The connection of the $\overline{\text{RESET}}$ pin differs from that in the target device.

[Description]

The connection of the $\overline{\text{RESET}}$ pin differs from that in the target device.

Target device: Without pull-up IE system: 4.7 kΩ pull-up in the IE system

[Workaround]

There is no workaround. Regard this as a permanent restriction.

No. 3 Do not use an accessing method that generates a wait request for the WDTM, ASIS0, ASIS6, ADM, ADS, PFM, PFT, and ADCR registers when operating with the subsystem clock and with the input clock stopped

[Description]

Do not use an accessing method that generates a wait request for the WDTM, ASIS0, ASIS6, ADM, ADS, PFM, PFT, and ADCR registers when operating with the subsystem clock and with the input clock stopped.

[Workaround]

LED2 (RETRY) that indicates the wait (retry) status stays lit in the IE system, the integrated debugger ID78K0-NS hangs up. Apply a reset by using either of the following methods to restore from the hang-up status.

- Reset applied from a circuit on the target device
- Internal reset by comparing the power supply voltage of the POC circuit and detection voltage
- Internal reset by comparing the power supply voltage of the low-voltage detector (LVI) and detection voltage
- Clock monitor reset by pressing emulation switch SW2 on the clock monitor

Regard this as a permanent restriction.

No. 4 SFRs may not be able to be accessed when operating at a frequency of over 5 MHz and at 3.3 to 4.0 V

[Description]

SFRs may not be able to be accessed when operating at the following frequency and voltage.

Voltage	Frequency
3.3 to 4.0 V	Over 5 MHz

[Workaround]

There is no workaround.

This restriction has been corrected in control code B.

No. 5 Transmit data cannot be written to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0) of the target device 78K0/KF1

[Description]

When writing transmit data to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0) of the target device 78K0/KF1, data may not be written correctly depending on the instruction executed after the write instruction (see SBG-DT-0128-E for details).

[Workaround]

See [Workaround] (3) in SBG-DT-0128-E.

This restriction has been corrected in control code B.

No. 6 The values of the RESF, LVIM, and LVIS registers are initialized by applying a reset from the target system even if RESET is masked

[Description]

The values of the RESF, LVIM, and LVIS registers are initialized by applying a reset from the target system to the IE system even if RESET is masked in the Configuration dialog box of the integrated debugger ID78K0-NS. (The values of other registers are not initialized.)

[Workaround]

There is no workaround. Regard this as a permanent restriction.

No. 7 The values of the RESF, LVIM, and LVIS registers are not initialized by the CPU reset button of the integrated debugger ID78K0-NS.

[Description]

The values of the RESF, LVIM, and LVIS registers are not initialized by the CPU reset button of the integrated debugger ID78K0-NS.

[Workaround]

Initialization can be implemented using the following resets.

<RESF register>

- Reset applied from a circuit on the target device

- Internal reset by comparing the power supply voltage of the POC circuit and detection voltage

<LVIM and LVIS registers>

- Reset applied from a circuit on the target device
- Internal reset by comparing the power supply voltage of the POC circuit and detection voltage
- Clock monitor reset by pressing emulation switch SW2 on the clock monitor
- Reset applied from the watchdog timer

Regard this as a permanent restriction.

No. 8 Some restrictions apply if Break (peripheral functions stopped) is specified as Peripheral Break in the Configuration dialog box of the integrated debugger ID78K0-NS

[Description]

(1) Prohibition of write

Do not write data to the TMC00, TMC01, WDTM, ADM, ADS, PFM, and PFT registers in the SFR window and Watch window and the buffer RAM area in the Memory window (there is no problem if data is written by the program.).

(2) Restriction on display

The value of the ADCR register in the SFR window and Watch window is illegal (there is no problem when Non Break is specified. In addition, there is no problem with the read value in the program.)

(3) Restriction on non-real-time execution

Writing to the TMC00, TMC01, WDTM, ADM, ADS, PFM, and PFT registers and the buffer RAM area may not be performed when a non-real-time execution (step-in, next over, or slowmotion) is performed.

(4) Restriction on break immediately before/after write operation to I/O register that generates a wait

Writing to the TMC00, TMC01, WDTM, ADM, ADS, PFM, and PFT registers and the buffer RAM area may not be performed normally when a break is set immediately before/after the write operation.

[Workaround]

There is no workaround. Regard this as a permanent restriction.

No. 9 The long-type emulation probe for 80-pin package cannot be used

[Description]

The long-type emulation probe for 80-pin package (NP-H80GC-TQ and NP-H80GK-TQ) cannot be used.

[Workaround]

There is no workaround. This restriction has been corrected in control code B.

No. 10 An internal reset may not be generated by the watchdog timer

[Description]

An internal reset may not be generated by the watchdog timer.

[Workaround]

There is no workaround. This restriction has been corrected in control code B.

No. 11 The integrated debugger may not start when it is restarted

[Description]

The integrated debugger may not start after it is shut down and restarted.

[Workaround]

Be sure to disconnect the power supply to the IE-78K0K1-ET after the integrated debugger is shut down.

This restriction has been corrected in control code C.

No. 12 Some 78K0/Kx1+ functions are now supported. [Addition of specification]

[Description]

Some 78K0/Kx1+ functions are now supported in control code C, but restrictions apply.

See No. 13 for details.

No. 13 Restrictions on using 78K0/Kx1+

[Description]

(1) Accessing the system control register (VSWC) is not possible. VSWC operates with the initial value 0H.

(2) An operating voltage lower than 2.5 V is not supported.

- The POC function of the device generates a POC reset when the voltage becomes 2.1 ±0.1 V, but the target voltage cannot be set to lower than 2.5 V in the IE-78K0K1-ET. Therefore, the POC reset cannot be emulated in the IE-78K0K1-ET.
- A detection voltage (VLVI) of 2.35 ±0.1 V cannot be used for the LVI function. Use a detection voltage of 2.6 ±0.1 V or higher.

(3) The self-programming function is not supported.

(4) The boot swap function is not supported.

(5) The maximum operating frequency of the device is 16 MHz, but the IE-78K0K1-ET does not support operation at a frequency higher than 12 MHz. Therefore, use the IE-78K0K1-ET with an operating frequency of 12 MHz or lower.

(6) The option byte function is not supported. Set RINGOSC using the mask option of the debugger.

[Workaround]

There is no workaround. Regard this as a permanent restriction.

No. 14 Bug related to RINGMSK operation during HALT

[Description]

The watchdog timer operation does not stop even if NONMSK (Ring-OSC can be stopped by software) is set for the mask option RINGMSK and the HALT instruction is executed, as long as the operation clock to the watchdog timer does not stop. As a result, a reset signal is generated.

[Workaround]

There is no workaround. This bug has been corrected in control code D.

No. 15 Bug related to reset

[Description]

The reset vector may be illegal after a reset.

[Workaround]

There is no workaround. This bug has been corrected in control code D.

No. 16 Bug related to STOP mode

[Description]

When an interrupt occurs in STOP mode, an interrupt flag is set but the interrupt vector may be illegal.

[Workaround]

There is no workaround. This bug has been corrected in control code D.

No. 17 Bug related to conflict between write to SFR in which a wait occurs and interrupt

[Description]

If a conflict occurs between writing to an SFR (TMC00, WDTM, ADM, ADS, PFM, or PFT) in which a wait occurs or writing to the buffer RAM and an interrupt, the interrupt vector may be illegal.

[Workaround]

There is no workaround. This bug has been corrected in control code D.

No. 18 Bug related to conflict between SFR access and interrupt

[Description]

If an interrupt occurs while accessing an SFR related to the functions shown below, the interrupt vector may be illegal. However, this bug does not occur in operation at a frequency of 12 MHz or lower.

Ports (except for 4, 5, and 6), A/D converter, 16-bit timer 0, 8-bit timer, watchdog timer, low-voltage detector, UART0, UART6, CSI1, CSIA0, watch timer, key interrupt, and registers for multiplication/division

[Workaround]

There is no workaround. This bug has been corrected in control code D.

4. Cautions

No. 1 LED3 (POC RESET)

[Description]

LED3 (POC RESET) is lit during the reset shown below. Do not perform a break when LED3 is lit; otherwise the integrated debugger ID78K0-NS will hang up.

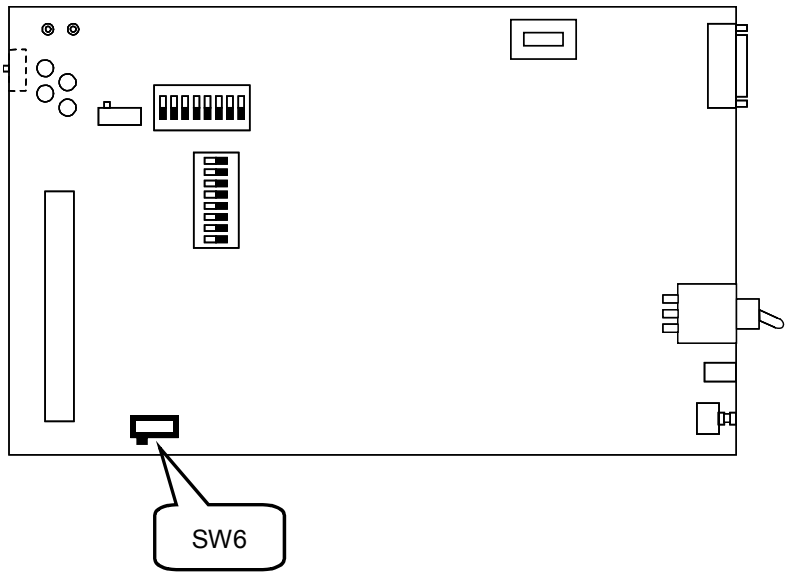
- Internal reset by comparing the power supply voltage and detection voltage of the POC circuit

No. 2 SW6

[Description]

Use SW6 in the default setting (3-side). (SW6 is a switch used for maintenance.)

Package Drawing of Emulation board (S-780148 Board)



No. 3 Product information

[Description]

NEC Electronics' Microcomputer website (http://www.necel.com/micro/index_e.html) provides product information, FAQs on development tools, the latest development tools, user's manuals, and a device file download service, etc.

No. 4 General cautions on handling this product

a) Circumstances not covered by product guarantee

- If the product was disassembled, altered, or repaired by the customer
- If it was dropped, broken, or given another strong shock
- Use at overvoltage, use outside guaranteed temperature range, storing outside guaranteed temperature range

- If power was turned on while the AC adapter, interface cable, or target system connection was in an unsatisfactory state
- If the AC adapter cable, interface cable, emulation probe, or the like was bent or pulled excessively
- If an AC adapter other than the one supplied with the product is used
- If the product got wet
- If the product and target system were connected while a potential difference existed between the GND of the product and the GND of the target system
- If a connector or cable was removed while the power was being supplied to the product
- If an excessive load was placed on a connector or socket

b) Safety precautions

- If used for a long time, the product may become hot (50°C to 60°C). Be careful of low temperature burns and other dangers due to the product becoming hot.
- Be careful of electrical shock. There is a danger of electrical shock if the product is used as described above in **a) Circumstances not covered by product guarantee**.

5. Difference Manual

This section explains changes from control code C and differences from the user's manual.

Target manual: IE-78K0K1-ET In-Circuit Emulator Preliminary User's Manual (document number: U16604E)

(1) Addition of 78K0/KB1+, 78K0/KC1+, 78K0/KD1+, 78K0/KE1+, 78K0/KF1+ to target devices

[Location] Cover, pages 3, 6, 8, 10, and 17

(2) Change of supported low-voltage range from "2.7 V to 5.5 V" to "2.5 V to 5.5 V"

[Location] Page 10

(3) Deletion of SW8

[Location] Pages 13, 14, and 31

(4) Change of description of PD78F0148 to PD78F0148H in figures

[Location] Pages 23 and 29

(5) Change of description "2.0 MHz to 10.0 MHz" to "2.0 MHz to 12.0 MHz"

[Location] Page 24

(6) Addition of multiplication circuit setting

[Location] Page 32

Main System Clock Frequency	SW2	SW3
10 MHz to 12 MHz	1, 6 ON (Other: OFF)	4, 6 ON (Other: OFF)

(7) Deletion of **3.10**

[Location] Page 33

(8) Addition of 78K0/KB1+ to target devices

[Location] Page 35

(9) Addition of 78K0/KC1+ to target devices

[Location] Page 39

(10) Addition of 78K0/KD1+ to target devices

[Location] Page 43

(11) Addition of 78K0/KE1+ to target devices

[Location] Page 47

(12) Addition of 78K0/KF1+ to target devices

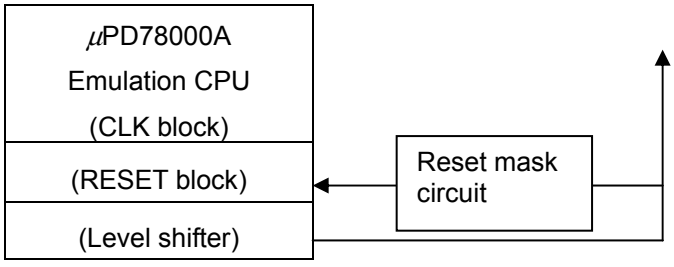
[Location] Page 51

(13) Change of emulation CPU from μPD78F0148 to μPD78F0148H

[Location] Pages 35 to 37, 39 to 41, 43 to 45, 47 to 49, and 51 to 53

(14) Addition of reset mask circuit

[Location] Pages 37, 41, 45, 49, and 53



(15) Addition of case for 78K0/Kx1+ to mask option settings

[Location] Page 33

(a) When target device is 78K0/Kx1

- Ring-OSC
- POC ON/OFF and detection voltage 2.85 V, 3.5 V
- P60 to P63 (these ports are not provided in the μPD780101, 780102, 780103, and 78F0103)

Set the mask options in the integrated debugger.

Open the mask option window from [Option] → [Mask Option] and set the mask options.

Refer to the ID78K0-NS Ver.2.52 Integrated Debugger Operation (U16488E) for details.

• RINGMSK	NONMSK	Ring-OSC stop by software enabled Watchdog timer stop enabled
	MSK	Ring-OSC stop by software disabled Watchdog timer stop disabled
• POC	ON	POC function ON
	OFF	POC function OFF
• POCV	2.85 V	POC detection voltage 2.85 V
	3.5 V	POC detection voltage 3.5 V
• P60 to P63	ON	Pulled up by the mask option resistor
	OFF	No mask option resistor

(b) When target device is 78K0/Kx1+

• Ring-OSC

Set the mask options in the integrated debugger.

Open the mask option window from [Option] → [Mask Option] and set the mask options.

Refer to the ID78K0-NS Ver.2.52 Integrated Debugger Operation (U16488E) for details.

• RINGMSK	NONMSK	Ring-OSC stop by software enabled Watchdog timer stop enabled
	MSK	Ring-OSC stop by software disabled Watchdog timer stop disabled

Caution When emulating the 78K0/Kx1+, "78K0Kx1plus" is displayed in the mask option window, but this does not need to be set.