To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A291A/E	Rev.	1.00
Title	H8S/2633 Series and H8S/2643 Series Notes on the SCL rise time in the I^2C bus interface module		Information Category	Technical Notification		
Applicable Product	H8S/2633W Series H8S/2643W Series	Lot No. All lots	Reference Document	Following hardware manuals: H8S/2633 Series Rev. 5.00 H8S/2643 Series Rev. 3.00		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the usage notes on the SCL rise time in the I^2C bus interface module.

1. Target Function

   I^2C bus interface module

2. Usage Notes

   When the master mode is set in the I^2C bus interface module, the SCL high period may be shortened in the following three conditions;

- when SCL is driven low by the slave device.
- when SCL rises slowly due to the load capacitance and pull-up resistance of the SCL line.
- when ϕ exceeds 20 MHz in the 7.5 t_{cyc} transfer rate.

Therefore, SCL is monitored and synchronized for each bit during communication. Figure 1 shows the bit synchronization circuit timing, and table 1 lists the permissible range of the SCL rise time (t_{sr}). If SCL does not rise within the permissible range (7.5 t_{cyc} or 17.5 t_{cyc}) of the SCL rise time (t_{sr}), the internal SCL high period is extended to the next rate.

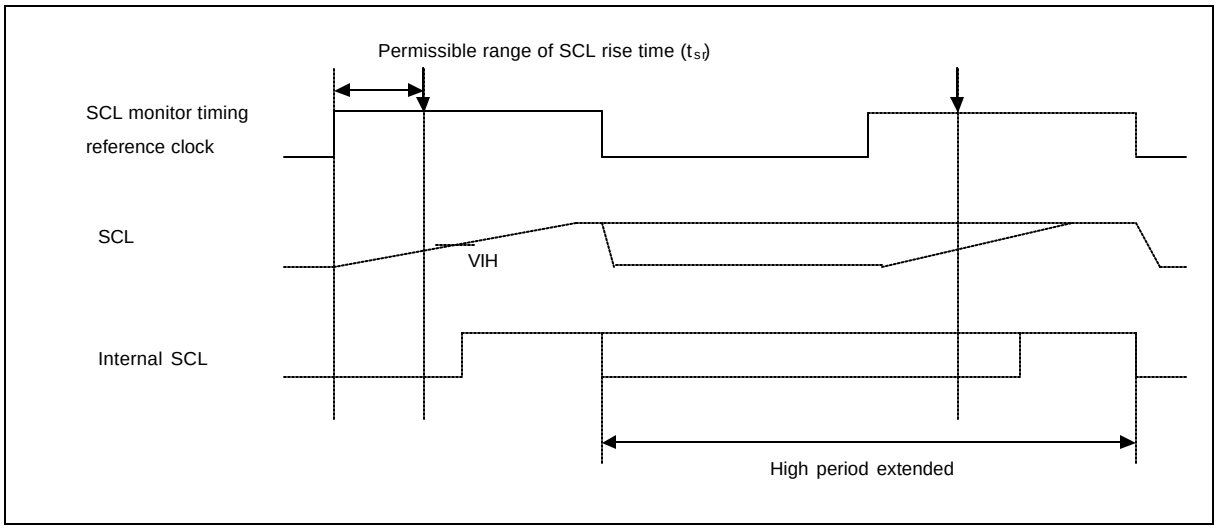

Figure 1 Bit Synchronization Circuit Timing

Table 1 Permissible Range of SCL Rise Time (t_{sr})

[Before change]

IICX	t_{cyc} Indication		Time Indication: I^2C Bus Specification (max.)	f = 5 MHz	f = 8 MHz	f = 10 MHz	f = 16 MHz	f = 20 MHz	f = 25 MHz	f = 28 MHz
0	7.5 t_{cyc}	Standard mode	1000 ns	1000 ns	937 ns	750 ns	468 ns	375 ns	300 ns	267 ns
		High-speed mode	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns
1	17.5 t_{cyc}	Standard mode	1000 ns	1000 ns	1000 ns	1000 ns	1000 ns	875 ns	700 ns	624 ns
		High-speed mode	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns

[After change]

IICX	t_{cyc} Indication		Time Indication: I^2C Bus Specification (max.)	f = 5 MHz	f = 8 MHz	f = 10 MHz	f = 16 MHz	f = 20 MHz	f = 25 MHz	f = 28 MHz
0	7.5 t_{cyc}	Standard mode	1000 ns	1000 ns	937 ns	750 ns	468 ns	375 ns	—	—
		High-speed mode	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	—	—
1	17.5 t_{cyc}	Standard mode	1000 ns	1000 ns	1000 ns	1000 ns	1000 ns	875 ns	700 ns	624 ns
		High-speed mode	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns

Note: When ϕ exceeds 20 MHz in the 7.5 t_{cyc} transfer rate, the transfer rate may be extended.

3. Manual Description Change

As shown in table 1, the permissible range of SCL rise time (t_{sr}) is changed and the note is added.