To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A355A/E	Rev.	1.00
Title	H8/38099 Group About the change of the electrical characteristics		Information Category	Technical Notification		
Applicable Product	H8/38099 Group	Lot No. All	Reference Document	H8/38099 Group Hardware Manual (REJ09B0309-0100)		

We would like to inform you about the change of the electrical characteristics for H8/38099 Group.

Change part 1

Section 26 Electrical Characteristics

26.2 Electrical Characteristics for F-ZTAT Version

26.2.2 DC Characteristics

Table 26.2 DC Characteristics

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Before change

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Note
Active mode current consumption	I_{OPE1}	V_{CC}	Active (high-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	TBD	—	mA	Max. guideline = 1.1 × typ *1 *2 *5
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	TBD	—		Max. guideline = 1.1 × typ *1 *2
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	TBD	TBD		*1 *2
	I_{OPE2}	V_{CC}	Active (medium-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{osc}/64	—	TBD	—	mA	Max. guideline = 1.1 × typ *1 *2 *5
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz, ϕ_{osc}/64	—	TBD	—		Max. guideline = 1.1 × typ *1 *2
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz, ϕ_{osc}/64	—	TBD	TBD		*1 *2
Sleep mode current consumption	I_{SLEEP}	V_{CC}	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	TBD	—	mA	Max. guideline = 1.1 × typ *1 *2 *5
			V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	TBD	—		Max. guideline = 1.1 × typ *1 *2
			V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	TBD	TBD		*1 *2
Subactive mode current consumption	I_{SUB}	V_{CC}	V_{CC} = 2.7 V, 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_W/8)	—	TBD	—	µA	*1 *2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_W/2)	—	TBD	TBD		*1 *2

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Note
Subsleep mode current consumption	I_{SUBSP}	V_{CC}	V_{CC} = 2.7 V, 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	TBD	TBD	µA	*1 *2
Watch mode current consumption	I_{WATCH}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C 32-kHz crystal resonator used	—	TBD	—	µA	*1 *2 *5 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator used	—	TBD	TBD		*1 *2
Standby mode current consumption	I_{STBY}	V_{CC}	V_{CC} = 3.0 V, Ta = 25°C 32-kHz crystal resonator not used	—	0.6	—	µA	*1 *2 Reference value
			32-kHz crystal resonator not used	—	1.0	5.0		*1 *2
RAM data retaining voltage	V_{RAM}	V_{CC}		1.5	—	—	V	
Allowable output low current (per pin)	I_{OL}	Output pins except port 9		—	—	0.5	mA	
		P90 to P93		—	—	15.0		
Allowable output low current (total)	ΣI_{OL}	Output pins except port 9		—	—	20.0	mA	
		Port 9		—	—	TBD		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	Vcc = 2.7 to 3.6 V	—	—	2.0	mA	
			Vcc = 1.8 to 3.6 V	—	—	0.2		
Allowable output high current (total)	$\Sigma - I_{OH}$	All output pins		—	—	10.0	mA	

After change

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Note
Active mode current consumption	I_{OPE1}	V_{CC}	Active (high-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	1.1	—	mA	Max. guideline = 1.1 × typ *1 *2 *5
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	3.4	—		Max. guideline = 1.1 × typ *1 *2
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	7.4	11.0		*1 *2
	I_{OPE2}	V_{CC}	Active (medium-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{osc}/64	—	0.4	—	mA	Max. guideline = 1.1 × typ *1 *2 *5
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz, ϕ_{osc}/64	—	0.7	—		Max. guideline = 1.1 × typ *1 *2
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz, ϕ_{osc}/64	—	1.1	1.5		*1 *2
Sleep mode current consumption	I_{SLEEP}	V_{CC}	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	1.0	—	mA	Max. guideline = 1.1 × typ *1 *2 *5
			V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	2.5	—		Max. guideline = 1.1 × typ *1 *2
			V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	5.2	7.5		*1 *2
Subactive mode current consumption	I_{SUB}	V_{CC}	V_{CC} = 2.7 V, 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_W/8)	—	9.0	—	µA	*1 *2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_W/2)	—	27.0	50.0		*1 *2

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Note
Subsleep mode current consumption	I_{SUBSP}	V_{CC}	V_{CC} = 2.7 V, 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	5.5	9.0	µA	*1 *2
Watch mode current consumption	I_{WATCH}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C 32-kHz crystal resonator used	—	0.5	—	µA	*1 *2 *5 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator used	—	1.5	5.0		*1 *2
Standby mode current consumption	I_{STBY}	V_{CC}	V_{CC} = 3.0 V, Ta = 25°C 32-kHz crystal resonator not used	—	0.1	—	µA	*1 *2 Reference value
			32-kHz crystal resonator not used	—	1.0	5.0		*1 *2
RAM data retaining voltage	V_{RAM}	V_{CC}		1.5	—	—	V	
Allowable output low current (per pin)	I_{OL}	Output pins except port 9		—	—	0.5	mA	
		P90 to P93		—	—	15.0		
Allowable output low current (total)	ΣI_{OL}	Output pins except port 9		—	—	20.0	mA	
		Port 9		—	—	60.0		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	Vcc = 2.7 to 3.6 V	—	—	2.0	mA	
			Vcc = 1.8 to 3.6 V	—	—	0.2		
Allowable output high current (total)	$\Sigma - I_{OH}$	All output pins		—	—	10.0	mA	

Change part 2

Section 26 Electrical Characteristics

26.2 Electrical Characteristics for F-ZTAT Version

26.2.3 AC Characteristics

Table 26.3 Control Signal Timing

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Before change

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min.	Typ.	Max.		
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V (10-MHz version)	2.0	—	10.0	MHz	
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	2.0	—	4.2		
System clock on-chip oscillation frequency	f_{Rosc}		On-chip oscillator for system clock selected V_{CC} = 2.7 to 3.6 V	TBD	—	TBD		*4
			On-chip oscillator for system clock selected V_{CC} = 1.8 to 2.7 V	TBD	—	TBD		
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V (10-MHz version)	100	—	500	ns	Figure 26.14 *2
						(1000)		
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	238	—	500		
						(1000)		
System clock on-chip oscillation clock (ϕ_{ROSC}) cycle time	t_{ROSC}		On-chip oscillator for system clock selected V_{CC} = 2.7 to 3.6 V	TBD	—	TBD		*4
			On-chip oscillator for system clock selected V_{CC} = 1.8 to 2.7 V	TBD	—	TBD		
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}	
				—	—	64	µs	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
Subclock oscillation frequency	f_W	X1, X2		—	32.768 or 38.4	—	kHz	
Watch clock (ϕ_W) cycle time	t_W	X1, X2		—	30.5 or 26.0	—	µs	Figure 26.14
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}			2	—	8	t_W	*1
Instruction cycle time				2	—	—	t_{cyc} t_{subcyc}	
Oscillation stabilization time	t_{rc}	OSC1, OSC2	Ceramic resonator (Vcc = 2.2 to 3.6 V)	—	20	45	µs	Figure 26.23
			Ceramic resonator (other than above)	—	80	—		
			Crystal resonator (V_{CC} = 2.7 to 3.6 V)	—	TBD	TBD		
			Crystal resonator (V_{CC} = 2.2 to 3.6 V)	—	TBD	TBD		
			Other than above	—	—	50	ms	
		On-chip oscillator for system clock	At switching on	—	—	TBD	µs	*4
		X1, X2	V_{CC} = 2.2 to 3.6 V	—	—	2	s	Figure 5.5
			Other than above	—	4	—		
External clock high width	t_{CPH}	OSC1	V_{CC} = 2.7 to 3.6 V (10-MHz version)	40	—	—	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	95	—	—		
		X1		—	15.26 or 13.02	—	µs	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
External clock low width	t_{CPL}	OSC1	V_{CC} = 2.7 to 3.6 V (10-MHz version)	40	—	—	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	95	—	—		
		X1		—	15.26 or 13.02	—	µs	
External clock rising time	t_{CPr}	OSC1	V_{CC} = 2.7 to 3.6 V (10-MHz version)	—	—	10	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	—	—	24		
		X1		—	—	55.0		
External clock falling time	t_{CPf}	OSC1	V_{CC} = 2.7 to 3.6 V (10-MHz version)	—	—	10	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	—	—	24		
		X1		—	—	55.0		
RES pin low width	t_{REL}	RES		10	—	—	t_{cyc}	Figure 26.15 *3

Notes: 1.Selected with the SA1 and SA0 bits in the system control register 2 (SYSCR2).

2.The value in parentheses is tOSC (max.) when an external clock is used.

3.For details on the power-on reset characteristics, refer to table 26.7 and figure 26.15.

4.The specifications may vary due to the effects of temperature, power-supply voltage, and dispersion of product lots. Thorough evaluation under the actual conditions of use is essential in the design of systems. Please confirm with our sales representatives for actual specification.

After change

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V (10-MHz version)	2.0	—	10.0	MHz	
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	2.0	—	4.2		
System clock on-chip oscillation frequency	f_{Rosc}		On-chip oscillator for system clock selected V_{CC} = 1.8 to 3.6 V	0.5	—	10.0		*3
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V (10-MHz version)	100	—	500	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	238	—	500		
System clock on-chip oscillation clock (ϕ_{ROSC}) cycle time	t_{ROSC}		On-chip oscillator for system clock selected V_{CC} = 1.8 to 3.6 V	100	—	2000		*3
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}	
				—	—	64	µs	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
Subclock oscillation frequency	f_W	X1, X2		—	32.768 or 38.4	—	kHz	
Watch clock (ϕ_W) cycle time	t_W	X1, X2		—	30.5 or 26.0	—	µs	Figure 26.14
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}			2	—	8	t_W	*1
Instruction cycle time				2	—	—	t_{cyc} t_{subcyc}	
Oscillation stabilization time	t_{rc}	OSC1, OSC2	Ceramic resonator (Vcc = 2.2 to 3.6 V)	—	20	45	µs	Figure 26.23
			Ceramic resonator (other than above)	—	80	—		
			Crystal resonator (V_{CC} = 2.7 to 3.6 V)	—	0.8	2.0	ms	
			Crystal resonator (V_{CC} = 2.2 to 3.6 V)	—	1.2	3.0		
			Other than above	—	—	50	ms	
		On-chip oscillator for system clock	At switching on	—	—	25	µs	*3
		X1, X2	V_{CC} = 2.2 to 3.6 V	—	—	2	s	Figure 5.5
			Other than above	—	4	—		
External clock high width	t_{CPH}	OSC1	V_{CC} = 2.7 to 3.6 V (10-MHz version)	40	—	—	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	95	—	—		
		X1		—	15.26 or 13.02	—	µs	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
External clock low width	t_{CPL}	OSC1	V_{CC} = 2.7 to 3.6 V (10-MHz version)	40	—	—	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	95	—	—		
		X1		—	15.26 or 13.02	—	µs	
External clock rising time	t_{CPr}	OSC1	V_{CC} = 2.7 to 3.6 V (10-MHz version)	—	—	10	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	—	—	24		
		X1		—	—	55.0		
External clock falling time	t_{CPf}	OSC1	V_{CC} = 2.7 to 3.6 V (10-MHz version)	—	—	10	ns	Figure 26.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	—	—	24		
		X1		—	—	55.0		
RES pin low width	t_{REL}	RES		10	—	—	t_{cyc}	Figure 26.15 *2

Notes: 1.Selected with the SA1 and SA0 bits in the system control register 2 (SYSCR2).

2.For details on the power-on reset characteristics, refer to table 26.7 and figure 26.15.

3.The specifications may vary due to the effects of temperature, power-supply voltage, and dispersion of product lots. Thorough evaluation under the actual conditions of use is essential in the design of systems. Please confirm with our sales representatives for actual specification.

Change part 3

Section 26 Electrical Characteristics

26.2 Electrical Characteristics for F-ZTAT Version

26.2.5 LCD Characteristics

Table 26.7 LCD Characteristics

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Before change

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min.	Typ.	Max.		
Segment driver drop voltage	V_{DS}	SEG1 to SEG40	I_D = 2 µA V1 = 2.7 to 3.6 V	—	—	0.6	V	*1
Common driver drop voltage	V_{DC}	COM1 to COM4	I_D = 2 µA V1 = 2.7 to 3.6 V	—	—	0.3	V	*1
LCD power supply split-resistance	R_{LCD}		Between V1 and V_{SS}	1.5	3.0	7.0	MΩ	
LCD display voltage	V_{LCD}	V1		2.2	—	3.6	V	*2
V3 power supply voltage	V_{LCD3}	V3	Between V3 and V_{SS}	0.9	1.0	1.1	V	*3*4
V2 power supply voltage	V_{LCD2}	V2	Between V2 and V_{SS}	—	2.0 (V_{LCD3} × 2)	—	V	*3*4
V1 power supply voltage	V_{LCD1}	V1	Between V1 and V_{SS}	—	3.0 (V_{LCD3} × 3)	—	V	*3*4
3-V constant voltage LCD power supply circuit current consumption	I_{LCD}	Vcc	Vcc = 3.0 V Booster clock: 125 kHz	—	20	—	µA	Reference value*4*5

After change

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min.	Typ.	Max.		
Segment driver drop voltage	V_{DS}	SEG1 to SEG40	I_D = 2 µA V1 = 2.7 to 3.6 V	—	—	0.6	V	*1
Common driver drop voltage	V_{DC}	COM1 to COM4	I_D = 2 µA V1 = 2.7 to 3.6 V	—	—	0.3	V	*1
LCD power supply split-resistance	R_{LCD}		Between V1 and V_{SS}	1.5	3.0	7.0	MΩ	
LCD display voltage	V_{LCD}	V1		2.2	—	3.6	V	*2
V3 power supply voltage	V_{LCD3}	V3	Between V3 and V_{SS}	0.9	1.0	1.1	V	*3*4
V2 power supply voltage	V_{LCD2}	V2	Between V2 and V_{SS}	—	2.0 (V_{LCD3} × 2)	—	V	*3*4
V1 power supply voltage	V_{LCD1}	V1	Between V1 and V_{SS}	—	3.0 (V_{LCD3} × 3)	—	V	*3*4
3-V constant voltage LCD power supply circuit current consumption	I_{LCD}	Vcc	Vcc = 2.7 V Booster clock: 32.768 kHz	—	12	—	µA	Reference value*4*5

Change part 4

Section 26 Electrical Characteristics

26.2 Electrical Characteristics for F-ZTAT Version

26.2.8 Flash memory Characteristics –Preliminary-

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Before change

26.2.8 Flash memory Characteristics **–Preliminary-**

Condition A:

AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, V_{CC} = 2.7 V to 3.6 V (operating voltage range in reading), V_{CC} = 3.0 V to 3.6 V (operating voltage range in programming/erasing),

Ta = –20 to +75°C (operating temperature range in programming/erasing: regular specifications, wide-range specifications)

Condition B:

AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, V_{CC} = 1.8 V to 3.6 V (operating voltage range in reading), V_{CC} = 3.0 V to 3.6 V (operating voltage range in programming/erasing),

Ta = –20 to +50°C (operating temperature range in programming/erasing: regular specifications, **wide-range specifications**)

After change

26.2.8 Flash memory Characteristics

Condition A:

AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, V_{CC} = 2.7 V to 3.6 V (operating voltage range in reading), V_{CC} = 3.0 V to 3.6 V (operating voltage range in programming/erasing),

Ta = –20 to +75°C (operating temperature range in programming/erasing: regular specifications, wide-range specifications)

Condition B:

AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, V_{CC} = 1.8 V to 3.6 V (operating voltage range in reading), V_{CC} = 3.0 V to 3.6 V (operating voltage range in programming/erasing),

Ta = –20 to +50°C (operating temperature range in programming/erasing: regular specifications)